International
IOR Rectifier

IR3510

DATA SHEET

HOT-SWAP N+1 REDUNDANT XPHASE CONTROL IC

DESCRIPTION

The IR3510 Hot-Swap N+1 Redundant X-Phase Controller combines input isolation control for hot-swappable application, X-Phase VRM/VRD control and output OR-ing control for N+1 redundant application. It interfaces with microcontroller and X-Phase phase ICs to provide a full featured and flexible solution for powering high-end CPUs and servers.

The IR3510 interfaces with system logic to receive “ENABLE”, “VSET” which is the analog reference voltage for controlling VRM output voltage, constant current limit “OCPSET” and OVP limit “OVPSET”. It feeds back to the system load current “IO”, VRM status “VRRDY”, OR-ing FETs status “ORING” and input fault “IOCD”.

The IR3510 works with existing X-Phase phase ICs to provide a full featured multiphase VRM control, including soft-start, voltage regulation, constant current limit, remote sense and open sense leads protection.

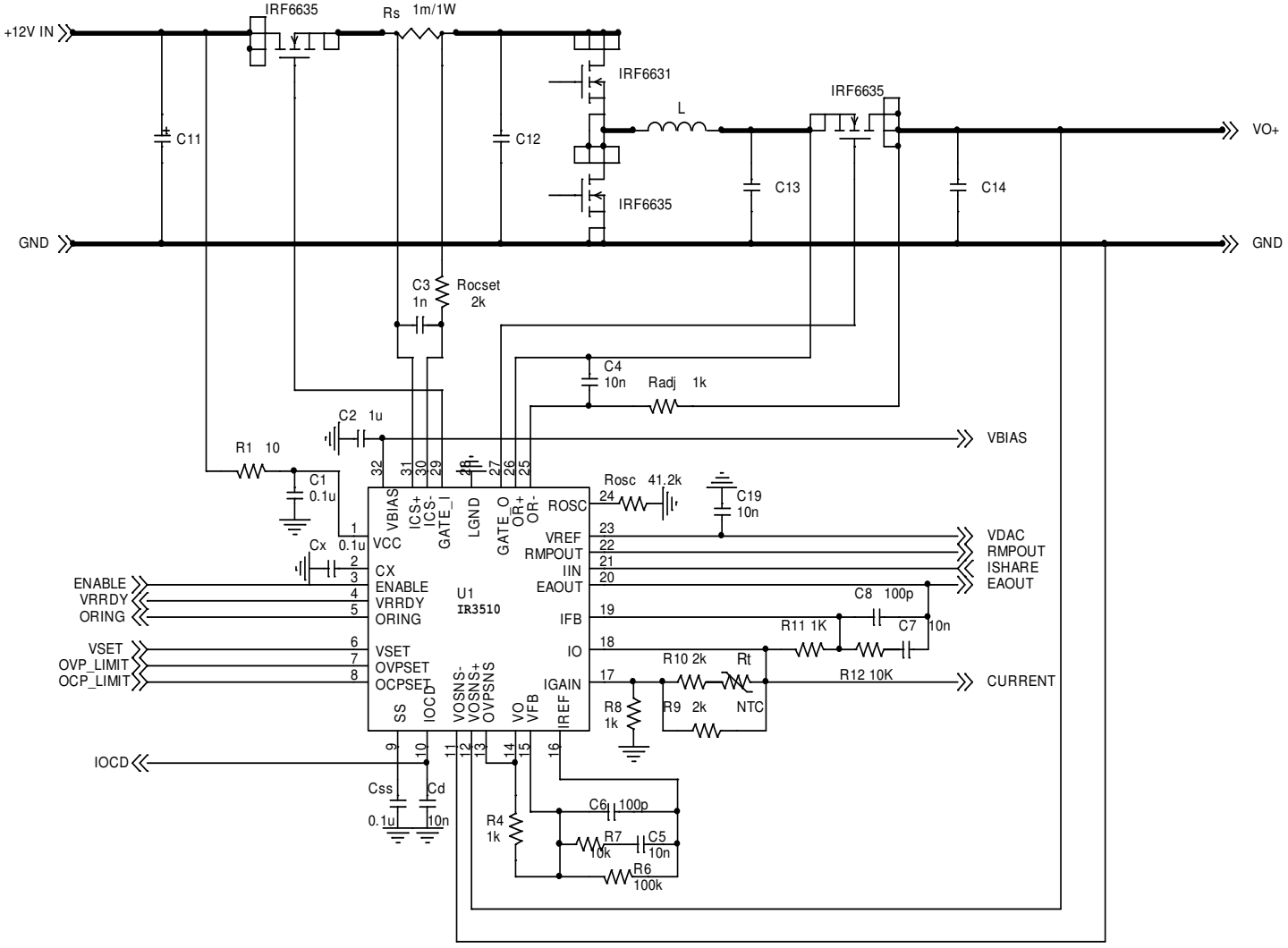
The IR3510 continuously monitors the 12V input current and VRM output voltage. Once the input current exceeds the programmable threshold, it goes to current limit mode and turn off the input FETs when the OC delay times out. It immediately turns off the input FETs when an OV condition is detected on the VRM output. It also has UVLO for both the 12V input and the supply voltage to the VRM.

The IR3510 has built-in OR-ing control function for N+1 redundant application. When the VRM output voltage is higher than the output voltage bus, it turns on the OR-ing FETs; When the VRM output is sinking current from the output voltage bus, it turns off the OR-ing FETs.

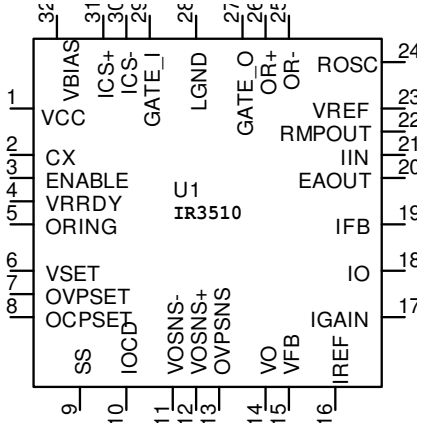
FEATURES

- Two ENABLE thresholds for turning on input FET and VRM output
- Input isolation FET control for hot-swap, input OCP and output OVP
- Programmable input OCP limit and delay
- Input isolation FET short detection
- Integrated Charge Pump drives input isolation FETs and output OR-ing FETs
- Programmable 150KHz to 1MHz oscillator
- Programmable two-stage soft-start
- Analog voltage setting for output voltage control, OVP limit and OCP limit
- True remote voltage sense with open-sense-lead protection
- Programmable output impedance
- Gain adjustable analog load current report with thermal compensation capability
- Average Current Mode control improving current sharing between paralleled modules
- Constant output current limit
- Compatible with existing IR3086A and IR3088A Phase ICs
- OR-ing control with adjustable reverse current cut-off threshold
- Input Fault, VRRDY and OR-ing status indications
- Operation from 12V input with 9V Under-Voltage Lockout
- 6.8V Bias Voltage provides system reference
- 32-lead MLPQ 5x5mm package

APPLICATION CIRCUIT



PACKAGE



(MLPQ-32, 5x5 mm, 34°C/W)

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature…….. 0 °C to 150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……3
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	VCC	20V	-0.3V	1mA	200mA
2	CX	30V	-0.3V	1mA	1mA
3	ENABLE	20V	-0.3V	1mA	1mA
4	VRRDY	20V	-0.3V	1mA	20mA
5	ORING	20V	-0.3V	1mA	20mA
6	VSET	10V	-0.3V	1mA	1mA
7	OVPSET	10V	-0.3V	1mA	1mA
8	OCPSET	10V	-0.3V	1mA	1mA
9	SS	10V	-0.3V	1mA	1mA
10	IOCD	10V	-0.3V	1mA	1mA
11	VOSNS-	0.5V	-0.5V	1mA	1mA
12	VOSNS+	10V	-0.5V	1mA	1mA
13	OVPSNS	10V	-0.3V	1mA	1mA
14	VO	10V	-0.3V	10mA	10mA
15	VFB	10V	-0.3V	1mA	1mA
16	IREF	10V	-0.3V	5mA	5mA
17	IGAIN	10V	-0.3V	1mA	1mA
18	IO	10V	-0.3V	20mA	10mA
19	IFB	10V	-0.3V	1mA	1mA
20	EAOUT	10V	-0.3V	5mA	5mA
21	IIN	10V	-0.3V	1mA	1mA
22	RMPOUT	10V	-0.3V	1mA	1mA
23	VREF	10V	-0.3V	10mA	1mA
24	ROSC	10V	-0.3V	1mA	1mA
25	OR-	10V	-0.3V	1mA	1mA
26	OR+	10V	-0.3V	1mA	1mA
27	GATE_O	25V	-0.3V DC, -2V for 100ns	1A for 100ns, 200ma DC	1A for 100ns, 200ma DC
28	LGND	n/a	n/a	50mA	1mA
29	GATE_I	30V	-0.3V DC, -2V for 100ns	1A for 100ns, 200ma DC	1A for 100ns, 200ma DC
30	ICS-	20V	-0.3V	1mA	1mA
31	ICS+	20V	-0.3V	1mA	1mA
32	VBIAS	10V	-0.3V	200mA	50mA

PIN DESCRIPTION

PIN#	PIN NAME	PIN DESCRIPTION
1	VCC	Power input for internal circuitry.
2	CX	Connect external cap for charge pump
3	ENABLE	Enable input. Lower level threshold turns on input FET, Higher level threshold turns on VRM output.
4	VRRDY	Open collector output indicating VRM soft-start end and no fault.
5	ORING	Open collector output indicating the OR-ing FET is on
6	VSET	Analog input sets VRM no-load output voltage. Non-inverting input to voltage error amplifier.
7	OVPSET	Analog input sets the OVP threshold which is relative to VSET.
8	OCPSET	Analog input sets the constant current limit threshold.
9	SS	Connect a capacitor to LGND to set input and output soft-start time.
10	IOCD	Connect a cap to LGND to set input OCP delay. Logic HIGH indicating input Fault.
11	VOSNS-	Remote sense amplifier input. Connect to ground at the load.
12	VOSNS+	Remote sense amplifier input. Connect to output at load.
13	OVPSNS	OVP sense input. Connect resistor divider to VO to program OVP threshold.
14	VO	Remote sense amplifier output.
15	VFB	Inverting input to the voltage error amplifier.
16	IREF	Voltage error amplifier output.
17	IGAIN	Inverting input to current report amplifier. Connecting external resistor divider to set gain.
18	IO	Analog output represents the VRM average output current.
19	IFB	Current feedback to the inverting input of current error amplifier.
20	EAOUT	Output of the current error amplifier.
21	IIN	Average phase current sense input from the phase ICs.
22	RMPOUT	Oscillator Output voltage. Used by Phase ICs to program phase timing
23	VREF	Buffered VSET, output to phase ICs VDAC pin.
24	ROSC	Connect a resistor to LGND to set oscillator frequency.
25	OR-	Output voltage at the DRAIN side of OR-ing FET.
26	OR+	Output voltage at the SOURCE side of OR-ing FET.
27	GATE_O	OR-ing FET gate drive signal.
28	LGND	Local Ground for internal circuitry and IC substrate connection
29	GATE_I	Input isolation FET gate signal
30	ICS-	Inverting input to the input current sense amplifier.
31	ICS+	Non-inverting input to the input current sense amplifier.
32	VBIAS	6.75V regulated output used as a system reference voltage for internal circuitry and the Phase ICs. It can also be used as external reference.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 8.1V ≤ VCC ≤ 16V, 0 °C ≤ T_J ≤ 100 °C, Rosc = 42KΩ

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VBIAS Regulator					
Output Voltage	-20mA ≤ I(VBIAS) ≤ 0mA C(VBIAS) = 1u	6.5	6.75	7.0	V
Charge Pump					
Output Voltage Above VCC	9V ≤ V(VCC) ≤ 16V, Cx = 0.01uF	6			V
Output Voltage Above VCC	V(VCC) = 9V, Cx = 0.01uF	5.3			V
Voltage Clamp		25	27	29	V
Input UVLO1					
Start Threshold Voltage	**Note 1**	8.7	9	**9.3**	V
Stop Threshold Voltage		7.95	8.2	8.5	V
Hysteresis	**Note 1**	**0.6**	0.8	1.0	V
ENABLE Input					
Enable 1Threshold Voltage	V(ENABLE) rising	0.5	0.6	0.7	V
Enable 1Threshold Voltage	V(ENABLE) falling	0.45	0.55	0.65	V
Hysteresis		25	50	75	mV
Enable 2Threshold Voltage	V(ENABLE) rising	1.05	1.15	1.25	V
Enable 2Threshold Voltage	V(ENABLE) falling	1.0	1.1	1.2	V
Hysteresis		25	50	75	mV
Pull-up Voltage		0.825	0.875	0.925	V
Pull-up Resistance		5	10	20	KΩ
Input Resistance	V(ENABLE) > 0.95V	50	100	200	KΩ
Input Fault Latch Reset Falling Edge Delay	Note 2	1.2	2	2.8	us
Soft-Start					
SS to VFB Input Offset Voltage	With V(VFB) = 0V, adjust V(SS) until V(IREF) drives high	0.75	1.35	1.6	V
Soft-Start Time	Css = 0.1u	3.5	5	10	ms
Charge Voltage		3.575	3.775	3.975	V
Charge Comparator Threshold Voltage	Relative to Charge Voltage, V(SS) rising	40	80	140	mV
Charge Comparator Threshold Voltage	Relative to Charge Voltage, V(SS) falling	105	145	200	mV
Charge Comparator Hysteresis		40	65	90	mV
Discharge Time	1V ≤ V(SS) ≤ 3.5V	50	225	500	us
Discharge Comparator Threshold		180	230	280	mV
VRRDY Output Voltage	I(VRRDY) = 4mA	0	150	400	mV
VRRDY Output Voltage	V(VCC) = 2V, I(VRRDY) = 1mA	0	150	400	mV
VRRDY Leakage Current	V(VRRDY) = 3.3V		0	10	μA

Input Soft-Start Regulator					
Gain	V(SS) = 2V	4.0	4.5	5.1	V/V
Transconductance	Note 2		200		µA/V
Bandwidth	Note 2, Cgate_i = 10n		4		KHz
Sink Current	2V ≤ V(GATE_I) ≤ V(CX)	7	15	23	µA
Input OC Regulator					
Input Offset Voltage	0V ≤ V(ICS+), V(ICS)- ≤ V(VCC)	-10	0	10	mV
ICS+ Input Impedance	0V ≤ V(ICS)+ ≤ V(VCC)	25	43	86	KΩ
ICS- Bias Current	0V ≤ V(ICS)- ≤ V(VCC)	-20	-22	-24	µA
OC Regulator Transconductance	Note 2, I(GATE_I) = 0A		140		µA/mV
OC Regulator Bandwidth	Note 2, Cgate_i = 10n, Rgate_i = 100		350		KHz
OC Time-out Threshold Voltage		0.7	0.8	0.9	V
OC Pull-down Current	3V ≤ V(GATE_I) ≤ V(CX)	25	75	115	mA
Severe Over-Current Threshold	Above V(ICS-)	40	60	95	mV
IOCD Charge Current	V(IOCD) = 0, 2V	- 19.5	-21.5	- 23.5	µA
IOCD Charge Voltage	Float IOCD	2.7	3	3.3	V
IOCD Discharge Time	0.8V ≤ V(IOCD) ≤ 3, C(IOCD) = 10n	0.2	3.5	5	us
IOCD Discharge Voltage	Float IOCD	0	50	100	mV
Input FET Gate Driver					
Turn-on Current	V(GATE_I) = V(VCC)	- 19	- 25	- 31	µA
Gate Fall Time	V(GATE_I) from 0.9 V(CX) to V(VCC) V(VCC) = 12V, Cgate_i = 10n	40	110	250	ns
GATE_I response to OC	Note 2	0.05	0.2	0.6	us
GATE_I response to Severe OC	Note 2, 50mv Over-Drive	0.025	0.1	0.25	us
Clamping Voltage	V(GATE_I) – V(ICS+)	9	13	16	V
VR Input UVLO2					
Start Threshold Voltage		8.7	8.9	9.3	V
Stop Threshold Voltage		7.9	8.1	8.5	V
VR Input UVLO Hysteresis		0.6	0.8	1.0	V
(UVLO1) – (UVLO2)	Stop Threshold Voltage	-180	90	350	mV
Oscillator					
Switching Frequency		255	300	345	KHz
Peak Voltage (5V typical, measured as % of VBIAS)		68	70.5	73	%
Valley Voltage (1V typical, measured as % of VBIAS)		11	14	16	%
VROSC	ROSC = 42K	1.220	1.232	1.244	V

Voltage Error Amplifier					
Input Offset Voltage	**Note 1**, 0.5V ≤ V(IREF)= V(VFB) ≤ 1.6V	**-5**	0	**5**	mV
VFB Bias Current	0.5V ≤ V(VFB) ≤ 1.6V	-0.5	0	0.5	µA
VSET Bias Current	0.5V ≤ V(VSET) ≤ 1.6V	-0.5	0	0.5	µA
DC Gain	Note 2	90	100	110	dB
Bandwidth	Note 2	4	8	12	MHz
Slew Rate	Note 2	1.4	3.2	5	V/µs
Source Current	V(IREF) = 1V	0.4	0.7	1.2	mA
Sink Current	V(IREF) = 1V	0.5	1.1	1.7	mA
Maximum Voltage	V(VBIAS)– V(IREF) (ref. to VBIAS)	150	350	600	mV
Minimum Voltage		30	125	200	mV
OC Clamping Buffer					
Input Offset Voltage	Measure V(EAOUT)-V(OCPSET), V(EAOUT)= V(IFB), V(OCPSET)=3V	-30	4	35	mV
OCPSET Bias Current	0.5V ≤ V(OCPSET) ≤ 4V	-2	0	2	µA
Current Error Amplifier					
Input Offset Voltage	0.5V ≤ V(EAOUT)=V(IFB) ≤ 4V, V(EAOUT)- V(IREF)	200	300	400	mV
IFB Bias Current	0.5V ≤ V(IFB) ≤ 4V	-2	0	2	µA
DC Gain	Note 2	90	100	110	dB
Bandwidth	Note 2	4	8	12	MHz
Slew Rate	Note 2	1.4	3.2	5	V/µs
Source Current	V(EAOUT) = 1V	0.4	0.7	1.2	mA
Sink Current	V(EAOUT) = 1V	0.4	1.1	1.7	mA
Maximum Voltage	Measure V(VBIAS) – V(EAOUT)	150	350	600	mV
Minimum Voltage		30	125	200	mV
VREF Buffer Amplifier					
Input Offset Voltage	0.5V ≤ VSET ≤ 1.6V	-6	-1	4	mV
Source Current	0.5V ≤ VSET ≤ 1.6V	85	165	240	uA
Sink Current	0.5V ≤ VSET ≤ 1.6V	1.5	5	9.5	mA
IIN Precondition Circuit					
Pull-down Resistance	V(SS) = 0	5	10	20	KΩ
Set Comparator Threshold	V(SS)	350	600	850	mV
Reset Comparator Threshold	V(EAOUT)	200	350	500	mV
Current Report Amplifier					
Input Offset Voltage	V(IGAIN) = V(IO), V(VREF)= V(IIN)	175	200	225	mV
IIN Bias Current	0V ≤ V(IIN) ≤ 4V	-1	0	1	µA
IGAIN Bias Current	0 ≤ V(IGAIN) ≤ 4V	-1	0	1	µA
Unity Gain Bandwidth	Note 2	1	4	8	MHz

Slew Rate	Note 2, V(IO)-V(IIN)	0.7	1.4	2.4	V/µs
Minimum Output Voltage	V(IGAIN) = V(IO), V(IIN) = V(VREF) – 0.1V	75	100	125	mV
Source Current	0.2V ≤ V(IO) ≤ 4V	2	6	11	mA
Sink Current	V(IO) = 0.5V	0.45	2	5	mA
OVP Comparator					
Threshold Voltage Rising	0.5V ≤ V(OVPSET) ≤ 4V	-10	0	10	mV
Threshold Voltage Falling	Note 2, 0.5V ≤ V(OVPSET) ≤ 4V	-45	-65	-95	mV
OVPSET Bias Current	0.5V ≤ V(OVPSET) ≤ 4V	-2	0	2	µA
OVPSNS Bias Current	0.5V ≤ V(OVPSNS) ≤ 4V	-2	0	2	µA
OVP Delay Time		3.5	6.5	9.5	us
BB Disable Clamp					
Input Offset Voltage	0.5V ≤ VREF ≤ 1.6V	-20	0	20	mV
Remote Sense Differential Amplifier					
Input Offset Voltage	**Note 1**,(VOSNS+) – (VOSNS-) = 0.8V	- 10	- **4**	3	mV
Input Offset Voltage	**Note 1**,(VOSNS+) – (VOSNS-) = 1.2V	- 12	- **3**	6	mV
Input Offset Voltage	**Note 1**,(VOSNS+) – (VOSNS-) = 5.5V	- 30	**10**	50	mV
VOSNS+ Bias Current	0.5V ≤ V(VOSNS+) ≤ 1.6V	4	15	25	uA
VOSNS- Bias Current	-0.3V ≤ V(VOSNS-) ≤ 0.3V	4	-15	-25	uA
Unity Gain Bandwidth	Note 2		4		MHz
VOSNS+ Input Voltage Range		0.5		5.5	V
Slew Rate	0.5V≤V(VOSEN+) - V(VOSEN-)≤5.5V	1	2	3.5	V/us
Source Current	0.5V≤V(VOSNS+) – V(VOSNS-)≤5.5V	5	15	19	mA
Sink Current	0.5V≤V(VOSNS+) – V(VOSNS-)≤5.5V	0.6	1	1.5	mA
Open Sense Lead Comparator					
Sense Line Detection Active Comparator Threshold Voltage		80	210	350	mV
Sense Line Detection Active Comparator Offset Voltage	V(VO) < [V(VOSNS+) – V(LGND)] / 2	40	65	90	mV
VOSNS+ Open Sense Line Comparator Threshold	Note2, Compare to VBIAS		90		%
VOSNS- Open Sense Line Comparator Threshold	Note 2		0.4		V
Sense Lines Source Currents	V(VO) = 100mV	250	500	700	uA
Open Sense Timer		3	5	7	us
OR-ing Control Comparator					
Offset Voltage	**Note 1**, 0.5V ≤ VOR+ = VOR- ≤ 5.5V	**-2**	0	**2**	mV
Hysteresis		10	32.5	55	mV
OR+ Bias Current	0.5V ≤ VOR+ ≤ 5.5V	-2	0	2	uA
OR- Bias Current	0.5V ≤ VOR- ≤ 5.5V	22	30	38	uA
ORING Output Voltage	I(ORING) = 4mA	0	150	400	mV
ORING Leakage Current	V(ORING) = 3.3V		0	10	uA

OR-ing FET Gate Driver					
GATE_O Pull-up Resistor		2	4	6	KΩ
GATE_O Charge Current	V(GATE_O) ≥ VCC	- 10	- 12.5	- 15	uA
Gate Turn-off Time	Cgate_o = 10n 2V ≤ V(GATE_O) – V(OR+) ≤ 10V	35	120	200	ns
Turn-off Delay Time	V(OR-) – V(OR+) = 150mV	80	140	200	ns
Voltage Clamping	V(GATE_O) – V(OR+)	9	14	17.5	V
General					
VCC Supply Current		20	28	36	mA

Note 1: Critical Parameters.
Note 2: Guaranteed by design, but not tested in production.

PIN FUNCTIONS

"VCC" (PIN#1): 12V bias voltage input for internal circuit**.** Connecting a 1uF decoupling cap is recommended.

"CX" (PIN#2): Charge-pump output. It is internally clamped to 27V typical and 29V max. Connecting a 0.1uF / 50V cap to GND is required.

"Enable" (PIN#3): Input FET and voltage regulator output enable input. It has two-level threshold. The lower level threshold of 0.7V turns on the input FET. The higher level threshold of 1.2V turns on the voltage regulator output. It has internal pull-up to 0.9V, so when it is float, it has the voltage above the lower level threshold and turns on input FET. When it is pulled down, both input FET and voltage regulator output are turned off.

"VRRDY" (PIN#4): Open collector output indicating that the soft-start is completed and there is no fault. It requires external pull-up.

"ORING" (PIN#5): Open collector output indicating Oring FET status. It requires external pull-up. HIGH indicates the Oring FET is ON; LOW indicates the Oring FET is OFF.

"VSET" (PIN#6): Analog input setting the no-load output voltage. It is internally connected to the non-inverting input of voltage error amplifier.

"OVPSET" (PIN#7): Analog input setting the Over-Voltage Protection threshold voltage. The internal OVP circuit compares the voltage on the "OVPS" pin and the voltage on this pin to determine the OV condition.

"OCPSET" (PIN#8): Analog input setting the constant current limit. The internal constant current limit circuit limits the "IO" pin voltage, which is the current report voltage, to be no more than the voltage set on this pin.

"SS" (PIN#9): Soft-start pin. Connect a capacitor to GND to set the soft-start time. An internal current source flowing out of this pin charges the cap to a fixed threshold to set the soft-start time. It controls both the input FET soft-start and the voltage regulator output voltage soft-start.

"IOCD" (PIN#10): Input FET fault indication output. Connect a capacitor to GND to program the input OCP delay time. Any fault condition which results turning off the input FET, including input FET short, input OCP and output OVP, will cause this pin be pulled HIGH.

"VOSNS-" (PIN#11): Negative remote sense input. It is internally connected to the inverting input of the differential voltage sense amplifier.

"VOSNS+" (PIN#12): Positive remote sense input. It is internally connected to the non-inverting input of the differential voltage sense amplifier.

"OVPSNS" (PIN#13): OVP sense input. It can be connected to "VO" pin if there is no feedback divider. If the output voltage is higher than the "VSET" voltage, a feedback resistor divider is required, and this pin needs to be connected to "VFB" pin. To disable internal OVP function, connecting this pin to GND.

"VO" (PIN#14): Remote sense voltage output. If the output voltage is higher than the "VSET" voltage, a feedback resistor divider is required to be connected to this pin.

"VFB" (PIN#15): Voltage feedback input. It is internally connected to the inverting input of the voltage error amplifier.

"IREF" (PIN#16): Voltage error amplifier output. It is also the current reference input to the current error amplifier. It is clamped by the "OCSET" voltage when it is running in constant current limit mode.

"IGAIN" (PIN#17): Inverting input to the current report amplifier. Connect a resistor network between this pin and the "IO" pin to program the current report amplifier gain.

"IO" (PIN#18): Current report amplifier output representing the output load current. In order to measure negative output current in a paralleling system, a fixed 200mv input offset voltage is added to the current report amplifier. At no load, it reports this offset voltage, which is amplified by the current report gain.

"IFB" (PIN#19): Current feedback input. It is internally connected to the inverting input of the current error amplifier. The output of "IO" pin is connected to this pin through a resistor.

"EAOUT" (PIN#20): Current error amplifier output. Connect it to the "EA" pin of the phase IC to control the PWM duty cycle.

"IIN" (PIN#21): Current sense input from the phase IC. It has an offset voltage of "VREF" voltage. Connect it to the "ISHARE" pin of the phase IC.

"RMPOUT" (PIN#22): Oscillator triangle waveform output. Connect it to the "RMPIN" pin of the phase IC to set the switching frequency and phase timing. The frequency of this ramp signal is programmed by the resistor connected to the "ROSC" pin.

"VREF" (PIN#23): Buffered output of "VSET" voltage. Connect it to the "DACIN" pin of the phase IC to set the "IIN" offset voltage and the PWM ramp floor voltage.

"ROSC" (PIN#24): Connect an external resistor to program the switching frequency. The lower the resistor value, the higher the switching frequency. The voltage on this pin can be used as a voltage reference with 1% tolerance. It is 1.230V typical with Rosc = 42K.

"OR-" (PIN#25): Oring comparator inverting input. Connect it to the DRAIN side of the Oring FET through a programming resistor. A constant current source flowing out of this pin goes through that programming resistor to set the reverse current cut-off threshold.

"OR+" (PIN#26): Oring comparator non-inverting input. Connect it to the SOURCE side of the Oring FET.

"GATE_O" (PIN#27): Oring FET gate driver output. It is driven by the internal charge-pump with 10uA charging and 2A discharging currents. It also has internal 3k resistor pulled-up to VIN to speed up the turn-on of Oring FET.

"LGND" (PIN#28): Local GND for Internal circuit and IC substrate connection.

"GATE_I" (PIN#29): Input FET driver output. It is driven by the internal charge-pump with 20uA charging and 2A discharging currents.

"ICS-" (PIN#30): Inverting input to the input current sense comparator. Connect it to the downstream of the input current sense resistor through a programming resistor. A constant current source flowing out of this pin goes through the programming resistor to set the input OCP threshold.

"ICS+" (PIN#31): Non-inverting input to the input current sense comparator. Connect it to the upstream of the input current sense resistor.

"VBIAS" (PIN#32): 6.7V regulated output voltage. It is used as a system reference voltage for the internal circuits and the phase IC. It can also be used as external voltage reference.

SYSTEM THEORY OF OPERATION

XPhase™ Voltage Regulator Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can be used in any multiphase converter ranging from 1 to 16 or more phases where flexibility facilitates the design tradeoff of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 1, the *XPhase*™ architecture consists of an IR3510 Control IC and a scalable array of phase converters each using a single Phase IC IR3088A. The IR3510 Control IC communicates with the Phase ICs through a 5–wire analog bus, i.e. bias voltage, reference voltage, phase timing, error amplifier output and average phase current. The IR3510 control IC has the functions of reference voltage, bias voltage, PWM ramp oscillator, soft-start, voltage error amplifier, current error amplifier, current limit, current report and fault protections etc. The IR3088A Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over voltage protection, and current sensing and sharing.

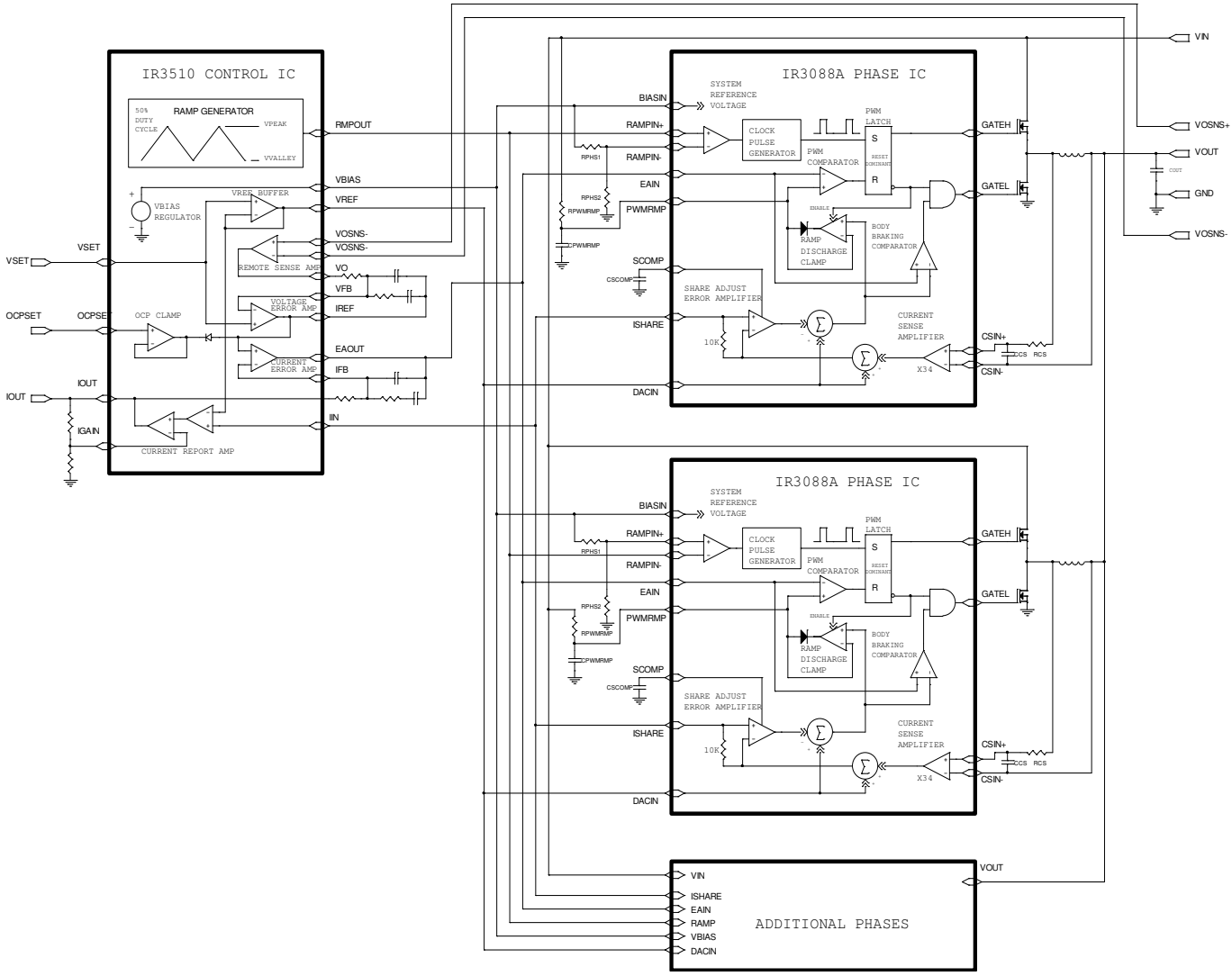


Figure 1 – System Block Diagram

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point–to–point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is also shown in Figure 1. Average current mode control with trailing edge modulation is used. Dual error amplifiers, outer loop voltage error amplifier and inner loop current error amplifier, are used in the Control IC to control the PWM duty cycle. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed–forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.

Frequency and Phase Timing Control

The oscillator is located in the Control IC and its frequency is programmable from 150 kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 4.8V and 0.9V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 4 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP + and – pins.

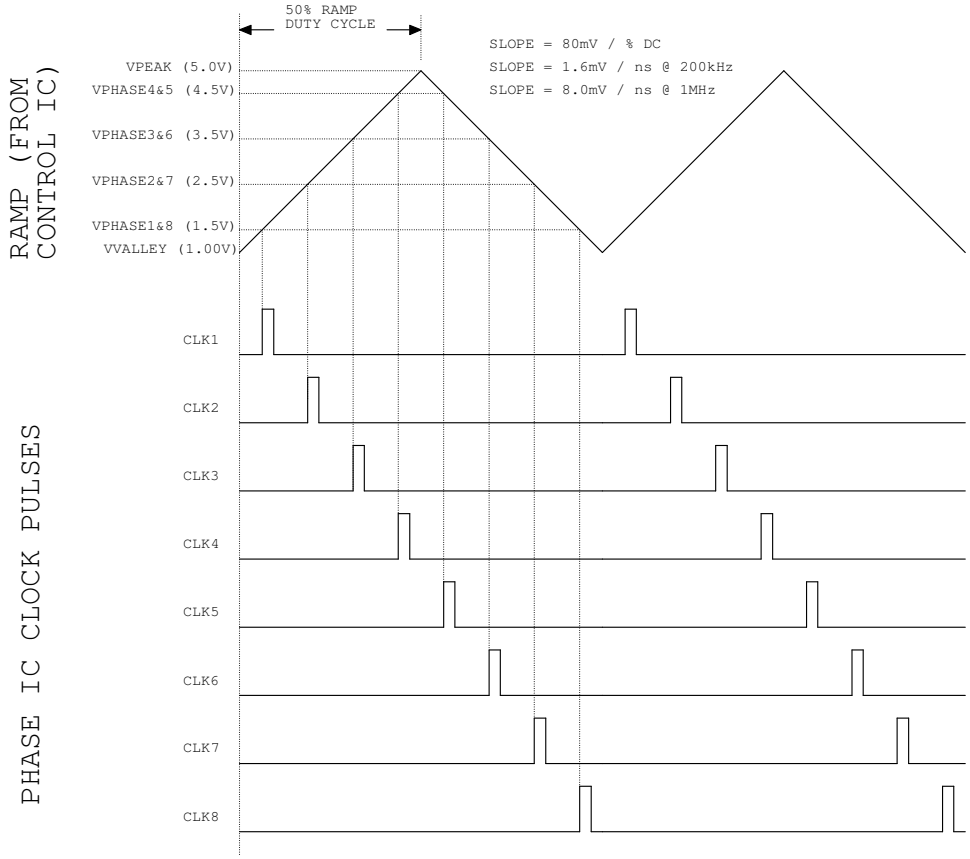


Figure 2 – 8 Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the EAOUT voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide “single cycle transient response” where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VREF.

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier’s body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as “body braking” and is accomplished through the “0% Duty Cycle Comparator” located in the Phase IC. If the Error Amp’s output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

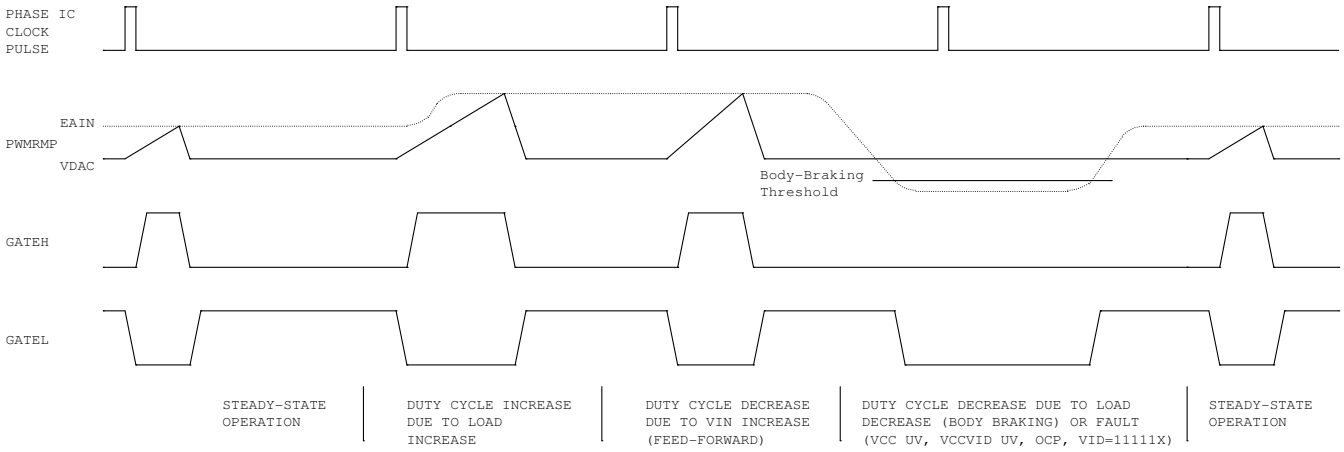


Figure 3 – PWM Operating Waveforms

Loss-less inductor current sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor.

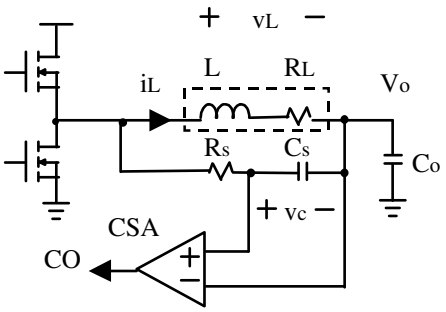


Figure 4 – Inductor Current Sensing and Current Sense Amplifier

The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_SC_S} = i_L(s)\frac{R_L+sL}{1+sR_SC_S}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of RL was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak–to–average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak–to–average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the Phase IC, as shown in Figure 1. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (–1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor, these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to –20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases

are tied together and the voltage on the share bus represents the average inductor current through all the inductors and is used by the Control IC for voltage positioning and current limit protection

Average Phase Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

Average current mode control with limited voltage loop gain

Redundant system requires good current sharing between voltage regulators to reduce electrical/thermal stress on each module and improve system reliability. There are several current sharing schemes for paralleling voltage regulators. Most of them require a common current share bus which represents the average current or maximum current in the paralleling system. But, this common current share bus can cause single point of failure if it is shorted or opened.

To eliminate single-point failure, but still have good current sharing between paralleled voltage regulators for high-reliability redundant system application, a novel average current mode control with limited voltage loop gain scheme can be used.

As shown in Fig. 5, there is no common current share bus between modules. By using limited voltage error gain, the current reference to the non-inverting input of the current error amplifier is identical for each module, because each module has the same voltage reference and the same remote sense feedback voltage. The average current control loop will force each module to carry the same amount of load current.

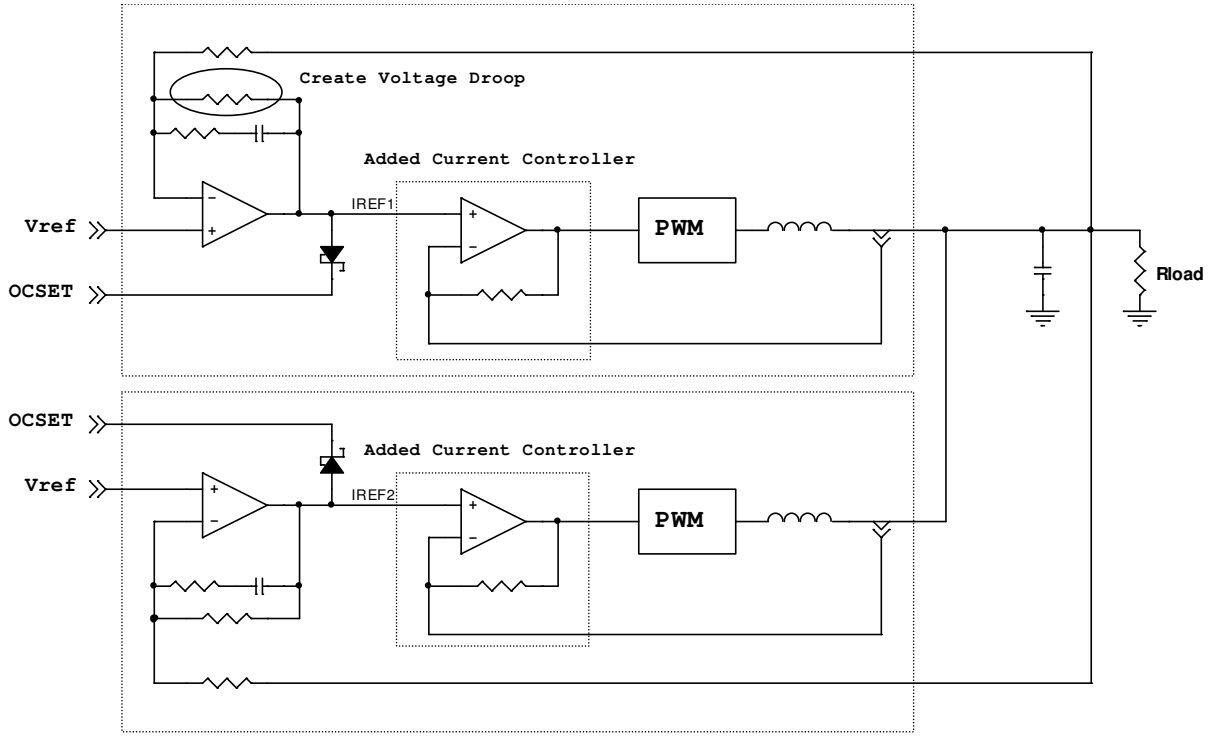


Fig. 5 Average current mode control with limited voltage loop gain

The limited voltage loop DC gain controls the voltage droop,

$$Vdroop = (Kv\ Ki / Gv)\ Io,$$

Where, Kv is the voltage feedback divider factor, Ki is current sense gain, and Gv is the voltage loop DC gain.

The average current mode control also provides constant current limit function for the voltage regulator output, which is a desired feature for redundant power system.

Input Soft-Start for Hot-Swappable applications

For hot-swappable applications, an input control FET in series with the input voltage is required to prevent the voltage regulator from pulling down the VIN bus during start-up due to large input caps or pre-loaded output. It controls the slew rate of the input voltage applied to the voltage regulator. It also keeps the input current within the limit when the voltage regulator has fault or over-load condition. When OV condition occurs on the voltage regulator output, the input control FET can be turned off to protect the output load.

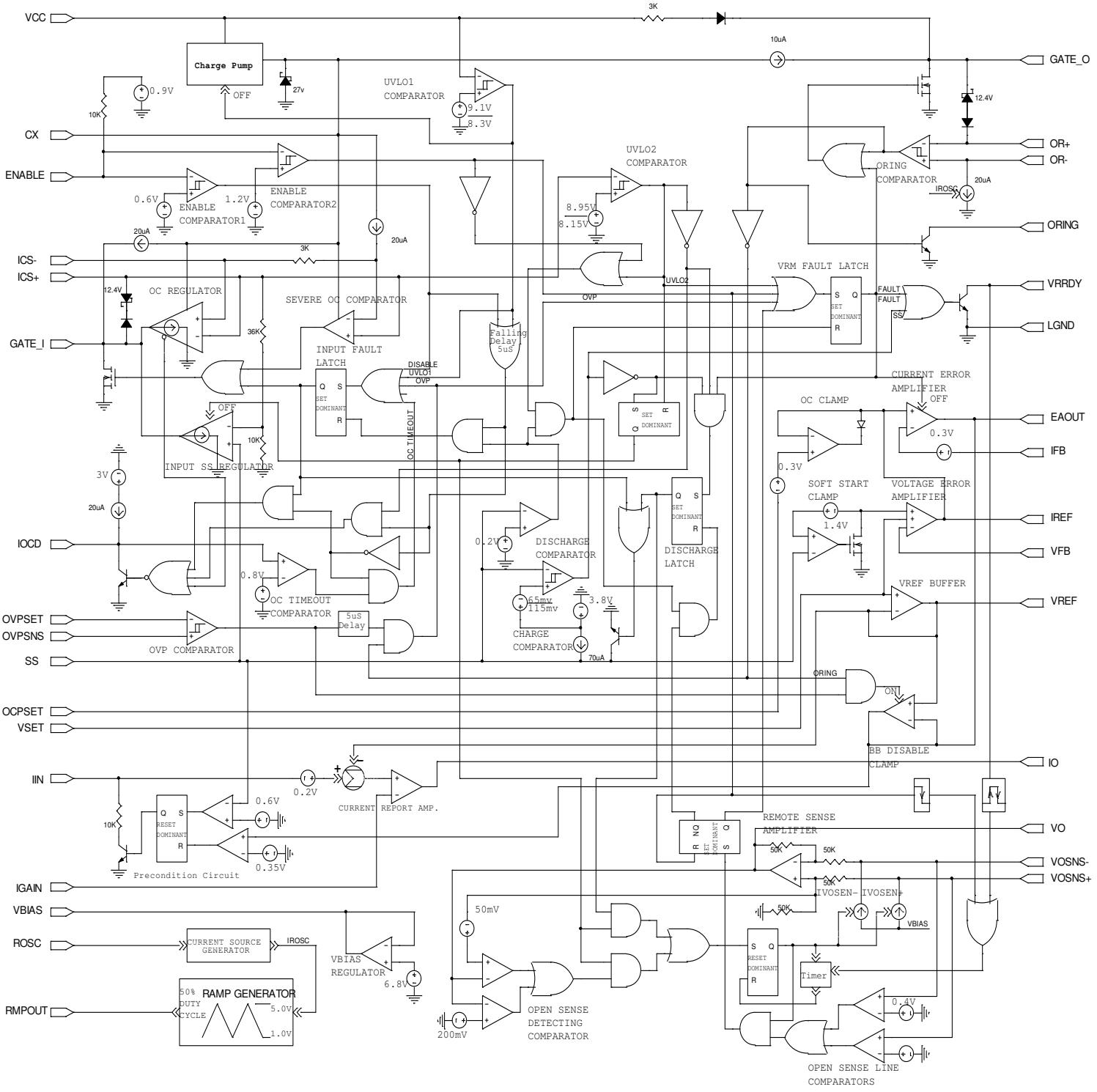
A current sense resistor in series with the input FET is used to sense the input current. Once the sense current exceeds the programmed OC threshold, the input control FET is controlled to run in linear mode to limit the current, so it has larger power loss and can't be running for a long period of time. A programmable time delay is normally implemented to prevent false trigger the input OCP and turns off the input control FET when it is time-out.

ORing Control for Redundant Applications

For redundant system application, multiple voltage regulators can be paralleled to provide fault-tolerant output voltage for critical load. ORing diode was used to isolate the fault module from the output, but its high power loss prevents it from being used in low voltage high current application. ORing FET is now commonly used in low voltage high current application, but its reverse conducting current needs to be limited. The reverse current can be caused by fault or the mismatch between two paralleled output voltages. Thus, the ORing FET control requires a reverse current comparator and fast turn-off gate driver.

The Rds(on) of Oring FET is normally used to sense the reverse current. To reduce the conductive power loss, low Rds(on) FET is preferred for Oring application. Also the reverse current needs to be limited no more than 10% of rated current, otherwise too much energy would be feedback to the input and may cause input OV. Thus, a very low offset reverse current comparator and fast turn-off Oring gate driver are required.

IR3510 BLOCK DIAGRAM



Note: **"Input Reset" = ($\overline{Enable} + \overline{Vcc}$) x Vss; "OC Timeout" =ICOD x Enable x Vcc**

IOCD = (Input Fault Latch x Enable x Vcc) + P12 x ($\overline{Enable} + \overline{Vcc}$)

Css Discharge = Input Fault Latch + Css Charged x VRM Fault Latch x $\overline{UVLO2}$

IR3510 THEORY OF OPERATION

Vbias Regulator

The Vbias regulator supplies a 6.8V/20mA bias voltage for internal circuitry, and through VBIAS pin it also provides reference voltage for Phase IC. Since the oscillator ramp amplitude tracks the VBIAS voltage, it should be used to program the Phase IC trip points to minimize phase delay errors.

The VBIAS can also be used as system reference voltage to set VSET, OCPSET and OVPSET voltage.

Charge Pump

The Charge Pump provides gate drive voltage for input soft-start FET and output ORing FET. A Tripler circuit is used to boost the VCC voltage to a high-level voltage in order to drive the input FET.

It has internal voltage clamp of 27V. It provides 20uA input FET charge current and 10uA Oring FET charge current. It also supplies the internal input OC comparator and OCP regulator.

An external cap of 0.1uF/50V voltage is required. Fig. 6 shows the charge pump voltage vs. Vcc.

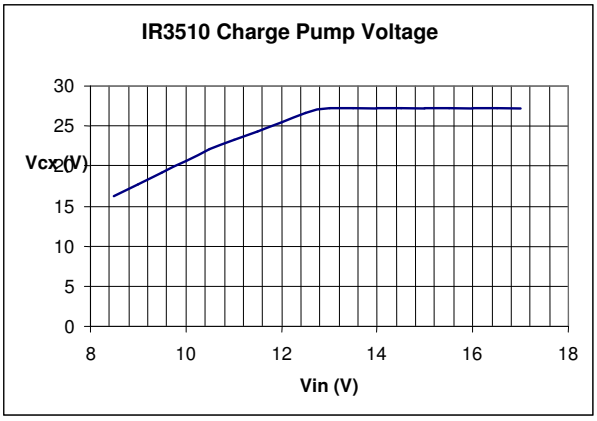


Fig. 6 Charge Pump Voltage

Input FET Soft-Start Regulator

The input FET soft-start regulator compares the voltage after the input FET and the voltage on the soft-start cap, which is externally connected on the “SS” pin, and then adjusts the input FET gate drive voltage to control the P12V, which is the voltage after the input FET, to follow the soft-start cap voltage and linearly increase until it reach the input voltage.

Since the input FET soft-start regulator can only sink current, it can only slow down the ramp of the input FET gate drive voltage. If the soft-start cap is too small, or the input FET gate capacitance is large enough, the P12V voltage may not be able to follow the soft-start cap.

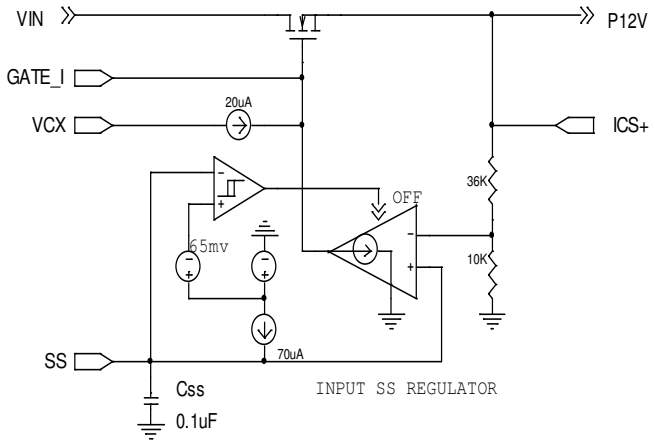


Fig. 7 Soft-Start Regulator

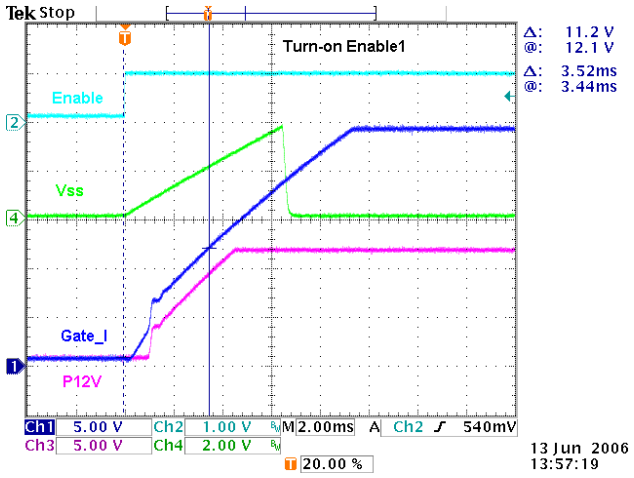


Fig. 8 Input FET Soft-Start

Input current limit

Input current limit is required for hot-swap application to eliminate the inrush current drawn from the VIN power supply. There are two stages of input current limit. The first stage is input current limit, in which the input FET runs into linear mode first to limit the input current, and it is then latched off after a programmable delay time. The second stage is the severe over current protection. The input FET is immediately turned off once the input current reaches the severe OCP threshold. Since it is not latched, once the current is reduced below the severe OCP threshold, the input FET runs into normal current limit mode and then latched off after time-out.

The input current is sensed by a sense resistor placed after and in series with the input FET. A 20uA current source going out of the "ICS-" pin flows through Rocset and sets the input current limit threshold.

Iocset = Rocset x 20uA / Rs

The severe OCP threshold voltage is 60mv above the normal current limit threshold, which gives,

Isevere = (Rocset x 20uA + 60mv) / Rs

The input OCP delay is set by an external cap connected on the "IOCD" pin. Once the input current limit threshold is reached, a 20uA current source going out of the "IOCD" pin charges the Cocd. The input FET is turned off once the "IOCD" is charged above 0.8V threshold voltage. The time-out delay is,

Tocd = Cocd x 0.8V / 20uA

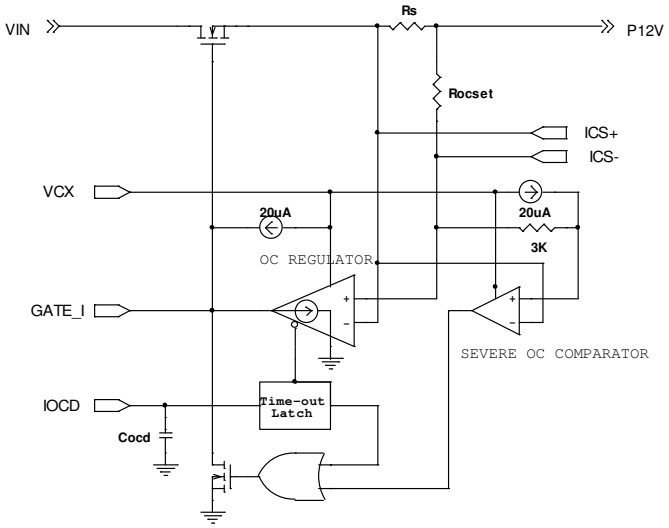


Fig. 8 Input OCP Control

Two-Level Enable Threshold Voltages

The IR3510 is designed for multiple outputs application, in which a common input FET is used. In order to turn on each output independently, two-level Enable threshold voltages are used. The first threshold voltage is 0.7v, and is used to turn on just the input FET; The second threshold is 1.2v, and is used to turn on the voltage regulator output.

The "Enable" pin has internal pull-up to 0.9V. If it is left open, it is above the first threshold, so it turns on the input FET. To turn on the voltage regulator output, a voltage higher than the second threshold voltage needs to be applied to the "Enable" pin.

Two-Stage Soft-Start

The IR3510 has a two-stage programmable soft-start to limit the surge current during both the input FET turn-on and the voltage regulator start-up. The soft-start capacitor connected between the "SS" and "LGND" pins controls soft start timing. A charge current of 70uA control the up slope of the voltage at the "SS" pin.

The first stage soft-start is controlled by the first enable threshold voltage. Once the Enable voltage is above its first threshold, the soft-start cap is charged up until it reaches its charge-up threshold voltage. During this soft-start time, the input FET is controlled by the input soft-start regulator and the voltage after the input FET ramps up following the soft-start cap voltage. If the Enable voltage is below the second enable threshold voltage, the SS voltage will be kept charged and complete the soft-start of the input FET.

If a voltage higher than the second enable threshold is applied to the Enable pin after the input FET is fully turned on, the soft-start cap is quickly discharged and then re-charged up by the same 70ua charging current to provide the soft-start for the voltage regulator output.

Figure 9 depicts the start-up sequence of the voltage regulator. If there is no fault, the SS pin will start charging when the enable crosses the threshold. The current error amplifier output EAOUT is clamped low until SS reaches 1.35V. The error amplifier will then regulate the voltage regulator's output voltage to match the SS voltage less the 1.35V offset until the output reaches the set voltage. The SS voltage continues to increase until it rises above 3.7V and allows the VRRDY signal to be asserted. SS finally settles at 3.8V, indicating the end of the soft start.

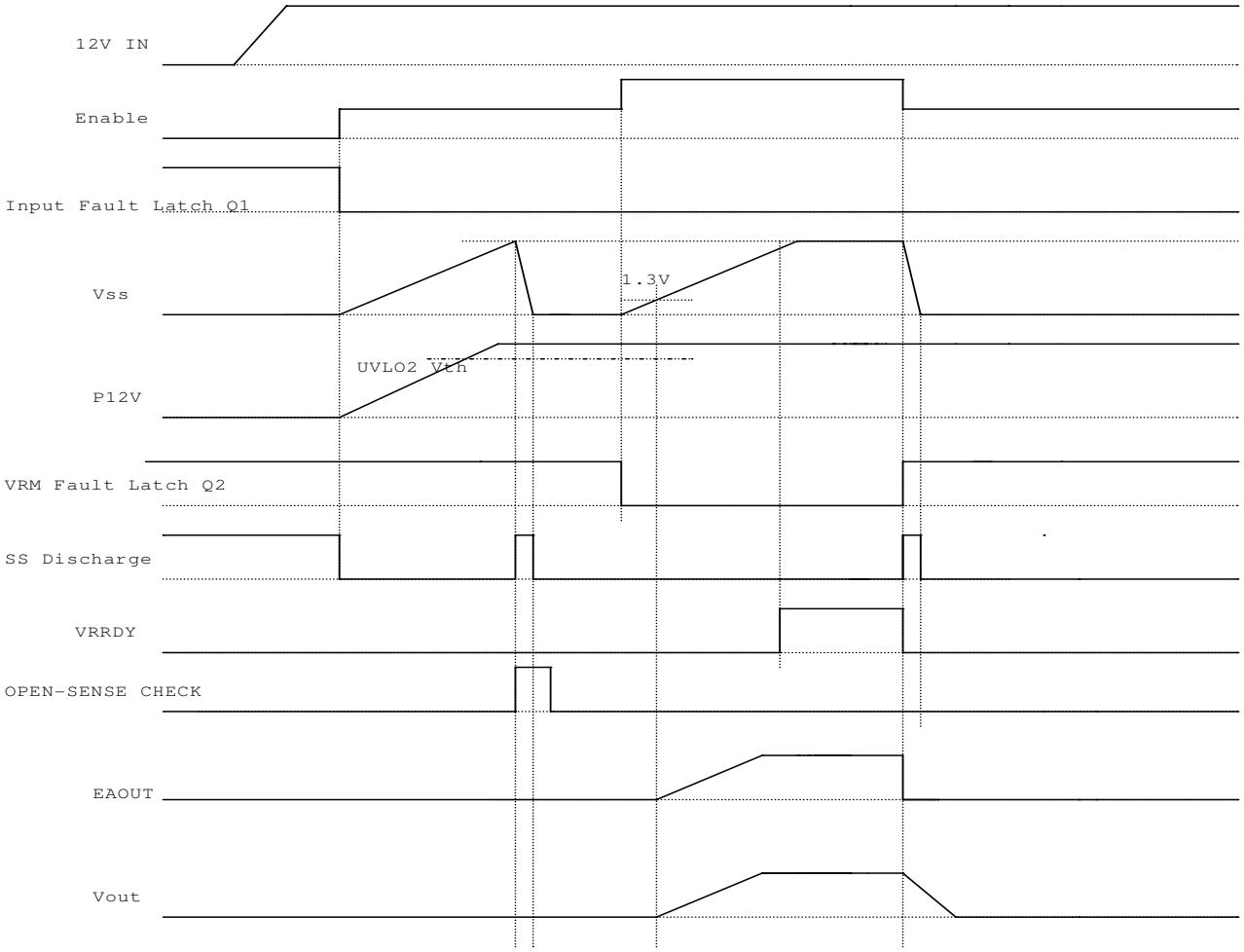


Figure 9 Start-up sequence of converter

If a higher than the second enable threshold voltage is applied to the "Enable" pin when the input FET is OFF, a consecutive two-stage soft-start cycle is started. The input FET is first turned on, and immediately follows the soft-start of the voltage regulator, as seen in the Fig.10 waveform.

If the P12V takes longer time to ramp up than the soft-start cap voltage in the first soft-start cycle, the soft-start cap will hold its charge until the P12V voltage ramps up across the UVLO threshold of P12V voltage, then it starts the 2nd soft-start cycle.

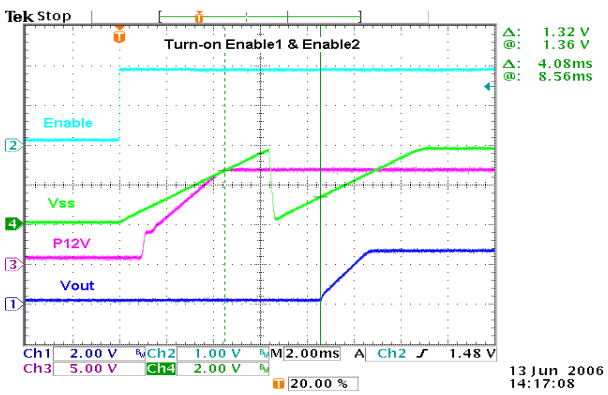


Fig. 10 Two-stage soft-start

VREF Buffer

The “VSET” pin inputs the VSET voltage from the system, and it is connected to the input of the VREF buffer. The buffered VSET voltage, VREF, is used as the reference voltage of the voltage error amplifier to control the voltage regulator output voltage. It’s is also used by the “Body Braking” comparator as a threshold voltage.

The VREF is one of the 5-wire buses connected to the phase IC. It is used as the offset voltage of the current sense signal IIN, and also the floor voltage of the PWM ramp.

Voltage Error Amplifier

The VRF reference voltage is connected to the non-inverting input of the voltage error amplifier. The soft-start clamping circuit is also connected to the non-inverting input to control the voltage EA output during soft-start.

Connected to the inverting input of the voltage error amplifier is the output feedback voltage, which comes directly from the remote voltage sense amplifier output or through a resistor divider.

Typical Type II or Type III can be used to compensate the voltage loop. The Rdroop is used to set the output voltage droop or the load line, the Rc and Cc is used to set the compensation zero, and Cp is used to set the high-frequency pole.

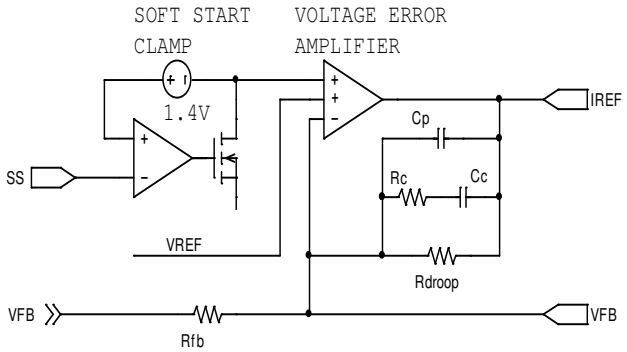


Fig. 11 Voltage Error Amplifier

Current Report Amplifier

Three-stage amplifiers are used to report the output load current through “IO” pin. The “IO” signal is also used to set the voltage droop and balance the current between voltage regulators. Since the current sense signal from the phase IC has an offset voltage of VREF, the first stage is a differential amplifier which subtracts the VREF voltage from the IIN signal. In order to measure the reverse current in a paralleled system, a 200mv fixed offset voltage is added to the current sense signal in a second-stage amplifier. A non-inverting third-stage amplifier with external gain setting resistors is used to program its output voltage to be proportional to the output load current.

A NTC thermistor is normally required to compensate the TC effect of the inductor DCR current sensing. Fig.12 shows the current report amplifiers and its typical thermal compensation circuit.

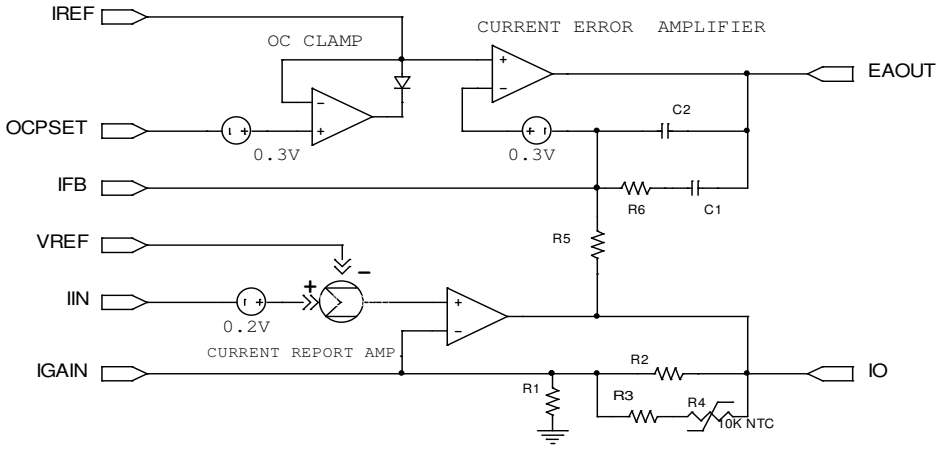


Fig. 12 Current Report with Thermal Compensation and Current Error Amplifier

Current Error Amplifier

The voltage error amplifier output, IREF, is connected to the non-inverting input of the current error amplifier. The current report output, IO, is connected to the "IFB" pin through a feedback resistor, and then connected to the inverting input of the current error amplifier.

The voltage error amplifier has minimum output voltage since it is powered from a single power supply. In order to keep the current error amplifier under control at no-load condition, a 300mv offset is added to the current feedback input of the current error amplifier, as seen in Fig. 12.

Constant Current Limit

Constant current limit function is required for paralleled redundant system. With average current mode control, the constant current limit can be easily implemented by clamping the current reference signal, which is the output of voltage error amplifier and also the non-inverting input of the current error amplifier.

An OC clamping amplifier is used to buffer the "OCPSET" voltage from the system. Its output is connected together with the current reference signal, so it clamps the current reference voltage to be no more than the "OCPSET" voltage. To compensate the 300mv offset voltage in the current feedback signal, a same 300mv offset voltage is added to the OC clamp amplifier input.

Remote Voltage Sense Amplifier

VOSEN+ and VOSEN- are used for remote sensing and connected directly to the load. The remote sense differential amplifier with high speed, low input offset and low input bias current ensures accurate voltage sensing and fast transient response.

Since the remote voltage sense amplifier has limited input impedance, any impedance in series with the remote sense lines will affect the voltage sense accuracy. If a voltage feedback divider is needed to match the VSET voltage, it's better to place the voltage divider at the remote sense amplifier output, that is, "VO" pin.

ORing Comparator and Oring FET Driver

The Oring comparator monitors the voltage across the Oring FET, which is produced by the current going through the Rds(on) of the Oring FET.

Oring FET is turned once it develops positive voltage from SOURCE to DRAIN. Since the Oring FET gate charge current from the Charge Pump is only 10uA, it takes some time to fully turn on the Oring FET. An internal 3K pull-up resistor is connected from "GATE_O" to Vcc to speed up the Oring FET turn-on.

When a negative voltage is detected and it is exceed the threshold voltage set by the programming resistor in series with the "OR-" pin, the "GATE_O" is quickly pulled down with 2A peak discharge current.

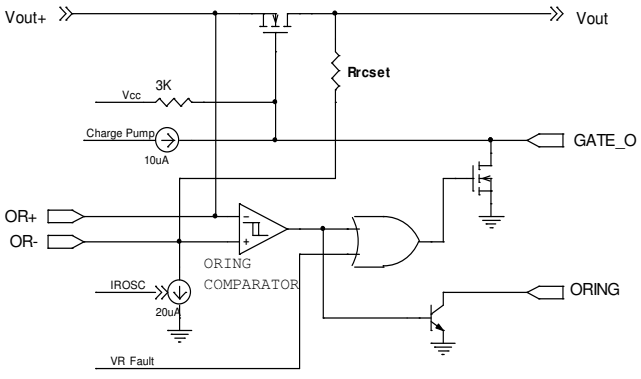


Fig. 13 Oring Comparator

A 30mv hesteresis is added to the Oring comparator to prevent it from chattering and ensure it is only turned off with negative input. The current source flowing into the "IR-" pin, which is used to program the reverse current cut-off threshold through an external resistor, is determined by the switching frequency in order to achieve good accuracy. It increases with the switching frequency.

An open-collector output "ORING" signal indicates the Oring FET status. HIGH means the Oring FET has positive load current, and LOW means the Oring FET is OFF or carrying negative current.

Under Voltage Lock Out

There are two UVLOs, UVLO1 for Vcc and UVLO2 for P12V which is the voltage after the input FET. The UVLO1 for Vcc has the start threshold of 9V and stop threshold of 8.2V. It controls the Charge Pump, the enable of the input FET, and the reset of the input fault latch. Any fault latch can be reset by cycling either Enable or Vcc.

The UVLO2 for P12V has the start threshold of 8.9V and the stop threshold of 8.1V. The UVLO2 threshold tracks the UVLO1 threshold to make sure the input FET is turned on without larger voltage droop across the input FET. The UVLO2 controls the input soft-start regulator, second soft-start cycle, and the turn-on of the voltage regulator output.

Input FET Short Detection

Detecting a failed input FET is critical for hot-swap and OVP. But, it's hard to detect when it is turned on, since its failure mode is shorted. A logic circuit is added to detect the P12V voltage before enabling the input FET. If it's above the UVLO2 threshold before the input FET is turned on, it declares the input FET shorted and latches the fault.

Over-Voltage Protection

The OVP comparator compares the voltage on the "OVPSET" pin and the voltage on the "OVPSNS" pin. The "OVPSET" voltage from the system sets the threshold of the OVP. The "OVPSNS" voltage is directly from the remote sense amplifier output "VO", or through a resistor divider to match the "OVPSET" voltage.

Once the OV condition is detected, it turns on the "Body-Braking Disable" circuit first to turn on all the bottom FETs. After 5uS delay, it turns off the input FET and latches the fault.

In a redundant system, the OV condition can be caused by any of the paralleled voltage regulators. In order to isolate the bad module but still keep the system running, "ORING" signal is used to determine which module is causing the OV, since only the bad module is having HIGH "ORING" signal. So, only the bad module will be disabled and latched off. All the good modules will resume supplying the load once the bad module is isolated and the OV condition is removed.

Fig. 14a shows the OVP response in a bad module, and Fig. 14b shows the OVP response in a good module.

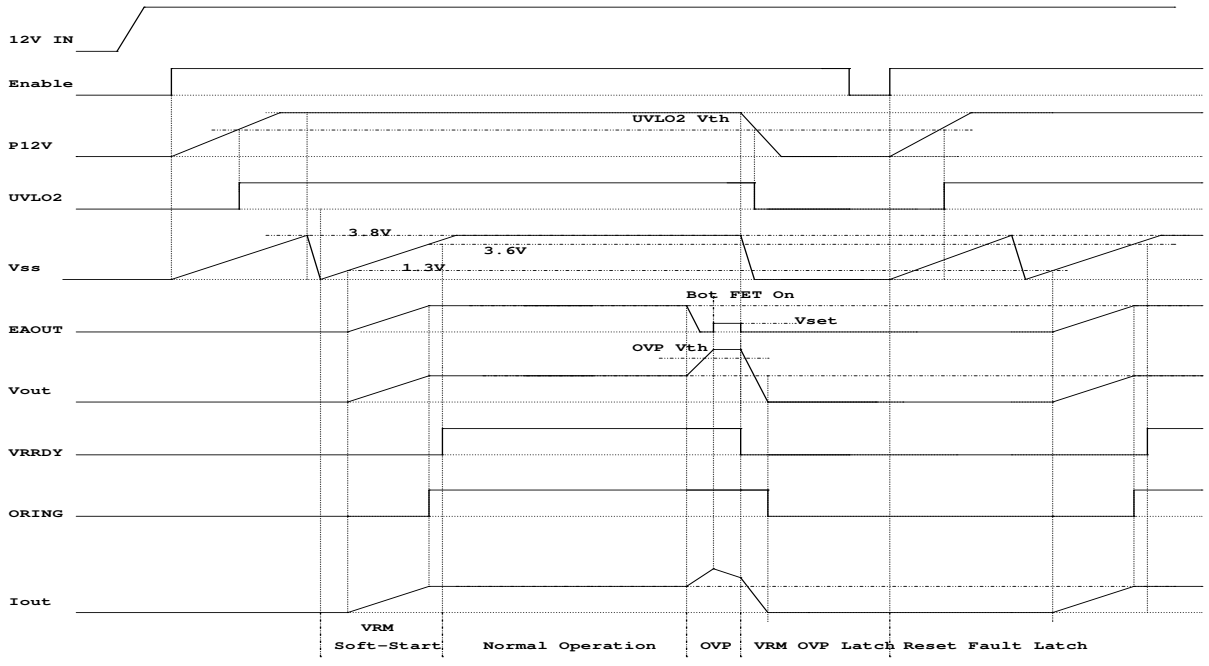


Fig. 14a Bad module OVP response

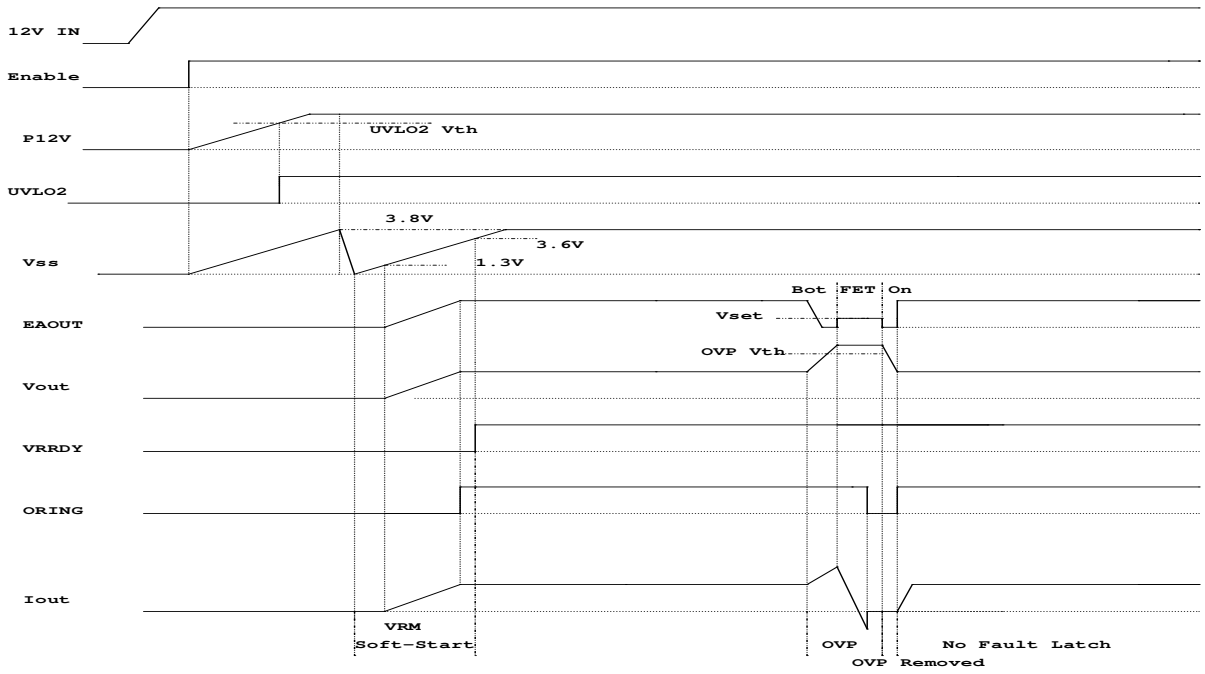


Fig. 14b Good module OVP response

Open Remote Sense Line Protection

If either remote sense line VOSEN+ or VOSEN- or both are open, the output of remote sense amplifier (VO) drops. The open-sense comparator monitors VO pin voltage continuously. If VO voltage is lower than 200 mV, two separate pulse currents are applied to VOSEN+ and VOSEN- pins respectively to check if the sense lines are open. If VOSEN+ is open, a voltage higher than 90% of VBIAS will be present at VOSEN+ pin and the output of open line detect comparator will be high. If VOSEN- is open, a voltage higher than 700mV will be present at VOSEN- pin and the output of open-line-detect comparator will be high. The open sense line fault latch is set, which pulls error amplifier output low immediately and shut down the voltage regulator.

The open sense protection circuit has limited current source, it may not be high enough to charge the open sense line up to the threshold voltage if there is a differential or common mode cap on these two remote sense lines. In this case, an alternative external open-sense protection circuit may be needed.

IR3510 DESIGN PROCEDURES

Application Circuit

Fig. 15 shows an application circuit with 4 phases using IR3088A as phase IC. Although It is not necessary to use one ORing FET for each phase, it is recommended to do so to improve the efficiency and have better layout.

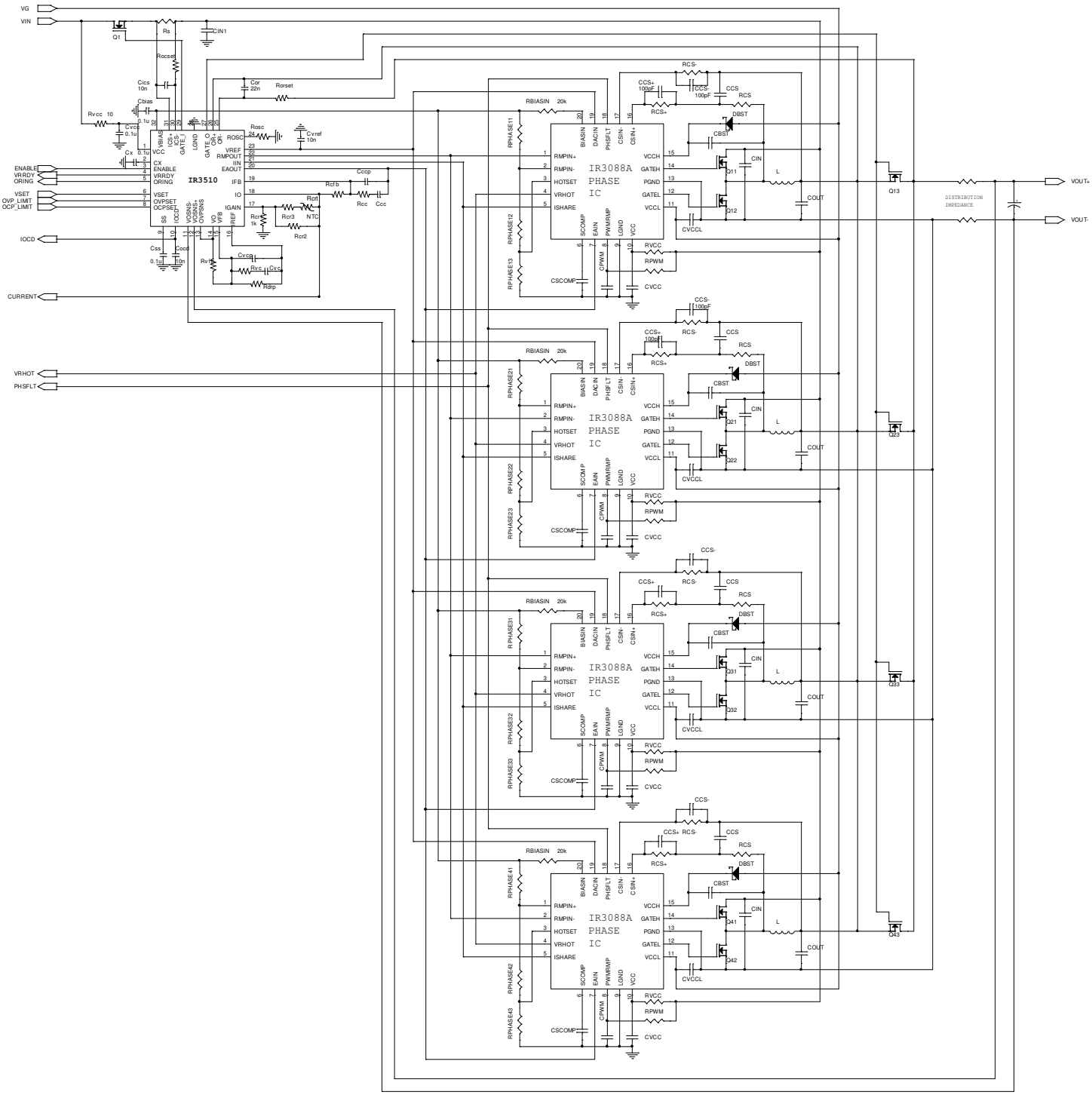


Fig. 15 4-phase IR3510 Application Circuit

VCC,CX and VBIAS Caps

Both VCC and VBIAS require a 0.1 uF 16V 0603 cap. For Charge Pump output cap CX, a 0.1uF 50V 0603 cap is needed since the charge pump voltage can be up to 27V.

Oscillator Resistor *Rosc*

The oscillator of IR3510 generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase equals the oscillator frequency, which is set by the external resistor ROSC according to the curve in Fig. 16.

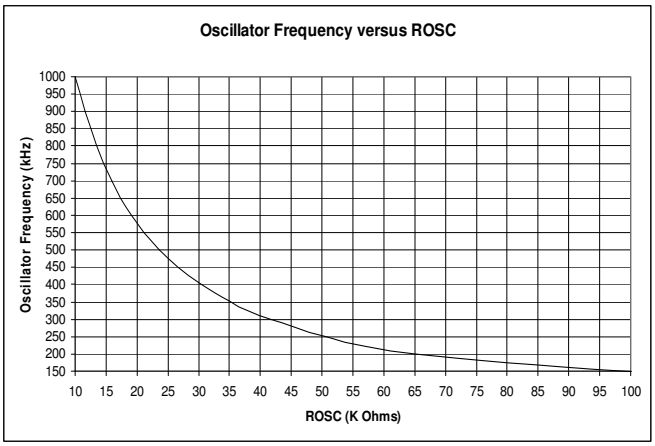


Fig. 16 Switching frequency Vs. Rosc

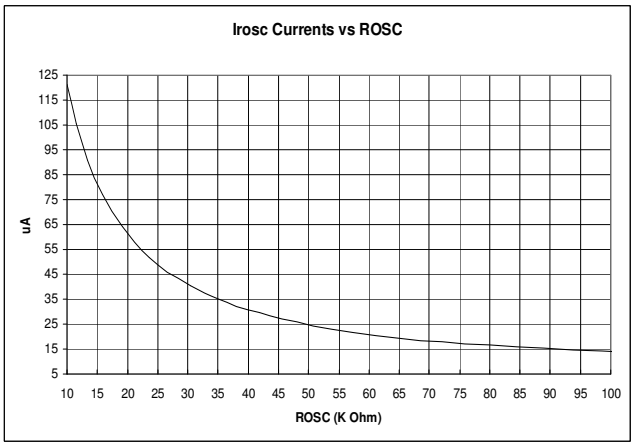


Fig. 17 Irosc Current Vs. Rosc

Soft Start Capacitor *Css*

The soft start capacitor CSS programs the soft start time for both the voltage regulator input voltage, which is the voltage after the input FET, and the converter output voltage. An internal 70uA current source charges the soft-start cap until it reaches the final charge-up voltage, which is typical 3.8V. It sets the input voltage ramp-up time, the output delay time, the output voltage ramp-up time and the VRRDY delay time.

The input voltage ramp-up time is determined by the input soft-start regulator gain Kss, which is typical 4.5, Vin and the input voltage applied before the input FET. Assume the input FET gate charge is small enough, so the gate voltage can follow the soft-start cap voltage,

$$Tir = \frac{C_{SS} * Vin}{I_{CHG} * Kss} = \frac{C_{SS} * 12}{70 * 10^{-6} * 4.5}$$

If the input FET has large gate charge or more than one input FETs are paralleled, the gate charge current may not be large enough to keep the voltage following the soft-start cap voltage, resulting in longer ramp-up time.

There is a delay time added in the soft-start of the converter output. The voltage error amplifier output is held LOW until the soft-start cap reaches 1.35v, resulting in the delay time.

$$Tod = \frac{C_{SS} * 1.35}{I_{CHG}} = \frac{C_{SS} * 1.35}{70 * 10^{-6}}$$

After the soft-start cap voltage moves above 1.35V, the voltage error amplifier is released and the feedback voltage VFB follows the soft-start cap voltage until it reaches the VSET voltage. Assuming the final VFB is less than the soft-start charge-up voltage, the converter output voltage ramp-up time is,

$$Tor = \frac{C_{SS} * (VFB - 1.35)}{I_{CHG}} = \frac{C_{SS} * (VFB - 1.35)}{70 * 10^{-6}}$$

The VRRDY goes HIGH when the soft-start cap voltage reaches the charge-up comparator threshold, which is 3.7V. The total soft-start time from Enable going HIGH to VRRDY going HIGH is determined by,

$$Tos = \frac{C_{SS} * 3.7}{I_{CHG}} = \frac{C_{SS} * 3.7}{70 * 10^{-6}}$$

The soft-start cap can be selected by one of the above equation based on which soft-start time needs to be met.

Input OCP setting resistor

The input current is sensed by a sense resistor placed after and in series with the input FET. The input OCP setting resistor is connected between the downstream of the input sense resistor and the "ICS-" pin. A typical 22uA current source flowing out of the "ICS-" pin goes through Rocset and sets the input current limit threshold voltage.

$$Iocset = \frac{Rocset * 22 * 10^{-6}}{Rs}$$

The severe OCP threshold voltage is 60mv more than the normal current limit threshold, which gives,

$$Isevere = \frac{Rocset * 22 * 10^{-6} + 60 * 10^{-3}}{Rs}$$

A 10nF cap Cics is recommended between "ICS+" and "ICS-" pins and placed close to the IC.

IOCD Cap

The IOCD cap programs the input OCP time-out delay. When the sensed input current reaches the input OCP threshold, the internal 20uA current source starts charging the IOCD cap, and once the IOCD cap voltage is charged above 0.85V, which is the time-out comparator threshold, the input FET is latch OFF.

The time-out delay time can be calculated as,

$$Tocd = \frac{C_{iocd} * 0.85}{I_{CHG}} = \frac{C_{iocd} * 0.85}{20 * 10^{-6}}$$

Current Error Amplifier Compensation

Average current mode control is used to implement the constant current limit function and keep good current sharing between modules. One added benefit of using current mode control is that it can eliminate the output inductor from the voltage loop and make the voltage loop compensation much simple.

The inputs to the current error amplifier are the voltage error amplifier output, which serves as the current reference signal, and the inductor current sense feedback signal. The open current loop gain is determined by the PWM gain for the power stage, the output inductor, the output cap and the load resistor. The open current loop has one output zero made by the output cap and the load resistor, and the L-C double-pole. The output zero frequency is usually smaller than the L-C resonant frequency Fo, which means the current loop can have enough phase margin.

In order to eliminate the inductor from the voltage loop, the current loop cross-over frequency needs to be much higher than the L-C resonant frequency. Meanwhile, it has to be less than 1/5 of the switching frequency. So, the current loop cross-over frequency can be placed between 3Fo and 1/5Fs.

Typical Type II compensation can be used with the compensation zero placed at the L-C double pole frequency and high frequency pole placed near the switching frequency. The cross-over frequency determines the middle frequency gain.

Assuming Lo is the equivalent output inductance for multiple phases, Rpwm and Cpwm set the PWM RAMP with the phase IC, Fs is the switching frequency, Ki is the current feedback gain which is defined by Vimax/Iomax, select the current EA compensation gain at the cross-over frequency to be,

$$Kci = \frac{2\pi * Lo * Fci}{Gpwm * Ki}$$

where, Fci is the target current loop cross-over frequency
Gpwm is the PWM gain of the power stage, Gpwm = Rpwm*Cpwm*Fs

Select Rcfb = 1K, then, Rcc = Kci (K Ohm)

Ccc = 1/ (2π*Rcc*Fo)

Ccp = 1/ (2π*Rcc*Fs)

Voltage Error Amplifier Compensation and Vdroop setting

The inner current loop removes the output inductor from the voltage loop, so the open voltage loop has only one pole, which is made by the output cap and load resistor, up to the current loop cross-over frequency. To avoid the interference between the outer voltage loop and the inner current loop, the voltage loop cross-over frequency should be placed at least 10KHz below the current loop cross-over frequency.

Typical type II compensation can be used with the compensation zero placed at the output pole and the high-frequency pole placed at the ESR zero of the output cap. The compensation middle-frequency gain determines the voltage loop cross-over frequency. It can be calculated as follows,

$$Kcv = \frac{2\pi * Co * Ki * Fcv}{Kv}$$

where, Fcv is the target voltage loop cross-over frequency
Kv is the voltage feedback gain. Without feedback resistor divider, It's a unity gain.

Select Rvfb = 1K, then, Rvc = Kcv (K Ohm)

Cvc = 1/ (2π*Rvc*Fo)

Cvcp = 1/ (2π*Rvc*Fesr)

The Type III compensation is only needed if the voltage loop cross-over frequency has to be greater than the current loop cross-over frequency in some applications. It can improve the phase margin.

The voltage droop is determined by the voltage error amplifier compensation DC gain, which is set by the feedback resistor Rdrp across the voltage error amplifier. Rdrp can be calculated as follows,

$$Rdrp = \frac{Ki * Io\max * Rfb}{Vdrp}$$

where, Iomax is the rated maximum output current
Rfb is the resistor connected to the inverting input of the voltage error amplifier
Vdrp is the required droop voltage at rated maximum output current.

Current Report Gain and Thermal Compensation

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/℃, and therefore the maximum inductor DCR can be calculated,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})]$$

Where, R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature T_{L_MAX} and room temperature $T_{\_ROOM}$.

The total input offset voltage (V_{CS_TOFST}) of current sense amplifier in the phase ICs is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor R_{CS}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS}$$

The current sense signal IIN received from phase IC is determined by,

$$IIN = Vref + [\frac{Io\max}{N} * R_{L\_MAX} + V_{CS\_TOFST}] * G_{CS}$$

Where,

Iomax = Maximum load current
N = Number of phases
G_{CS} = Gain of the current sense amplifier

The current report signal Io is determined by,

$$Io = \{[\frac{Io\ \max}{n} * R_{L\_MAX} + V_{CS\_TOFST}] * G_{CS} + 0.2\} * (1 + Rcr\ 2 / Rcr\ 1)$$

Where, the 0.2V offset voltage is added inside the IR3510 so it can measure the reverse current
Rcr1 is the resistor connected from "IGAIN" pin to GND.
Rcr2 is the external equivalent resistance between "IGAIN" pin and "IO" pin, which includes the thermal compensation network.

Rcr3 in series with Rcrt which is a NTC provides thermal compensation to cancel the TC effect of the inductor DCR. Place the NTC close to the output inductor of the center phase.

Oring Reverse Current Cut-Off Threshold setting resistor

The Oring FET reverse current is sensed by the Rds(on) of the Oring FET. The reverse current cut-off threshold programming resistor Rorset is connected between the Drain pin of the Oring FET and the "OR-" pin. A constant current source Iorset flowing out of the "OR--" pin goes through Rorset and sets the reverse current cut-off threshold voltage.

$$Rorset = \frac{Ior\max * Rds(on)}{Iorset}$$

Where, Iormax is the max. allowed reverse current which is normally 10% or less of the rated output current.

The constant current source Iorset is the same as Irosc which is determined by the switching frequency. Fig17. 15 shows the Irosc changing with the Rosc.

A 10nF-22nF cap Cor is recommended between “OR+” and “OR-“ pins and placed close to the IC.

IR3088A Phase IC Componets

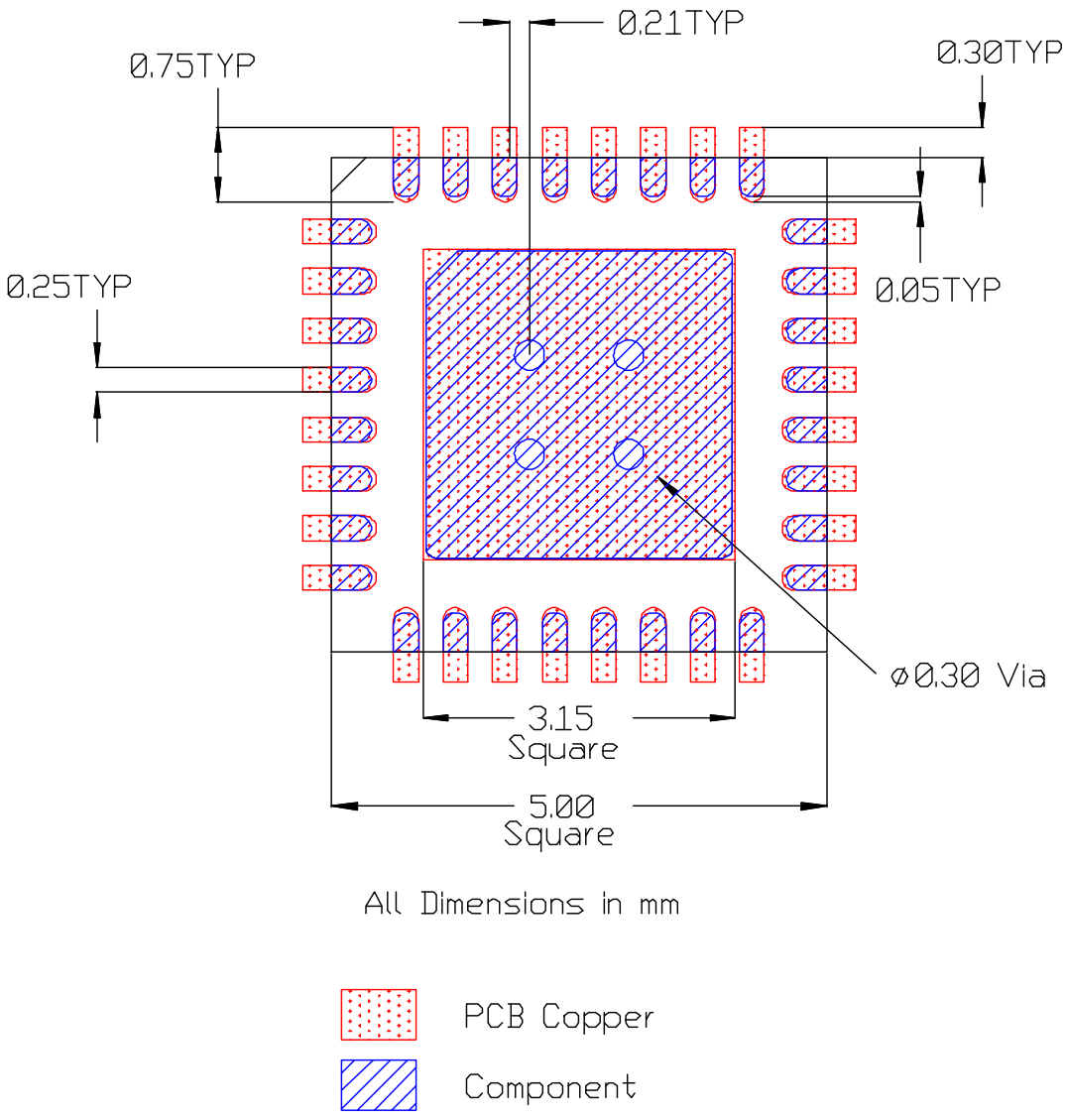
Please refer to IR3088A datasheet to select the values for the components around the phase ICs.

Rcs+ and Ccs+ are the two extra components needed for Oring application. Rcs+ is needed to prevent current sense amplifier output from saturation due to a potential negative voltage swing on the output terminal of the inductor, which can be caused by the turn-off of the Oring FETs. Ccs+ can be 100pF to eliminate high frequency noise from current sense input.

In order to balance the offset voltage caused by the input bias current, select Rcs- to be the sum of Rcs+ and Rcs.

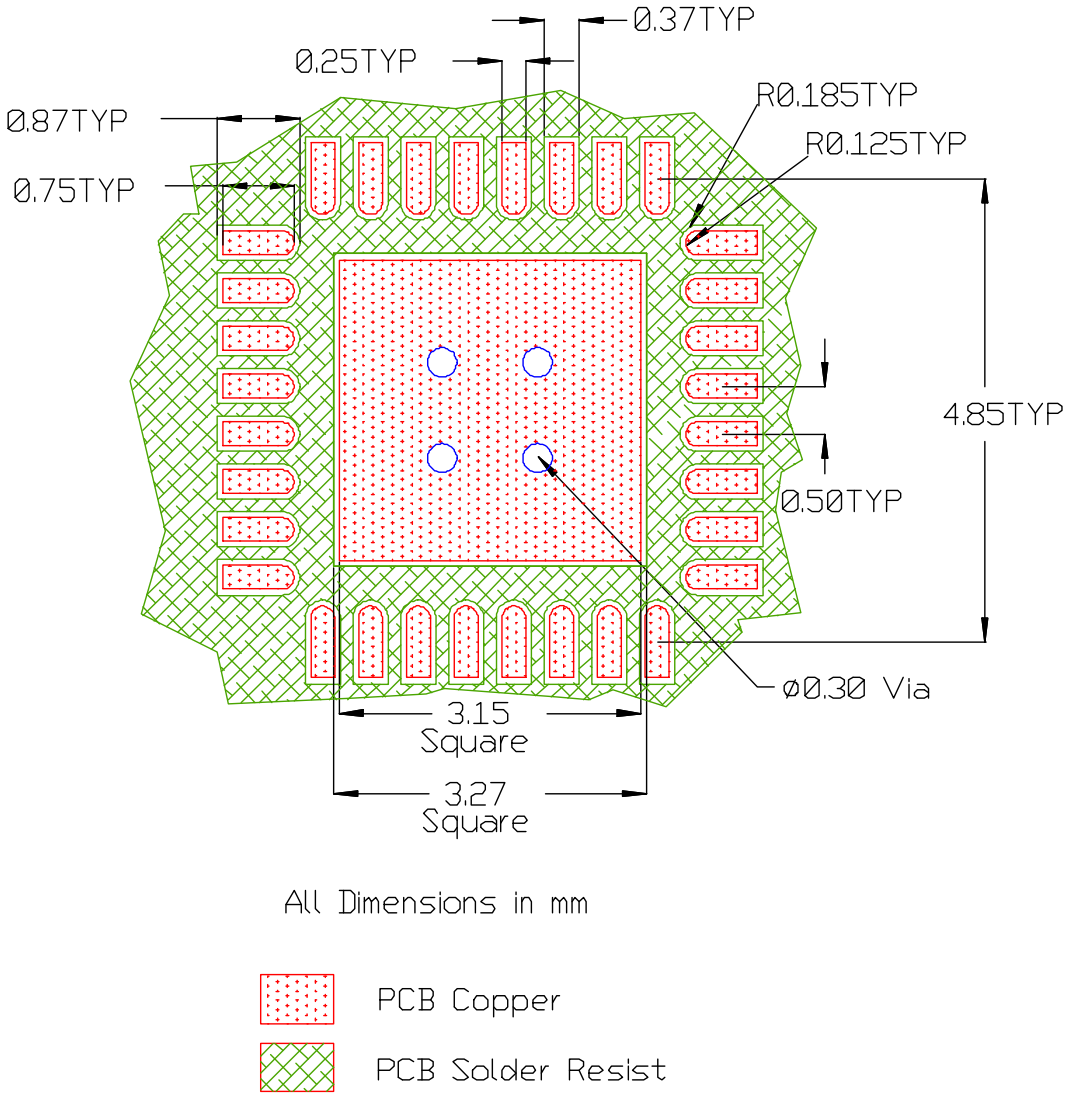
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.3mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



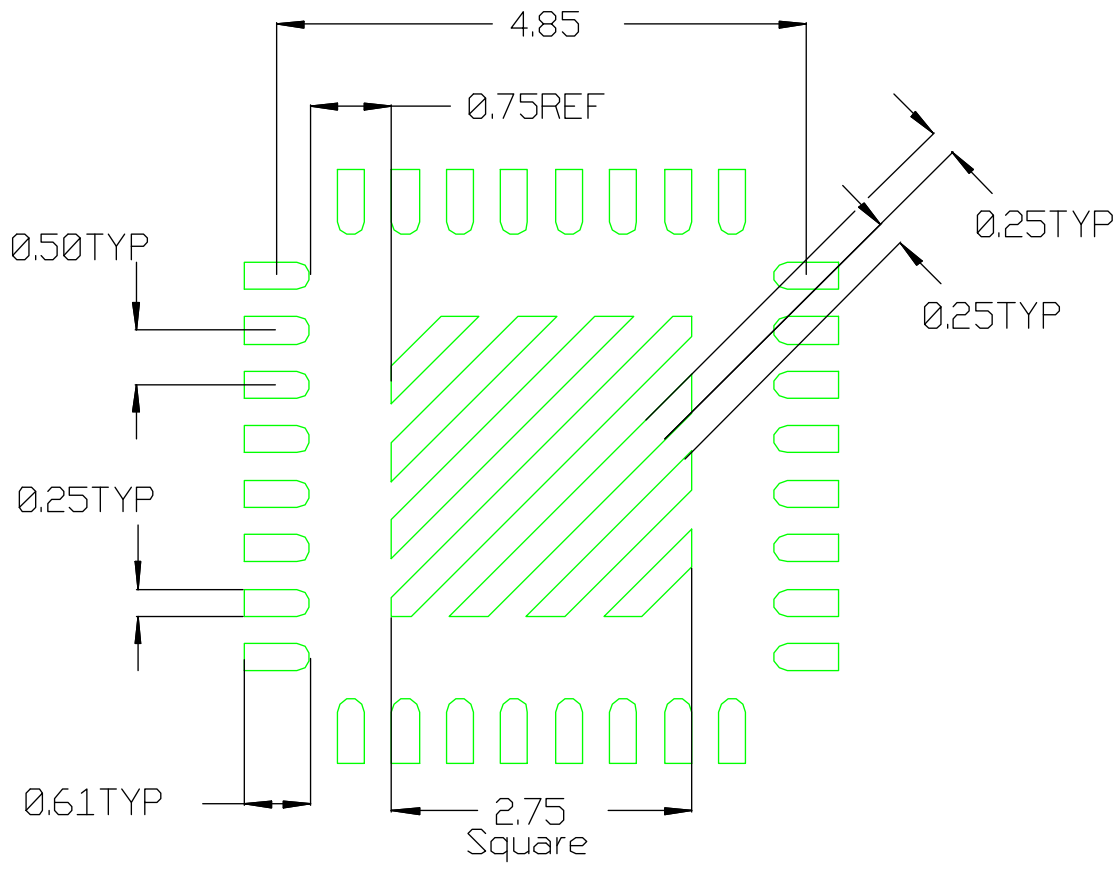
SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The four vias in the land pad should be tented or plugged from bottom board side with solder resist.



STENCIL DESIGN

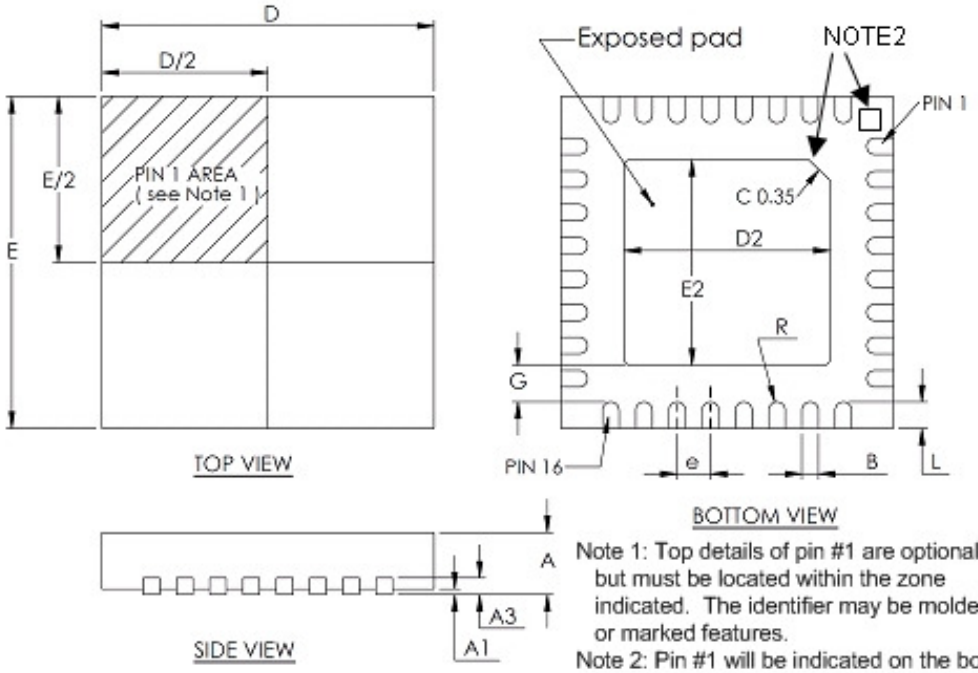
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) – θ_{JA} = 24.4°C/W, θ_{JC} =0.86 °C/W



Note 1: Top details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

Note 2: Pin #1 will be indicated on the bottom by either a chamfer or a square island.

32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

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