MAS7838

SYNCHRONOUS TO ASYNCHRONOUS CONVERTER SAC CMOS

- **Interfaces a duplex asynchronous channel to a synchronous channel**
- **Modem systems at speeds of 600, 1.2k, 2.4k, 4.8k, 9.6k and 19.2k**
- **Character length from 8 to 11 bits including start stop and parity bits**

DESCRIPTION

The MAS7838 is a single chip duplex synchronous to asynchronous converter. It converts asynchronous start stop characters to synchronous character format, with stop bit deletion when required as defined in the CCITT recommendation V.14 (V.22). On the receiver channel the MAS7838 converts the incoming synchronous data to asynchronous start stop character format with stop bit insertion when required as defined in the CCITT recommendation V.14 (V.22).The MAS7838 implements the data modes for the synchronous interface as specified in the V.14 (V.22). The device can be configured to operate at any frequency to maximum device speed within the above mentioned modes.
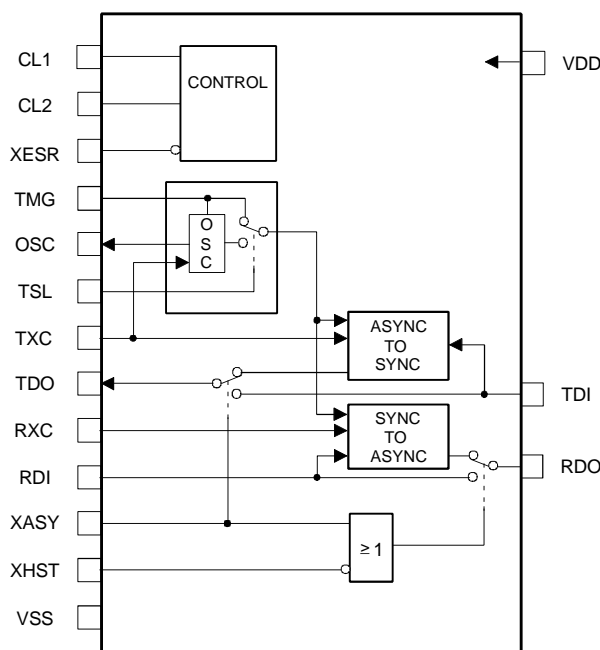
FEATURES

- Implements CCITT recommendations V.14 and V.22 chapters 4.1, 4.2 and 4.3
- Operates in modes as defined in the CCITT recommendations V.22 (i), ii), iii), iv) and v)
- Transmission rate up to 64 kbit/s
- CMOS compatible interface
- Low power consumption (typically 25 mW)
- No additional circuitry required to perform the conversion
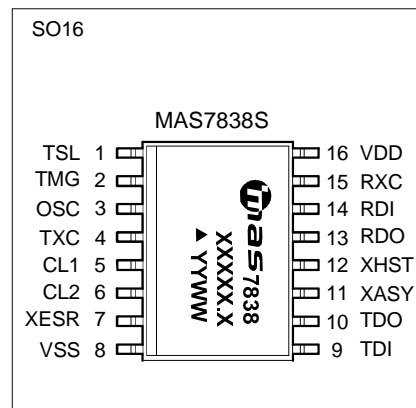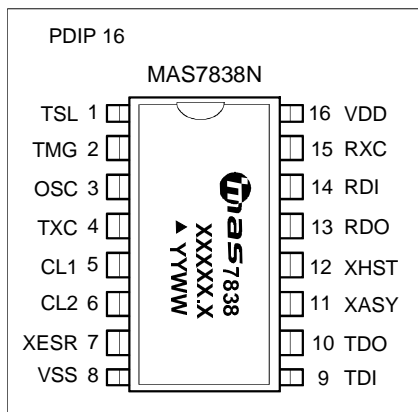- CMOS device
- Single =5V supply

APPLICATION

- Adapts asynchronous terminals to synchronous modems
- Full or half card PC modems using UART as a data source
- Simplifying data multiplexing in a MUX/DEMUX system

BLOCK DIAGRAM

PIN CONFIGURATION

PDIP 16

MAS7838N

```
TSL  1 ▯        ▯ 16  VDD
TMG  2 ▯        ▯ 15  RXC
OSC  3 ▯        ▯ 14  RDI
TXC  4 ▯        ▯ 13  RDO
CL1  5 ▯        ▯ 12  XHST
CL2  6 ▯        ▯ 11  XASY
XESR 7 ▯        ▯ 10  TDO
VSS  8 ▯        ▯  9  TDI
```

SO16

MAS7838S

```
TSL  1 ▯        ▯ 16  VDD
TMG  2 ▯        ▯ 15  RXC
OSC  3 ▯        ▯ 14  RDI
TXC  4 ▯        ▯ 13  RDO
CL1  5 ▯        ▯ 12  XHST
CL2  6 ▯        ▯ 11  XASY
XESR 7 ▯        ▯ 10  TDO
VSS  8 ▯        ▯  9  TDI
```

Top marking: YYWW = Year Week, XXXXX.X = Lot Number, ▲ =ESD Indicator

PIN DESCRIPTION

Pin name	Pin no.	I/O	Function
TSL	1	I	Timing select. 0 selects asynchronous sampling timing 16 x TXC from pin 2, TMG. 1 selects asynchronous sampling timing 256...8192 x TXC from pin 2, TMG.
TMG	2	I	Timing. Square wave timing signal 16 x TXC (TSL=0) or 256...8192 x TXC (TSL=1). Max f=10 MHz.
OSC	3	O	Oscillator. Output for crystal. If used, the crystal is connected between pins 2 and 3.
TXC	4	I	Transmitter timing. Synchronous square wave timing for transmitter. The transmitted data output, TDO is synchronized to the rising edge of TXC. The duty cycle of TXC has to be 50% +/- 5%.
CL1	5	I	Character length. The total character length including one start bit, one stop bit and
CL2	6	I	possible parity bit is selected with the CL1 and CL2 signals.
XESR	7	I	Extended signalling rate. The tolerance of the synchronous bit rate can be: XESR = 1 (basic signalling rate) TXC -2.5%...+1.0% XESR = 0 (extended signalling rate) TXC -2.5%...2.3%
VSS	8	G	Ground
TDI	9	I	Transmitter data input. 1 = mark or stop bit, 0 = space, start or break signal
TDO	10	O	Transmitter data output. The output data is synchronized to the synchronous timing signal TXC (pin 4). 1 = mark, 0 = space
XASY	11	I	Asynchronous mode. XASY=0 Asynchronous transmission. XASY=1 Synchronous transmission. In synchronous transmission the converter is totally bypassed in both directions: TDI=TDO, RDI=RDO
XHST	12	I	Higher speed signalling timing. XHST = 1 normal synchronous to asynchronous conversion (Bell 212; CCITT V.22). XHST = 0 asynchronous to synchronous conversion with higher speed synchronous timing (TXC, RXC). TXC and RXC timing must be 1-2% higher than the normal bit rate in order to allow some overspeed in the asynchronous data. On the receiver side the RX buffer is deleted and the synchronous data RDI is directly connected to the asynchronous output RDO.
RDO	13	O	Receiver data output. RDO is the received data converted back to asynchronous mode. 1 = mark or stop bit, 0 = space, start or break signal
RDI	14	I	Receiver data input. 1 = mark, 0 = space. The received data must be synchronized to the receiver timing RXC from the synchronous channel (pin 15).
RXC	15	I	Receiver timing. Receiver square wave timing from the synchronous channel. The received data RDI must be synchronized to the rising edge of RXC.
VDD	16	P	Power supply

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ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VDD		-0.5	5.5	V
Storage Temperature	Ts		-55	+150	^{o}C

RECOMMEDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		4.75	5	5.25	V
Supply Current	IDD			4	6	mA
Operating Temperature	Ta		0		+70	^{o}C

ELECTRICAL CHARACTERISTICS

◆ Inputs

(test conditions: VDD = +5V, VSS = 0V, 0°C to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}		3.5			V
Input low voltage	V_{IL}				1.1	V
Input leakage current	I_{IL}			-100		pA
Input capacitance load	C_I			5		pF
Internal pull-up resistor for digital inputs	$R_{pull-up}$	VIN = 0.4v VIN = 2.5v		350 850		kΩ

◆ Outputs

(test conditions: VDD = +5V, VSS = 0V, 0°C to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output low voltage	V_{OL}	IOL = -0.6mA			0.4	V
Output high voltage	V_{OH}	IOH = 0.4mA	4.6			V

◆ Data Timing

(test conditions: VDD = +5V, VSS = 0V, 0°C to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low to high logic transition time	tR	CL = 10pF		20		ns
High to low logic transition time	tF	CL = 10pF		20		ns

(test conditions: TSL = 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TDO delay time after TXC	T1		50		$T_{TXC}/16+350$	ns
RDI set up time before RXC	T2		1/4 T_{RXC}			ns
RDI hold time after RXC	T3		1/4 T_{RXC}			ns

(test conditions: TSL = 0, TMG = 16xTXC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TDO delay time after TXC	T1		50		1/TMG+350	ns
RDI set up time before RXC	T2		1/4 T_{RXC}			ns
RDI hold time after RXC	T3		1/4 T_{RXC}			ns

ELECTRICAL CHARACTERISTICS

Timings between synchronous clocks and data are shown below. Note that absolute delays depend on the speed of the data transmission.
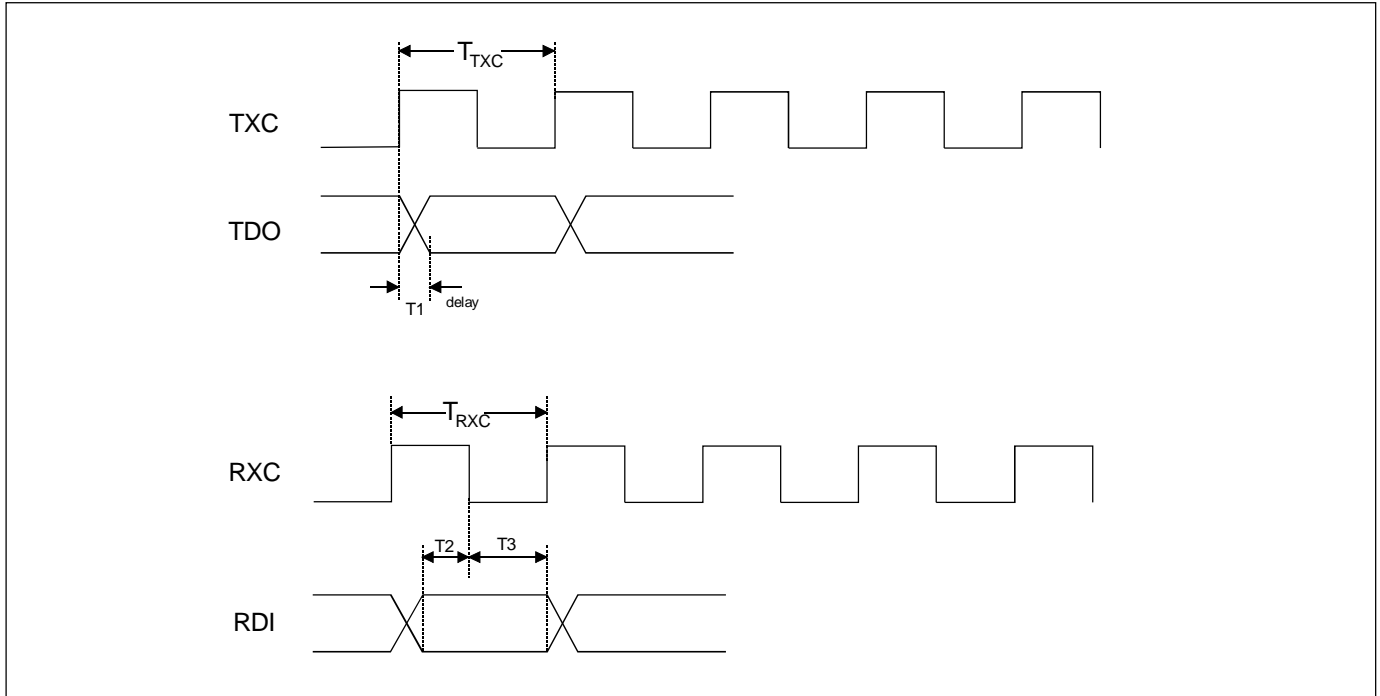
If pin TSL = 1 (Automatic synchronous sampling timing)

FUNCTIONS

◆ Asynchronous to synchronous converter

The synchronous start-stop character, TDI (transmitter data input), is read into the Tx buffer. When the character is available the data bits are transferred as TDO (transmitter data output) with the synchronous timing signal TXC (transmitter clock). The bit rate of TDI must be the same as the TDO rate within -2.5%...+1% or -2.5%...+2.3% tolerance depending on XESR (extended signalling rate) signal. The transmitter adds extra stop bits to the synchronous data stream, if TDI is slower than TDO. The over speed is handled by

deleting one stop bit in every 8th character at maximum in the synchronous output data TDO. When extended signal rate (XESR = 0) is used 4th stop bit may be deleted. When the transmitter detects a break signal(at least M bits of start polarity, where M is length of character), it sends 2M + 3 bits of start - polarity to TDO. If the break is longer than 2M + 3 bits, then all bits are transferred to TDO. After a break signal, at least 2M bits of stop polarity must be transmitted before sending further data.

◆ Synchronous to asynchronous converter

The synchronous RDI (receiver data input) is buffered to recognise the stop and start bits. If a missing stop bit is detected, it is added to the RDO (receiver data output). In this case the stop bits are shortened 12.5%

(25% if XESR = 0) during each character. When the receiver gets at least 2M + 3 bits of start polarity, it does not add stop bits to RDO. This enables the break signal to go through the buffer.

◆ Converting with higher speed timing

An alternative method to handle the over speed in asynchronous data is to boost synchronous timing TXC and RXC by 1-2%. In this mode XHST (higher speed timing) = 0. In this case there is no need to delete any

stop bits in the transmitter buffer. The break signal goes through unchanged. On the receiver side the synchronous data, RDI, is transferred directly to the asynchronous output RDO with RXC.

FUNCTIONS

◆ Timing selection

The MAS7838 requires clock signals in order to function properly. The synchronous data transfer always requires the TXC clock. The clock is used internally for:
- shifting data out from the TX buffer (to pin TDO)
- shifting data into the RX buffer (via pin RDI)
- detection of the bit rate in order to adjust the internal baud rate generator (only if TSL = 1)

The asynchronous data transfer (pins TDI, TDO) is accomplished by generating an internal timing signal for the asynchronous circuits. This internal timing signal (16T) is 16 times the TXC bit rate in order to sample the asynchronous data stream (TDI) at the proper speed.
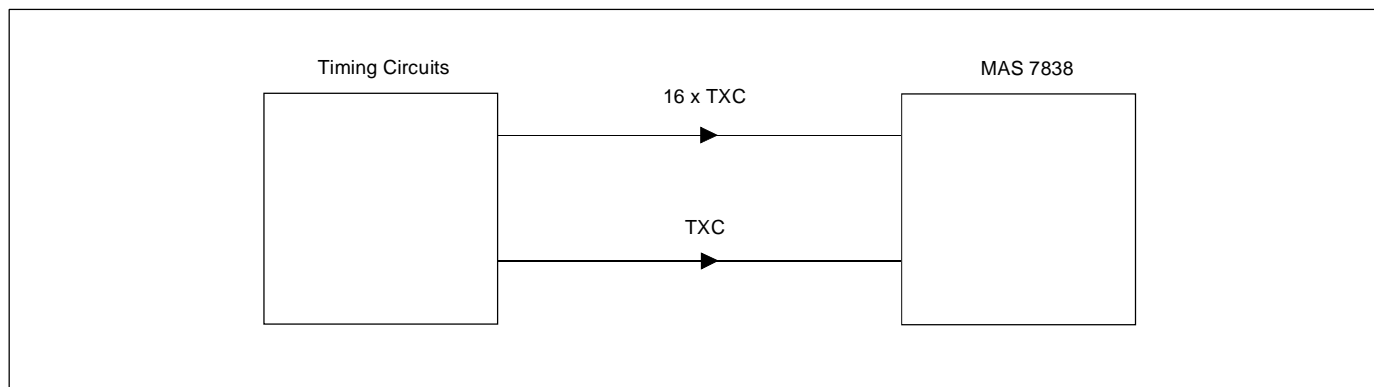
EXTERNALLY GENERATED 16T CLOCK

APPLICATION INFORMATION

◆ Synchronous modem with asynchronous interface

The MAS7838 is intended for applications where an asynchronous and synchronous data source must be linked together. A typical case appears in a data modem

where the terminal interface of the modem has been specified to be asynchronous but the modem data pump operates in a synchronous fashion.
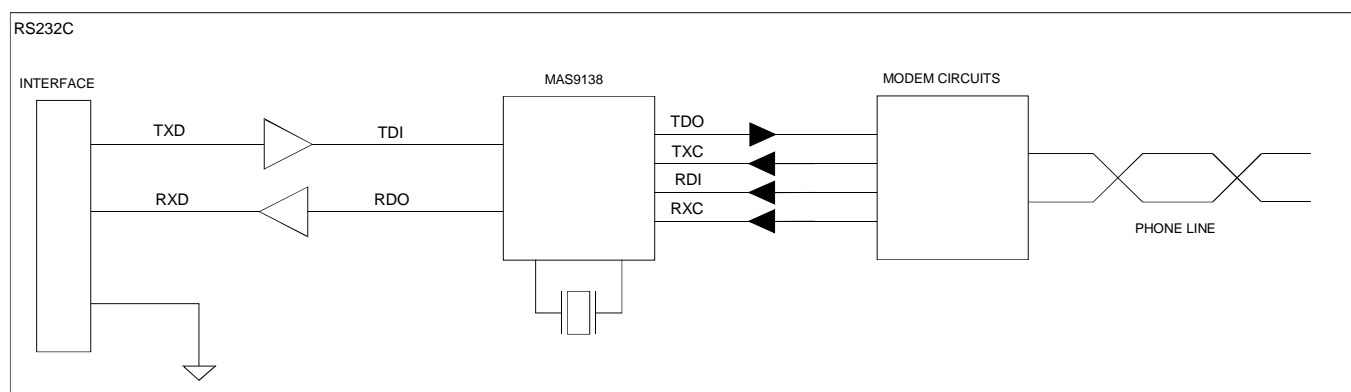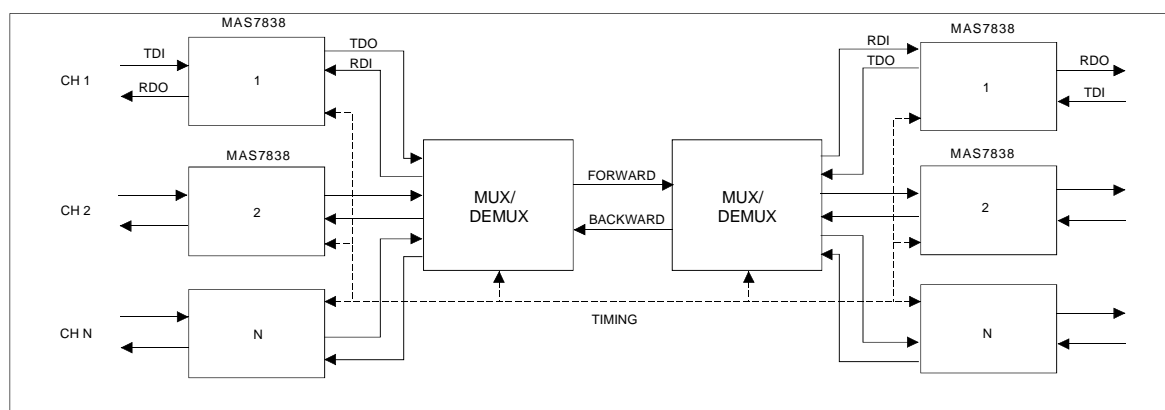
APPLICATION INFORMATION
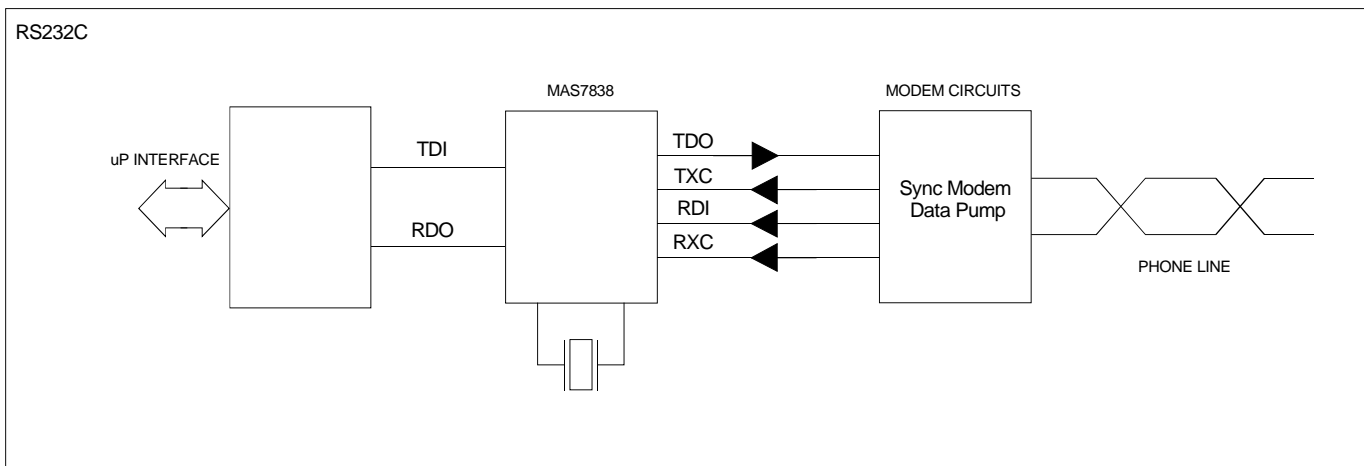
◆ **Synchronous serial interface with uP interface**

Another application is a synchronous serial interface for uP which uses UART as a data source. The concept is illustrated below.
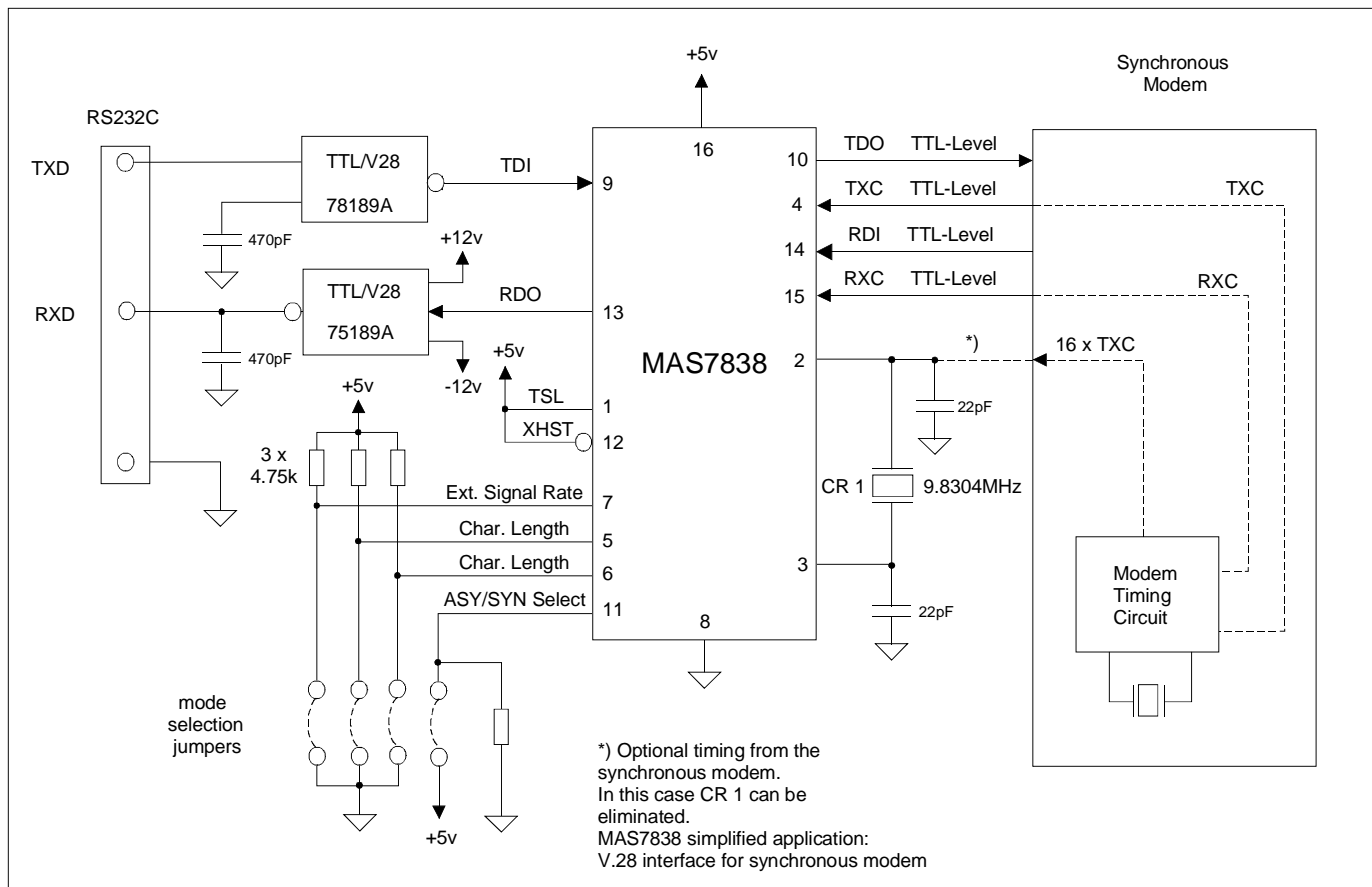
◆ **Data multiplexer**

A third application is a data multiplexing/demultiplexing system. The system accepts data from several sources. These data lines are sampled and the samples are sent through a multiplexer to a demultiplexer. To accomplish this, either a very high sample rate is needed or first convert the data to synchronous mode, where synchronous multiplexing can be used and only one sample per data bit is needed.
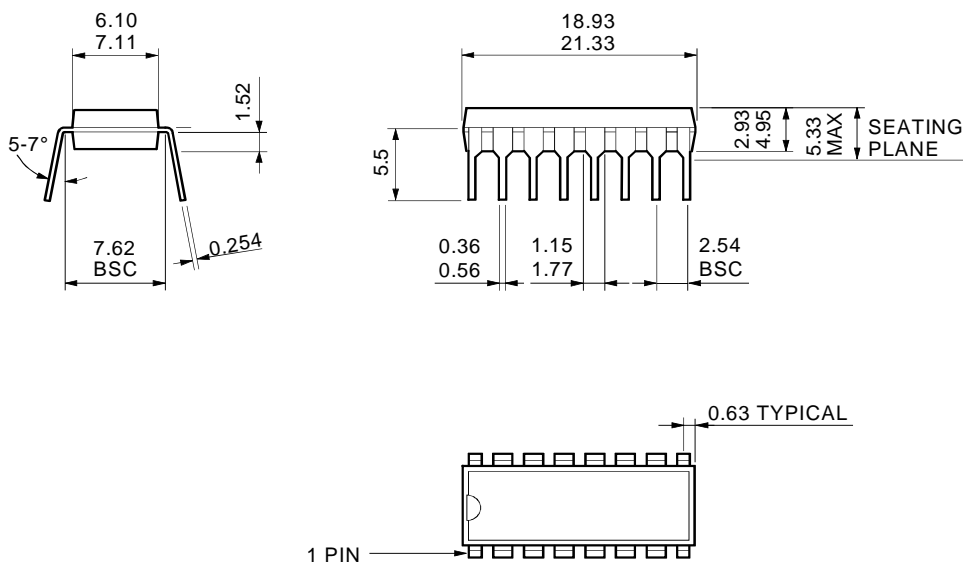
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APPLICATION INFORMATION

*) Optional timing from the
synchronous modem.
In this case CR 1 can be
eliminated.
MAS7838 simplified application:
V.28 interface for synchronous modem

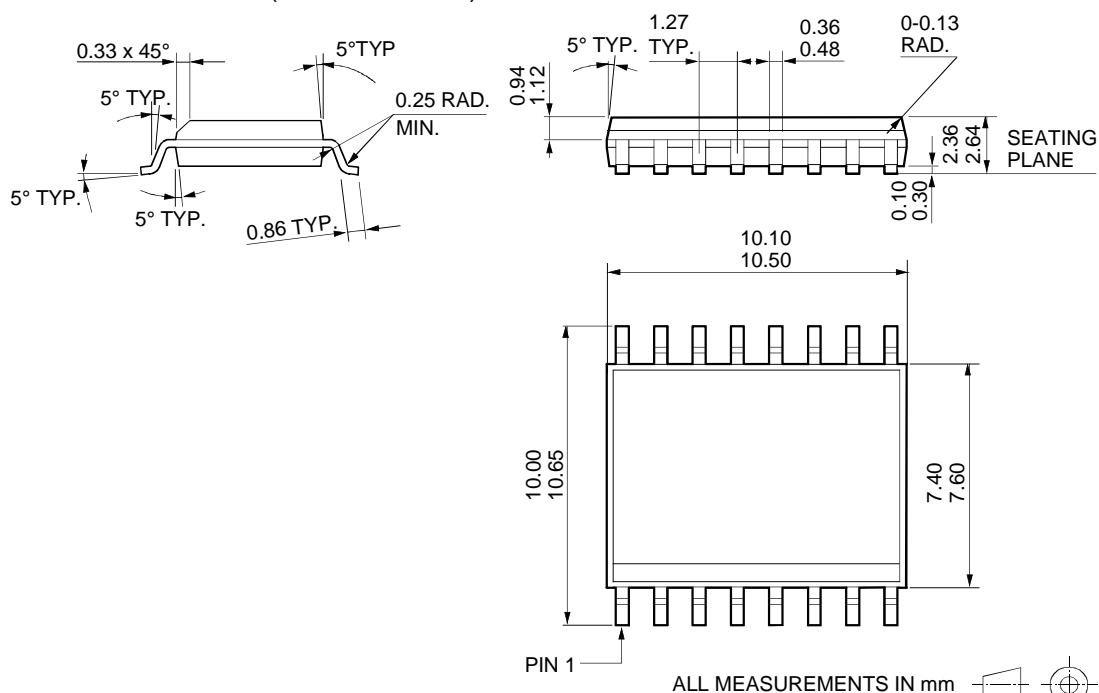**MICRO ANALOG SYSTEMS**

PACKAGE OUTLINES

16 LEAD PDIP OUTLINE (300 MIL BODY)

ALL MEASUREMENTS IN mm

All dimensions are in accordance with JEDEC standard MS-001.

16 LEAD SO OUTLINE (300 MIL BODY)

ALL MEASUREMENTS IN mm

All dimensions are in accordance with JEDEC standard MS-013.

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS7838N		PDIP16	25 pcs/tube
MAS7838S-T		SO16	1000 pcs/reel
MAS7838S		SO16	47 pcs/tube MSB0091A Bake recommendation for surface mounted devices

LOCAL DISTRIBUTOR

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