PRELIMINARY

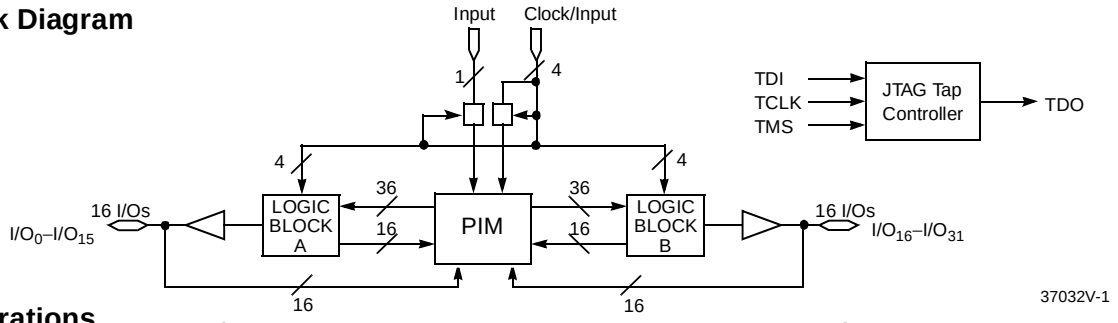
# CY37032V

# UltraLogic™ 32-Macrocell ISR™ CPLD

## Features

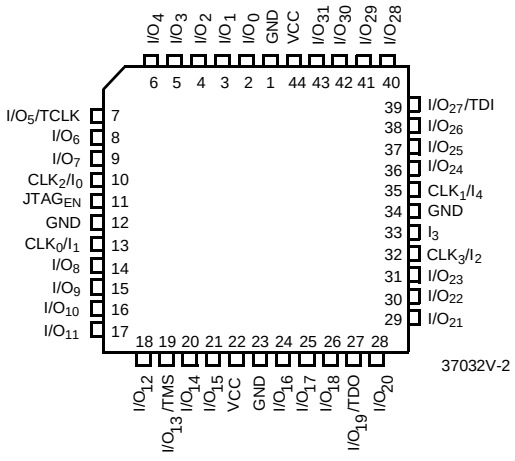
- 32 macrocells in two logic blocks
- 3.3V In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- IEEE standard 3.3V operation
  - 3.3V ISR
  - 5V tolerant
- Up to 32 I/Os
  - plus 5 dedicated inputs including 4 clock inputs
- High speed
  - $f_{MAX}$ = 143 MHz
  - $t_{PD}$ = 8.5 ns
  - $t_S$ = 5.0 ns
  - $t_{CO}$ = 6.0 ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant[1]
- Available in 44-pin TQFP, 44-pin PLCC
- Pinout compatible with the CY37032, CY37064/37064V

## Logic Block Diagram

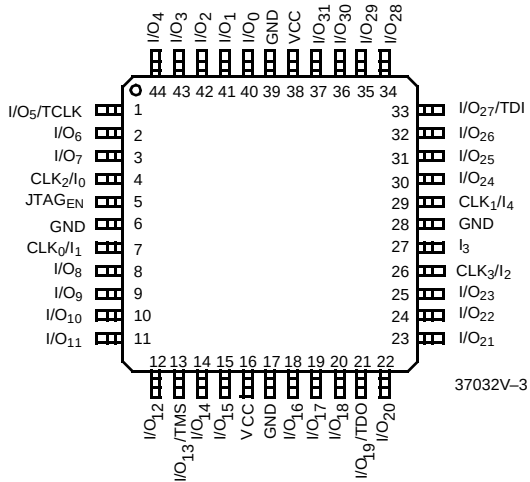



## Pin Configurations

**44-pin PLCC**
**Top View**




**44-pin TQFP**
**Top View**




## Selection Guide

| | CY37032V-143 | CY37032V-100 |
|---|---|---|
| Maximum Propagation Delay, $t_{PD}$ (ns) | 8.5 | 12 |
| Minimum Set-Up, $t_S$ (ns) | 5.0 | 7.0 |
| Maximum Clock to Output, $t_{CO}$ (ns) | 6.0 | 6.5 |
| Typical Supply Current, $I_{CC}$ (mA) in Low Power Mode | 15 | 15 |

**Note:**
1. Due to the 5V tolerant nature of the I/Os, the I/Os are not clamped to $V_{CC}$.

## Functional Description

The CY37032V is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37032V is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The CY37032V is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY37032V.

For a more detailed description of the architecture and features of the CY37032V see the Ultra37000 family data sheet.

## Fully Routable with 100% Logic Utilization

The CY37032V is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

## Simple Timing Model

The CY37032V features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

## Low-Power Operation

Each Logic Block of the CY37032V can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by $t_{LP}$

## Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

## In-System Reprogramming

The CY37032V can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37032V can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3*™ programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR Programming data sheet (CY3600i).

## User-Programmable Bus Hold

All outputs of the CY37032V can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

## Design Tools

Development software for the CY37032V is available from Cypress's *Warp*™ or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0V to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range[2]

| Range | Ambient Temperature[2] | Junction Temperature | $V_{CC}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0°C to +90°C | 3.3V ± 0.3V |
| Industrial | –40°C to +85°C | –40°C to +125°C | 3.3V ± 0.3V |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –4 mA (Com'l)[3] | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 8 mA (Com'l)[3] | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH voltage for all inputs[4] | | 2.0 | $V_{CCmax}$ | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW voltage for all inputs[4] | | –0.5 | 0.8 | V |
| $I_{IX}$ | Input Load Current | $V_I$ = GND OR $V_{CC}$ | | –10 | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | $V_O$ = GND or $V_{CC}$, Output Disabled | | –50 | 50 | µA |
| $I_{OS}$ | Output Short Circuit Current[5, 6] | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V | | –30 | –160 | mA |
| $I_{BHL}$ | Input Bus Hold LOW Sustaining Current | $V_{CC}$ = Min., $V_{IL}$ = 0.8V | | +75 | | µA |
| $I_{BHH}$ | Input Bus Hold HIGH Sustaining Current | $V_{CC}$ = Min., $V_{IH}$ = 2.0V | | –75 | | µA |
| $I_{BHLO}$ | Input Bus Hold LOW Overdrive Current | $V_{CC}$ = Max. | | | +500 | µA |
| $I_{BHHO}$ | Input Bus Hold HIGH Overdrive Current | $V_{CC}$ = Max. | | | –500 | µA |

## Inductance[6]

| Parameter | Description | Test Conditions | 44-lead TQFP | 44-lead PLCC | Unit |
|---|---|---|---|---|---|
| L | Maximum Pin Inductance | $V_{IN}$ = 3.3V at f = 1 MHz | 2 | 5 | nH |

## Capacitance[6]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance | $V_{IN}$ = 3.3V at f = 1 MHz at $T_A$ = 25°C | 8 | pF |
| $C_{CLK}$ | Clock Signal Capacitance | $V_{IN}$ = 3.3V at f = 1 MHz at $T_A$ = 25°C | 12 | pF |

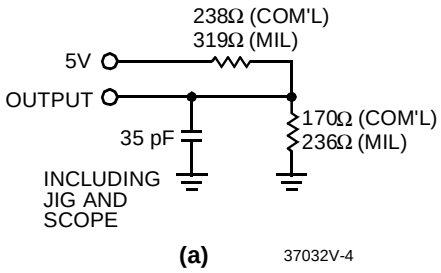
**Notes:**

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
3. $I_{OH}$ = –2 mA, $I_{OL}$ = 2 mA for TDO.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. $V_{OUT}$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested initially and after any design or process changes that may affect these parameters.

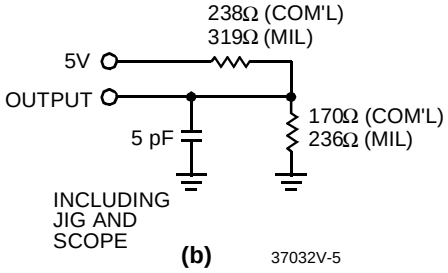
## Endurance Characteristics[6]

| Parameter | Description | Test Conditions | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions[2] | 1,000 | 10,000 | Cycles |

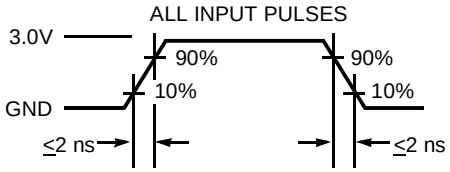
## AC Test Loads and Waveforms




(a) 37032V-4

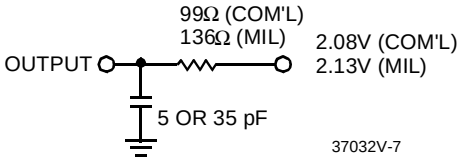



(b) 37032V-5

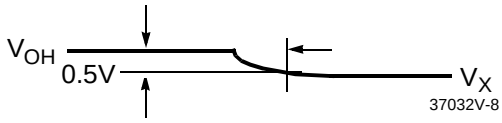
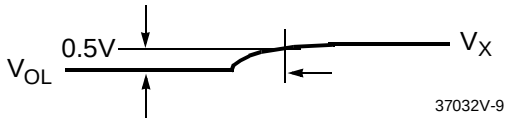
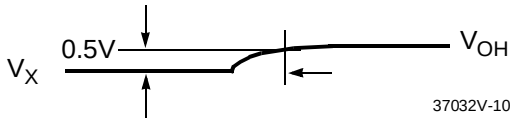
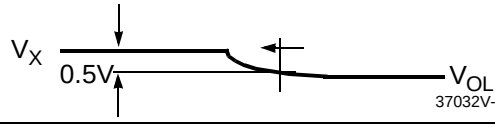



(c) 37032V-6

Equivalent to: THÉVENIN EQUIVALENT




37032V-7

| Parameter[7] | $V_X$ | Output Waveform–Measurement Level |
|---|---|---|
| $t_{ER(-)}$ | 1.5V |  |
| $t_{ER(+)}$ | 2.6V |  |
| $t_{EA(+)}$ | 1.5V |  |
| $t_{EA(-)}$ | $V_{the}$ |  |



**(d) Test Waveforms**

**Note:**

7. $t_{ER}$ measured with 5-pF AC Test Load and $t_{EA}$ measured with 35-pF AC Test Load.

## Switching Characteristics Over the Operating Range[8]

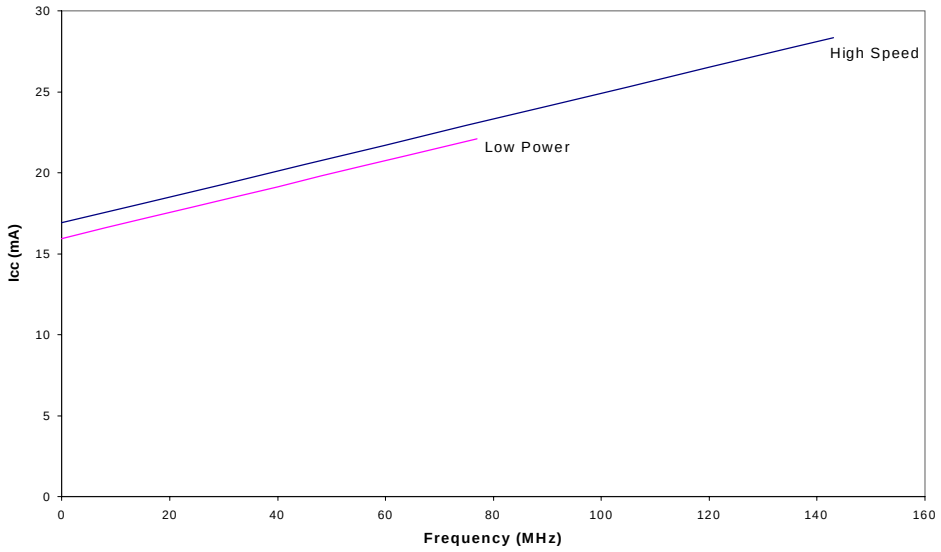
| Parameter | Description | 37032V-143 | | 37032V-100 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Combinatorial Mode Parameters** | | | | | | |
| $t_{PD}$[9, 10] | Input to Combinatorial Output | | 8.5 | | 12 | ns |
| $t_{PDL}$[9, 10] | Input to Output Through Transparent Input or Output Latch | | 12 | | 16.5 | ns |
| $t_{PDLL}$[9, 10] | Input to Output Through Transparent Input and Output Latches | | 13.5 | | 17 | ns |
| $t_{EA}$[9, 10] | Input to Output Enable | | 13 | | 16 | ns |
| $t_{ER}$[9] | Input to Output Disable | | 13 | | 16 | ns |
| **Input Register Parameters** | | | | | | |
| $t_{WL}$ | Clock or Latch Enable Input LOW Time[6] | 2.5 | | 3 | | ns |
| $t_{WH}$ | Clock or Latch Enable Input HIGH Time[6] | 2.5 | | 3 | | ns |
| $t_{IS}$ | Input Register or Latch Set-Up Time | 2 | | 2.5 | | ns |
| $t_{IH}$ | Input Register or Latch Hold Time | 2 | | 2.5 | | ns |
| $t_{ICO}$[9, 10] | Input Register Clock or Latch Enable to Combinatorial Output | | 12.5 | | 16 | ns |
| $t_{ICOL}$[9, 10] | Input Register Clock or Latch Enable to Output Through Transparent Output Latch | | 14 | | 18 | ns |
| **Synchronous Clocking Parameters** | | | | | | |
| $t_{CO}$[10] | Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable to Output | | 6 | | 6 | ns |
| $t_S$[9] | Set-Up Time from Input to Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable | 5 | | 7 | | ns |
| $t_H$ | Register or Latch Data Hold Time | 0 | | 0 | | ns |
| $t_{CO2}$[9, 10] | Output Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable to Combinatorial Output Delay (Through Logic Array) | | 12 | | 16 | ns |
| $t_{SCS}$[9] | Output Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable to Output Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable (Through Logic Array) | 7 | | 10 | | ns |
| $t_{SL}$[9] | Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable | 9 | | 12 | | ns |
| $t_{HL}$ | Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) or Latch Enable | 0 | | 0 | | ns |
| **Product Term Clocking Parameters** | | | | | | |
| $t_{COPT}$[9, 10] | Product Term Clock or Latch Enable (PTCLK) to Output | | 13 | | 13 | ns |
| $t_{SPT}$ | Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK) | 3 | | 3 | | ns |
| $t_{HPT}$ | Register or Latch Data Hold Time | 3 | | 3 | | ns |
| $t_{CO2PT}$[9, 10] | Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array) | | 19 | | 21 | ns |

**Notes:**
8. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
9. Logic Blocks operating in low power mode, add $t_{LP}$ to this spec.
10. Outputs using Slow Output Slew Rate, add $t_{SLEW}$ to this spec.

## Switching Characteristics Over the Operating Range[8] (continued)

| Parameter | Description | 37032V-143 | | 37032V-100 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Pipelined Mode Parameters** | | | | | | |
| $t_{ICS}$[9] | Input Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) to Output Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) | 7 | | 10 | | ns |
| **Operating Frequency Parameters** | | | | | | |
| $f_{MAX1}$ | Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[6] | 143 | | 100 | | MHz |
| $f_{MAX2}$ | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$) | 167 | | 143 | | MHz |
| $f_{MAX3}$ | Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$) | 91 | | 80 | | MHz |
| $f_{MAX4}$ | Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$) | 125 | | 100 | | MHz |
| **Reset/Preset Parameters** | | | | | | |
| $t_{RW}$ | Asynchronous Reset Width[6] | 8 | | 12 | | ns |
| $t_{RR}$[9] | Asynchronous Reset Recovery Time[6] | 10 | | 14 | | ns |
| $t_{RO}$[9, 10] | Asynchronous Reset to Output | | 14 | | 18 | ns |
| $t_{PW}$ | Asynchronous Preset Width[6] | 8 | | 12 | | ns |
| $t_{PR}$[9] | Asynchronous Preset Recovery Time[6] | 10 | | 14 | | ns |
| $t_{PO}$[9, 10] | Asynchronous Preset to Output | | 14 | | 18 | ns |
| **User Option Parameters** | | | | | | |
| $t_{LP}$ | Low Power Adder | | 4 | | 4 | ns |
| $t_{SLEW}$ | Slow Output Slew Rate Adder | | 2 | | 2 | ns |
| **JTAG Timing Parameters** | | | | | | |
| $t_{S\ JTAG}$ | Set-Up time from TDI and TMS to TCK | 0 | | 0 | | ns |
| $t_{H\ JTAG}$ | Hold Time on TDI and TMS | 20 | | 20 | | ns |
| $t_{CO\ JTAG}$ | Falling Edge of TCK to TDO | | 20 | | 20 | ns |
| $f_{JTAG}$ | Maximum JTAG Tap Controller Frequency | | 20 | | 20 | MHz |

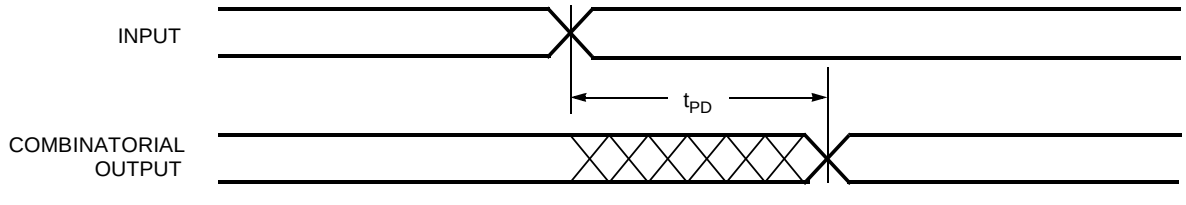
## Typical $I_{cc}$ Characteristics




The typical pattern is a 16 bit up counter, per logic block, with outputs disabled.
$V_{cc}$ = 3.3V, $T_A$ = Room Temperature

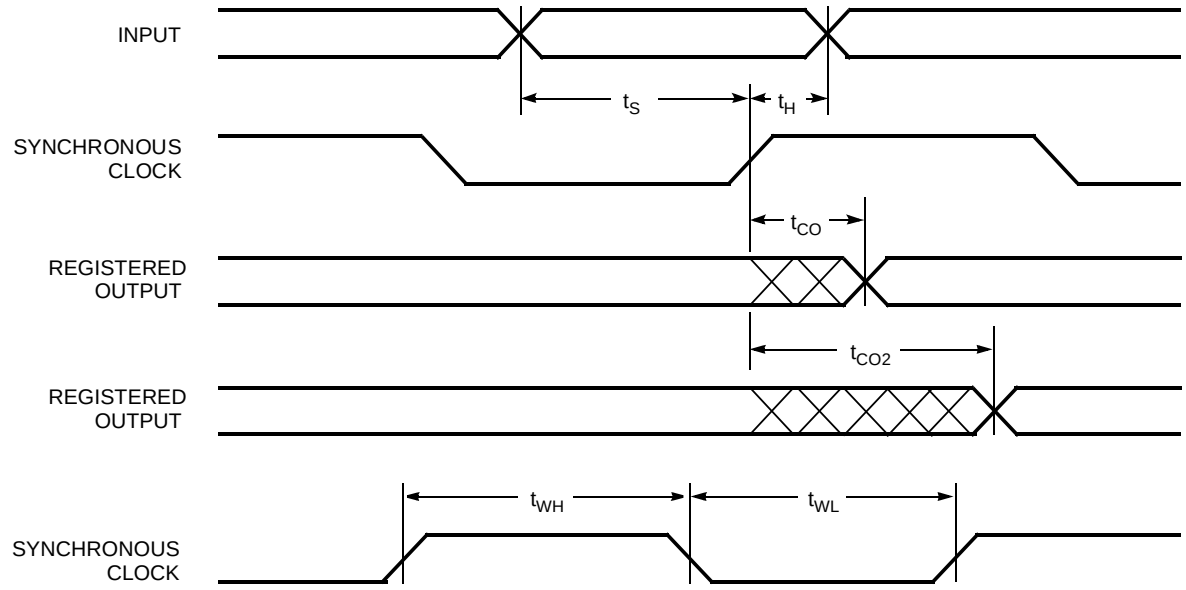
## Switching Waveforms

### Combinatorial Output



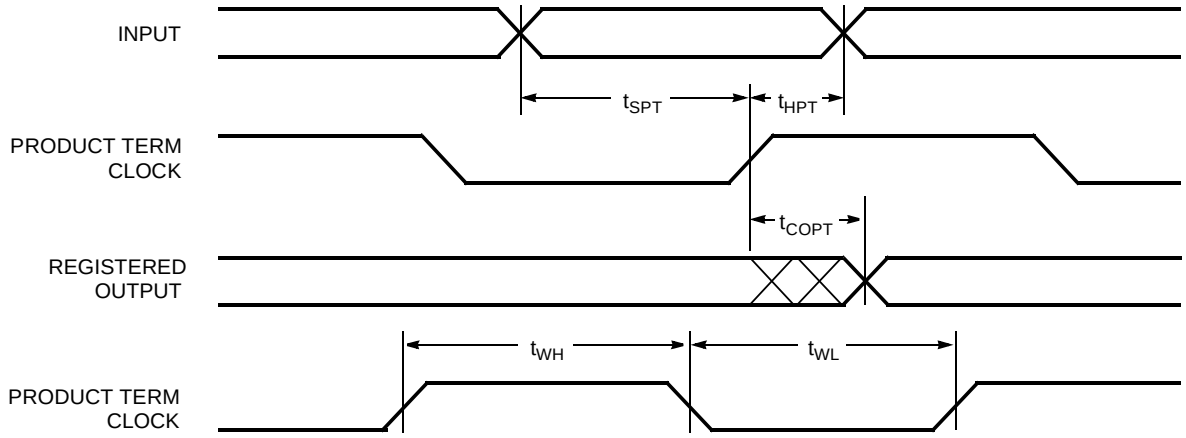

37032V-12

### Registered Output with Synchronous Clocking




37032V-13

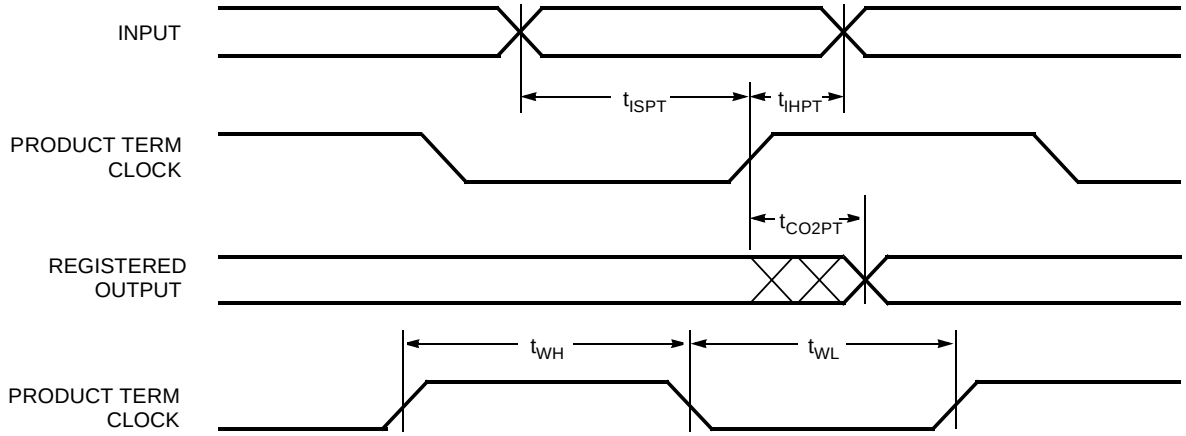
### Registered Output with Product Term Clocking Input Going Through the Array




37032V-14

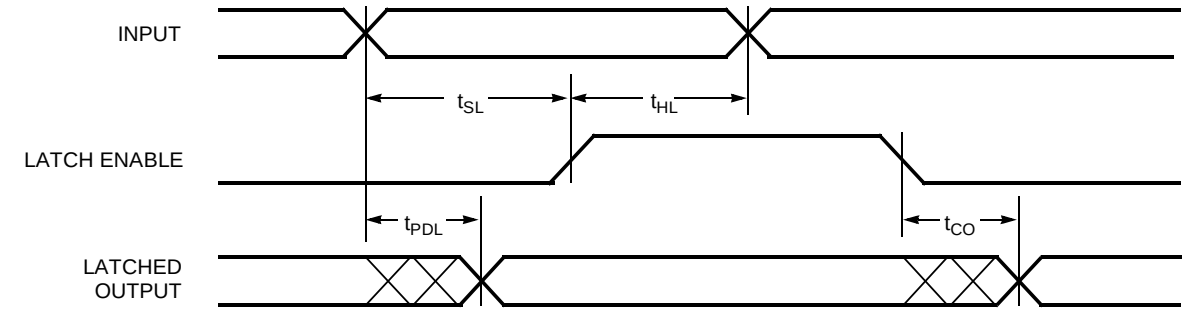
## Switching Waveforms (continued)

### Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



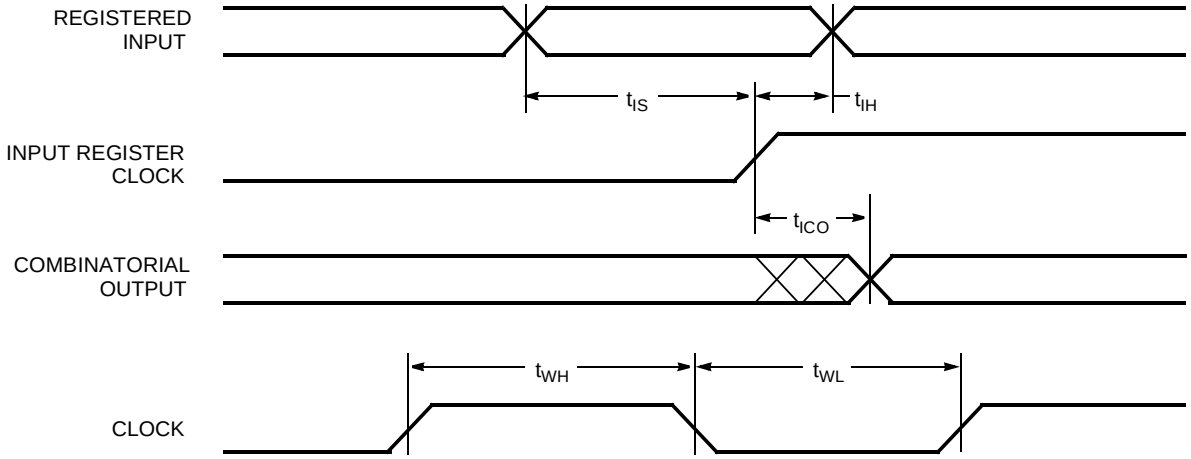

37032V-15

### Latched Output




37032V-16

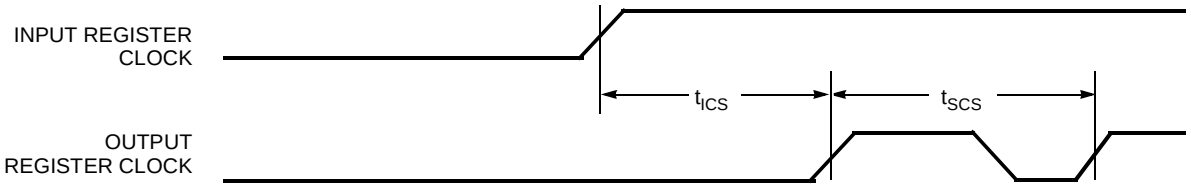
### Registered Input




37032V-17

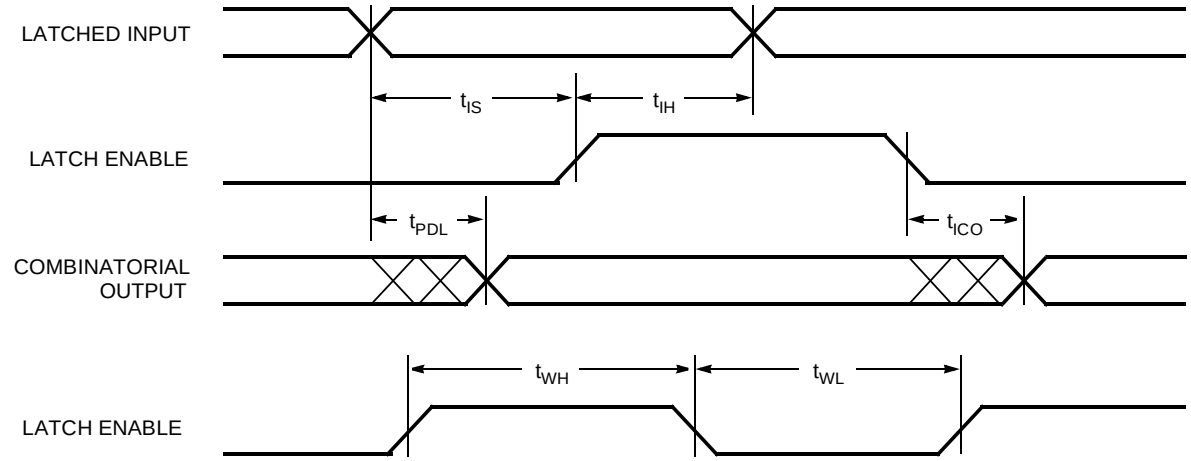
## Switching Waveforms (continued)

### Clock to Clock



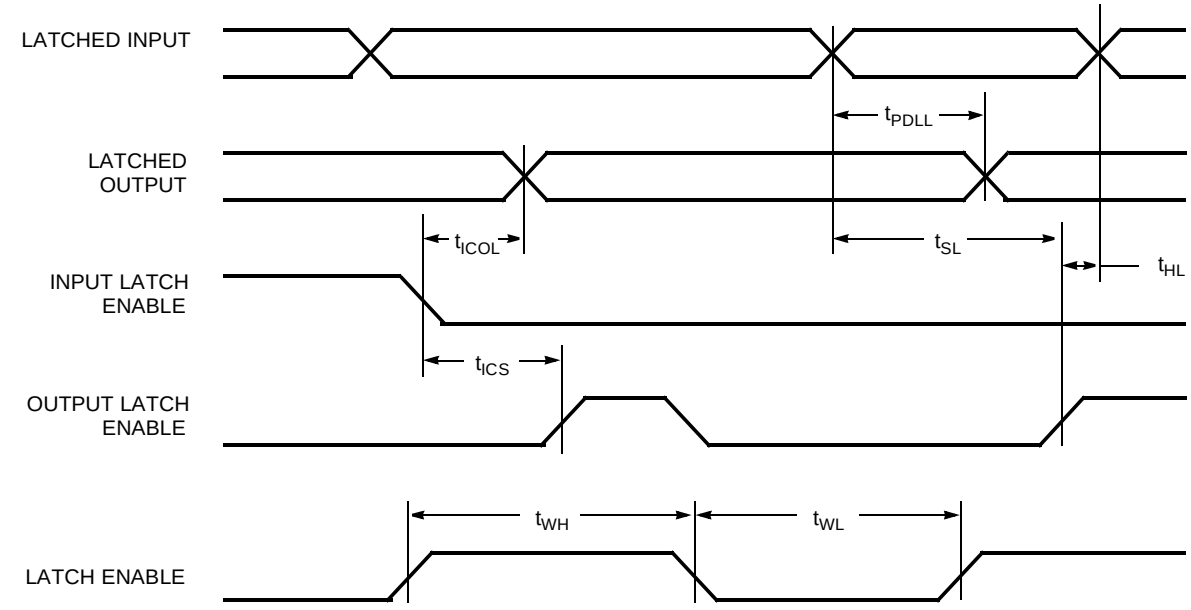

37032V-18

### Latched Input




37032V-19

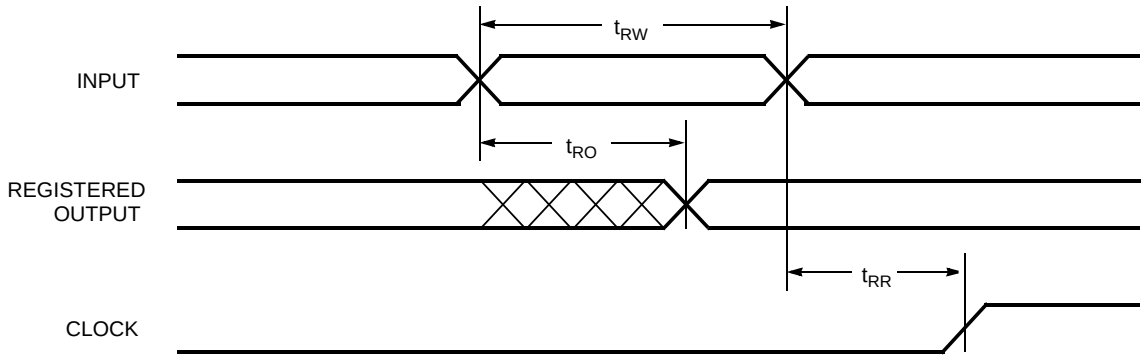
### Latched Input and Output




37032V-20

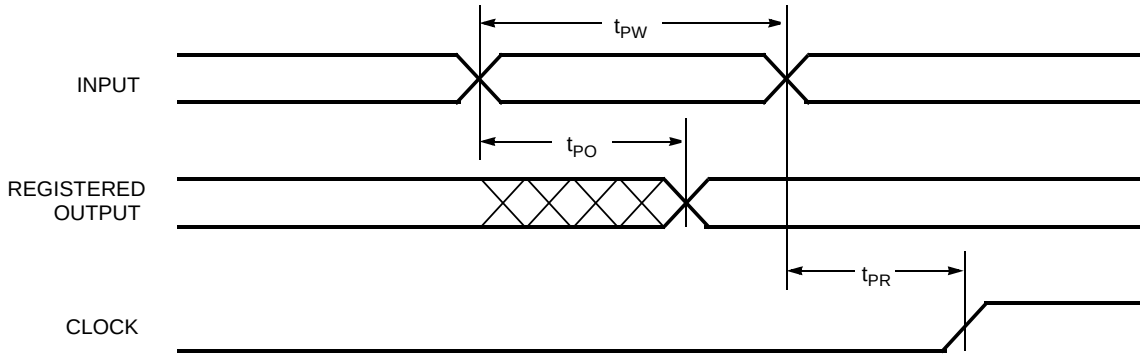
## Switching Waveforms (continued)

### Asynchronous Reset



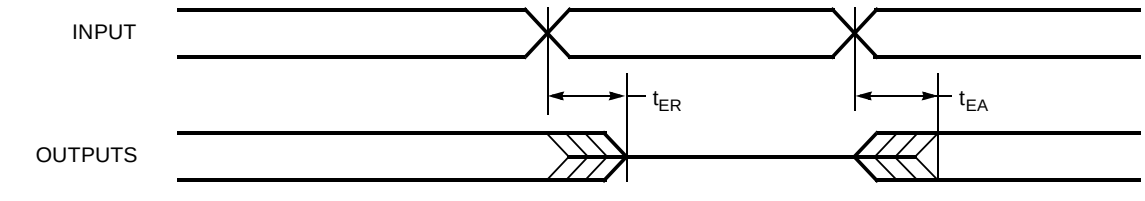

37032V-21

### Asynchronous Preset




37032V-22

### Output Enable/Disable




37032V–23

## Ordering Information

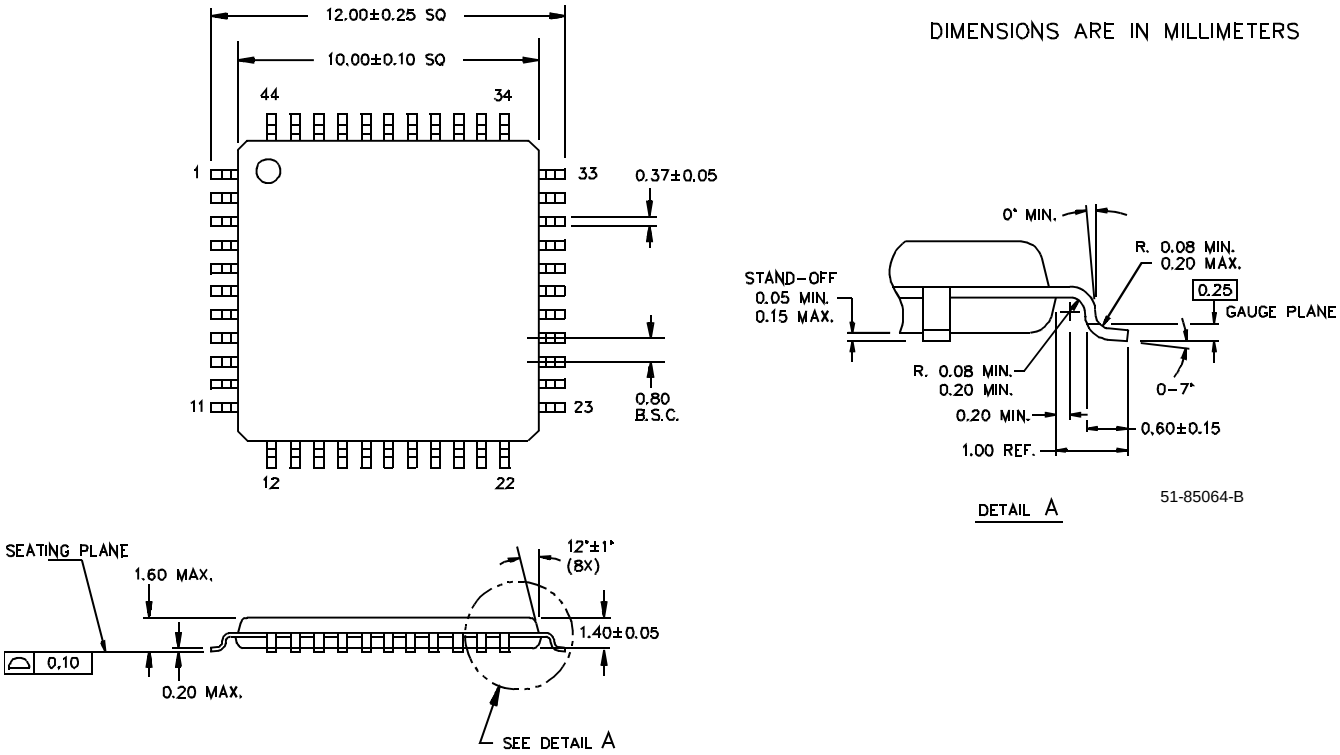
| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 143 | CY37032VP44-143AC | A44 | 44-Pin Thin Quad Flatpack | Commercial |
| | CY37032VP44-143JC | J67 | 44-Pin Plastic Leaded Chip Carrier | |
| 100 | CY37032VP44-100AC | A44 | 44-Pin Thin Quad Flatpack | Commercial |
| | CY37032VP44-100JC | J67 | 44-Pin Plastic Leaded Chip Carrier | |
| | CY37032VP44-100AI | A44 | 44-Pin Thin Quad Flatpack | Industrial |
| | CY37032VP44-100JI | J67 | 44-Pin Plastic Leaded Chip Carrier | |



Document #: 38–00713-A

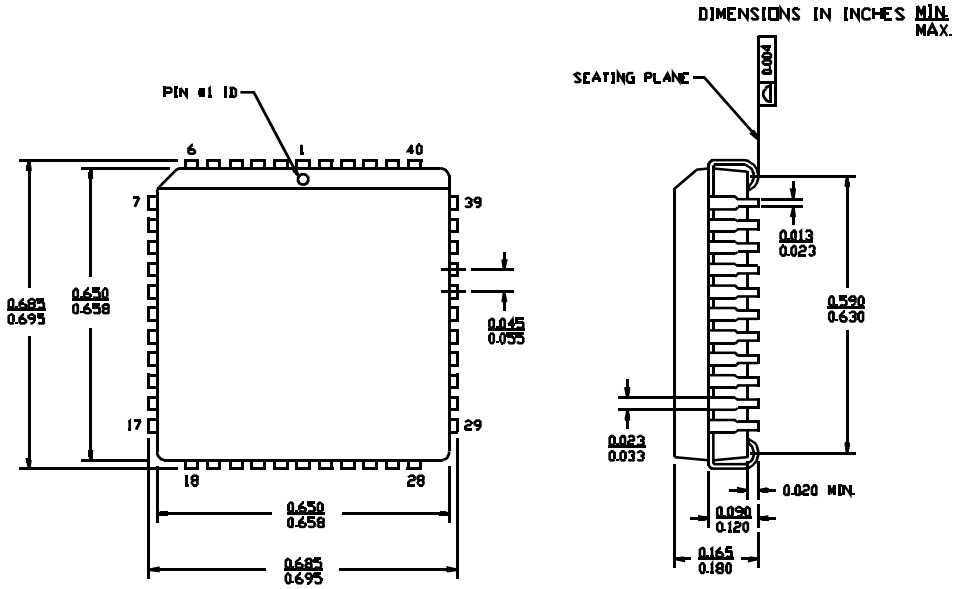
**Package Diagrams**

**44-Lead Thin Plastic Quad Flat Pack A44**



**Package Diagrams** (continued)

**44-Lead Plastic Leaded Chip Carrier J67**

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