TUSB9260
USB 3.0 TO SATA BRIDGE

Data Manual

Literature Number: SLLS962D
December 2009–Revised May 2011

Contents

List of Figures

List of Tables

USB 3.0 TO SATA BRIDGE

Check for Samples: TUSB9260

1 MAIN FEATURES

1.1 TUSB9260 Features

- Universal Serial Bus (USB)
  - SuperSpeed USB 3.0 Compliant - TID 340000007
    - Integrated Transceiver Supports SS/HS/FS Signaling
  - Best in Class Adaptive Equalizer
    - Allows for Greater Jitter Tolerance in the Receiver
  - USB Class Support
    - USB Attached SCSI Protocol (UASP)
    - USB Mass Storage Class Bulk-Only Transport (BOT)
    - Support for Error Conditions Per the 13 Cases (Defined in the BOT Specification)
    - USB Bootability Support
    - USB Human Interface Device (HID)
  - Supports Firmware Update Via USB, Using a TI Provided Application
- SATA Interface
  - Serial ATA Specification Revision 2.6
    - gen1i, gen1m, gen2i, and gen2m
  - Support for Mass-Storage Devices Compatible With the ATA/ATAPI-8 Specification
- Integrated ARM Cortex M3 Core
  - Customizable Application Code Loaded From EEPROM Via SPI Interface
  - Two Additional SPI Port Chip Selects for Peripheral Connection
  - Up to 12 GPIOs for End-User Configuration
    - 2 GPIOs Have PWM Functionality for LED Blink Speed Control
  - Serial Communications Interface for Debug (UART)
- General Features
  - Can Operate from Either a Single Low Cost Crystal or Clock Oscillator
    - Supports 40 MHz
  - A JTAG Interface is Used for IEEE1149.1 and IEEE1149.6 Boundary Scan
  - Available in a Fully RoHS Compliant Package

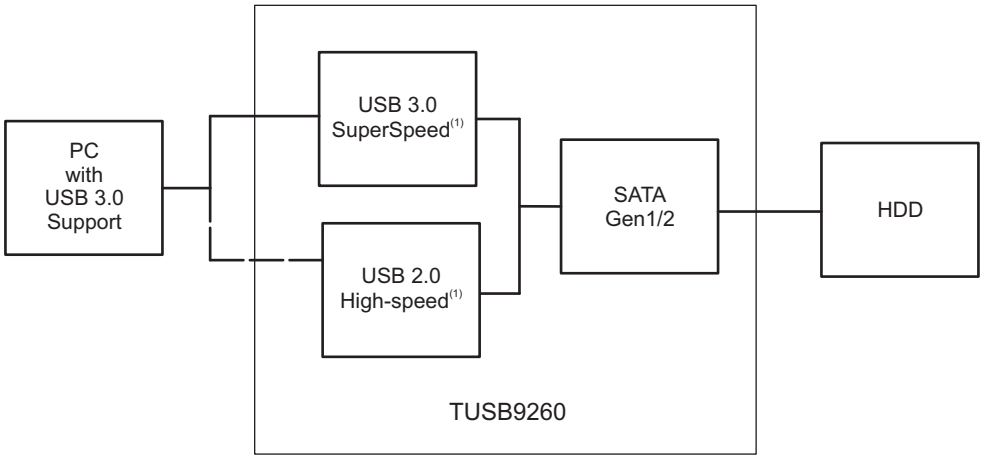
1.2 Target Applications

- External HDD/SSD
- External DVD
- External CD
- HDD-Based Portable Media Player

2 INTRODUCTION

2.1 System Overview

The TUSB9260 is an ARM cortex M3 microcontroller based USB 3.0 to serial ATA bridge. It provides the necessary hardware and firmware to implement a USB attached SCSI protocol (UASP) compliant mass storage device suitable for bridging hard disk drives (HDD), solid state disk drives (SSD), optical drives and other compatible SATA 1.5-Gbps or SATA 3.0-Gbps devices to a USB 3.0 bus. In addition to UASP support, the firmware implements the mass storage class bulk-only transport (BOT), and USB human in-terface device (HID) interfaces.



(1) USB connection is made at either SuperSpeed or High-Speed depending on the upstream connection support.

2.2 Device Block Diagram

The major functional blocks are as follows:

- Cortex M3 microcontroller subsystem including the following peripherals:
  - Time interrupt modules, including watchdog timer
  - Universal asynchronous receive/transmit (SCI)
  - Serial peripheral interface (SPI)
  - General purpose input/output (GPIO)
  - PWM for support of PWM outputs (PWM)
- USB 3.0 core (endpoint controller) and integrated SuperSpeed PHY
- AHCI compliant SATA controller and integrated SATA PHY
  - Supporting gen1i, gen1m, gen2i, and gen2m
- Chip level clock generation and distribution
- Support for JTAG 1149.1 and 1149.6

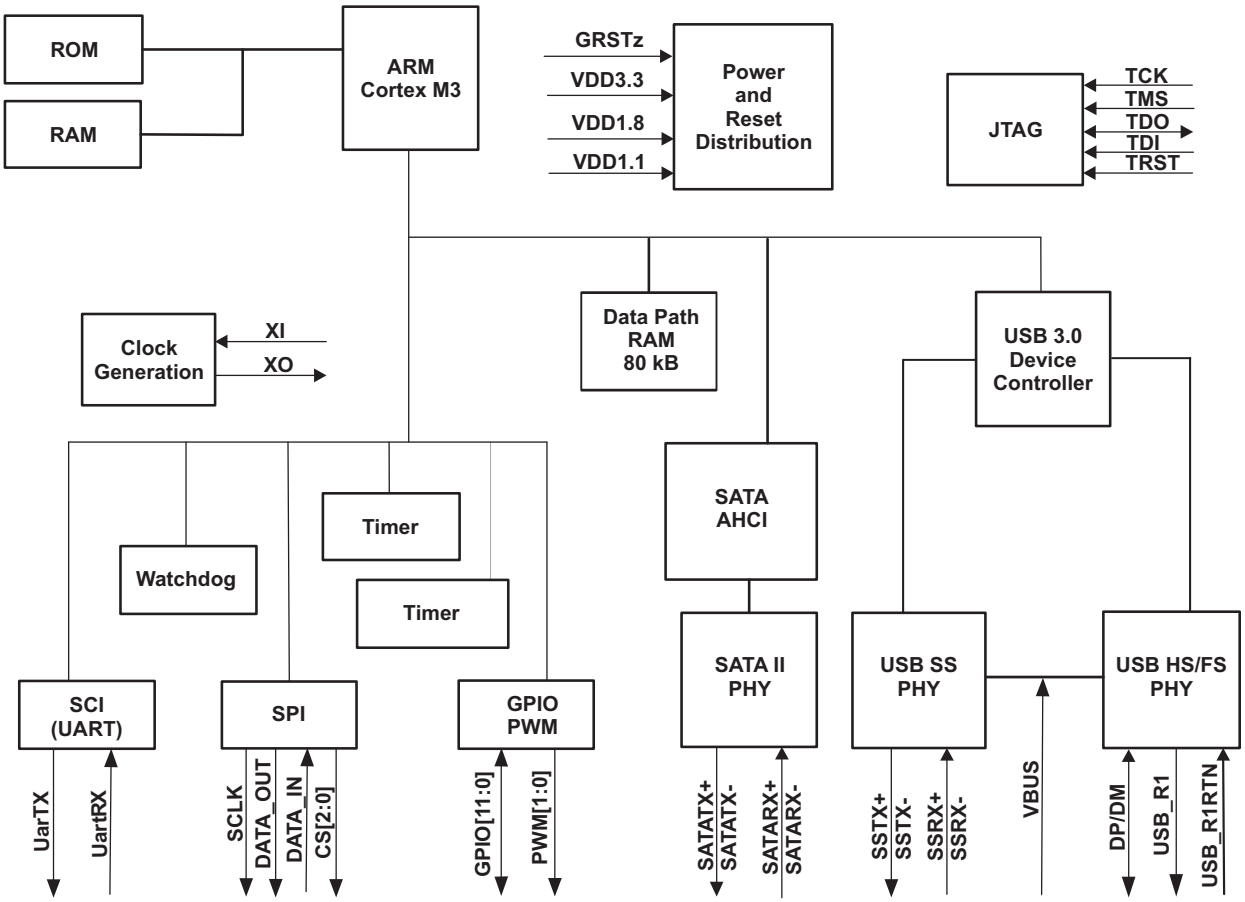


Figure 2-1. Device Block Diagram

3 OPERATION

3.1 General Functionality

The TUSB9260 ROM contains boot code that executes after a global reset which performs the initial con-figuration required to load a firmware image from an attached SPI flash memory to local RAM. In the ab-sence of an attached SPI flash memory or a valid image in the SPI flash memory, the firmware will idle and wait for a connection from a USB host through its HID interface which is also configured from the boot code. The latter can be accomplished using a custom application or driver to load the firmware from a file resident on the host system.

Once the firmware is loaded it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller. In addition, the configuration of the AHCI includes a port reset which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps).

The configuration of the USB device controller includes creation of the descriptors and configuration of the device endpoints for support of UASP and USB mass storage class bulk-only transport (BOT). In addition, the firmware provides any other custom configuration required for application specific implementation, for example a HID interface for user initiated backup.

After USB device controller configuration is complete, if a SATA device was detected during the AHCI con-figuration the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9260 will initially try to connect at SuperSpeed, if successful it will enter U0; otherwise, after the training time out it will enable the DP pull up and connect as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected, the firmware presents the BOT interface as the primary interface and the UASP inter-face as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

Following speed negotiation, the device should transmit a device to host (D2H) FIS with the device signature. This first D2H FIS is received by the link layer and copied to the port signature register. When firmware is notified of the device connection it queries the device for capabilities using the IDENTIFY DEVICE command. Firmware then configures the device as appropriate for its interface and features supported, for example an HDD that supports native command queuing (NCQ).

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class bulk-only transport (BOT), allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application specific implementation, for example a HID interface for user initiated backup.

After USB device controller configuration is complete, if a SATA device was detected during the AHCI configuration the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9260 will initially try to connect at SuperSpeed, if successful it will enter U0; otherwise, after the training time out it will enable the DP pull up and connect as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected as a SuperSpeed device, the firmware presents the UASP interface as the primary interface, and the BOT interface as a secondary interface. If the host stack is not UASP aware, it can enable the BOT interface using a SET_INTERFACE request for alternate interface 1.

3.2 Firmware Support

Default firmware support is provided for the following:

- USB 3.0 SuperSpeed and USB 2.0 High-Speed and Full-Speed
- USB Attached SCSI Protocol (UASP)
- USB Mass Storage Class (MSC) Bulk-Only Transport (BOT)
  - Including the 13 Error Cases
- USB Mass Storage Specification for Bootability
- USB Device Class Definition for Human Interface Devices (HID)
  - Firmware Update and Custom Functionality (e.g. One-Touch Backup)
- Serial ATA Advanced Host Controller Interface (AHCI)
- General Purpose Input/Output (GPIO)
  - LED Control and Custom Functions (e.g. One-Touch Backup Control)
- Pulse Width Modulation (PWM)
  - LED Dimming Control
- Serial Peripheral Interface (SPI)
  - Firmware storage and storing Custom Device Descriptors
- Serial Communications Interface (SCI)
  - Debug Output Only

3.3 GPIO/PWM LED Designations

The default firmware provided by TI drives the GPIO and PWM outputs as listed in the table below.

Table 3-1. GPIO/PWM LED Designations

GPIO0	SW heartbeat	
GPIO1/GPIO5	USB3 power state (U0-U3)	00: U3 state or default 01: U2 state 10: U1 state 11: U0 state
GPIO2	HS/FS suspend	
GPIO3	Push button input on customer board	
GPIO4	Not used	
GPIO6	FS/HS connected	
GPIO7	SS connected	
PWM0	Disk activity	
PWM1	U3 or HS/FS suspend state (fades high and low)	
GPIO10 (SPICS1)	Not used	
GPIO11 (SPICS2)	Not used	

The LED's on the TUSB9260 Product Development Kit (PDK) board are connected as in the table above. Please see the TUSB9260 PDK Guide (SLLA303) for more information on GPIO LED connection and usage. This EVM is available for purchase, contact TI for ordering information.

3.4 Power Up and Reset Sequence

The TUSB9260 does not have specific power sequencing requirements with respect to the core power (VDD), I/O power (VDD33), or analog power (VDDA11, VDDA33, VDDA18, and VDDR18). The core power (VDD) or IO power (VDD33) may be powered up for an indefinite period of time while others are not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, par-ticularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 1 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz.

4 SIGNAL DESCRIPTIONS

Table 4-1. I/O Definitions

I/O TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input - Output
PU	Internal pull-up resistor
PD	Internal pull-down resistor
PWR	Power signal

Table 4-2. Clock and Reset Signals

TERMINAL		I/O	DESCRIPTION		
NAME	PIN NO.				
GRSTz	4	I PU	Global power reset. This reset brings all of the TUSB9260 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.		
XI	52	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.		
XO	54	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.		
FREQSEL[1:0]	31, 30	I PU	Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows:		
			FREQSEL[1]	**FREQSEL[0]**	**INPUT CLOCK FREQUENCY**
			0	0	Reserved
			0	1	Reserved
			1	0	Reserved
			1	1	40 MHz

Table 4-3. SATA Interface Signals(1)

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SATA_TXP	57	O	Serial ATA transmitter differential pair (positive)
SATA_TXM	56	O	Serial ATA transmitter differential pair (negative)
SATA_RXP	60	I	Serial ATA receiver differential pair (positive)
SATA_RXM	59	I	Serial ATA receiver differential pair (negative)

(1) Note that the default firmware and reference design for the TUSB9260 have the SATA TXP/TXM swapped for ease of routing in the reference design. If you plan to use the TI default firmware please review the reference design in the TUSB9260 DEMO User's Guide (SLLU131) for proper SATA connection.

Table 4-4. USB Interface Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
USB_SSTXP	43	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM	42	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP	46	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM	45	I	USB SuperSpeed receiver differential pair (negative)
USB_DP	36	I/O	USB High-speed differential transceiver (positive)
USB_DM	35	I/O	USB High-speed differential transceiver (negative)
USB_VBUS	33	I	USB bus power
USB_R1	39	O	Precision resistor reference. A 10-kΩ ±1% resistor should be connected between R1 and R1RTN.
USB_R1RTN	40	I	Precision resistor reference return

Table 4-5. Serial Peripheral Interface (SPI) Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SPI_SCLK	17	O PU	SPI clock
SPI_DATA_IN	18	I PU	SPI master data in
SPI_DATA_OUT	20	O PU	SPI master data out
SPI_CS0	21	O PU	Primary SPI chip select for Flash RAM
SPI_CS2/ GPIO11	23	I/O PU	SPCI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O.
SPI_CS1/ GPIO10	22	I/O PU	SPCI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O.

Table 4-6. JTAG, GPIO, and PWM Signals

TERMINAL NAME	PIN NO.	I/O	DESCRIPTION
JTAG_TCK	25	I PD	JTAG test clock
JTAG_TDI	26	I PU	JTAG test data in
JTAG_TDO	27	O PD	JTAG test data out
JTAG_TMS	28	I PU	JTAG test mode select
JTAG_TRSTz	29	I PD	JTAG test reset
GPIO9/UART_TX	6	I/O PU	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general purpose output.
GPIO8/UART_RX	5	I/O PU	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general purpose output.
GPIO7	16	I/O PD	Configurable as general purpose input/outputs
GPIO6	15	I/O PD	
GPIO5	14	I/O PD	
GPIO4	13	I/O PD	
GPIO3	11	I/O PD	
GPIO2	10	I/O PD	
GPIO1	9	I/O PD	
GPIO0	8	I/O PD	
PWM0	2	O PD(1)	Pulse Width Modulation (PWM). Can be used to drive status LED's.
PWM1	3	O PD(1)	

(1) PWM pull down resistors are disabled by default. A firmware modification is required to turn them on. All other internal pull up/down resistors are enabled by default.

Table 4-7. Power and Ground Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
VDDR18	48, 62	PWR	1.8-V power rail
VDDA18	37	PWR	1.8-V analog power rail
VDD	1, 12, 19, 32, 38, 41, 44, 47, 49, 55, 58, 61, 63, 64	PWR	1.1-V power rail
VDD33	7, 24, 50, 51	PWR	3.3-V power rail
VDDA33	34	PWR	3.3-V analog power rail
VSSOSC	53	PWR	Oscillator ground. If using a crystal, this should not be connected to PCB ground plane. If using an oscillator, this should be connected to PCB ground. See the Clock Source Requirements section for more details.
VSS	65	PWR	Ground - Thermal Pad

5 CLOCK CONNECTIONS

5.1 Clock Source Requirements

The TUSB9260 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance be-tween XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capaci-tors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (C_{load}) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in Figure 5-1. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB9260 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

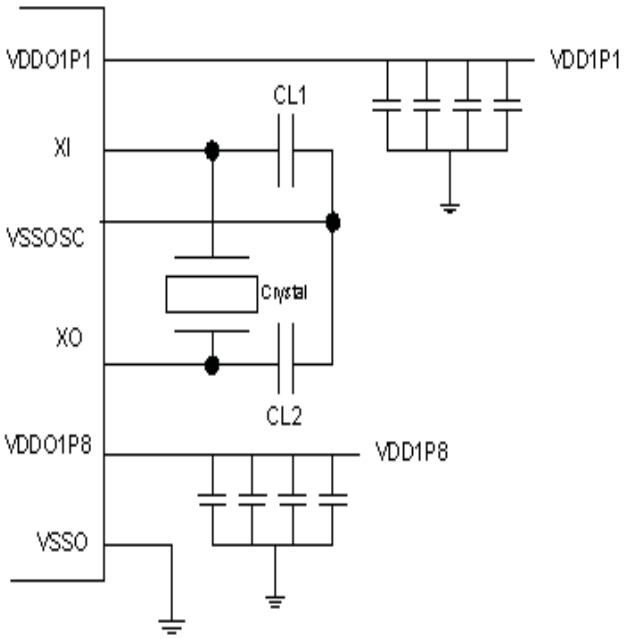


Figure 5-1. Typical Crystal Connections

5.2 Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock will degrade both the trans-mit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the Lock Detector to issue an Unlock signal. A good quality, low jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function - JTF). As the PLL typically has a number of additional jitter compo-nents, the Reference Clock jitter must be considerably below the overall jitter budget.

5.3 Oscillator

XI should be tied to the 1.8-V clock source and XO should be left floating.

VSSOSC should be connected to the PCB ground plane.

A 40-MHz clock can be used.

Table 5-1. Oscillator Specification

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
C_{XI}	XI input capacitance	VDDIO = 1.8 V, T_J = 25°C		0.414		pF
V_{IL}	Low-level input voltage				0.35 x VDDR18	V
V_{IH}	High-level input voltage		0.65 x VDDR18			V
T_{tosc_i}	Frequency tolerance	Operational temperature	–50		50	ppm
T_{duty}	Duty cycle		45	50	55	%
T_R/T_F	Rise/Fall time	20% - 80 %			6	ns
R_J	Reference clock R_J	JTF (1 sigma)(1)(2)			0.8	ps
T_J	Reference clock T_J	JTF (total p-p)(2)(3)			25	ps
T_{p-p}	Reference clock jitter	(absolute p-p)(4)			50	ps

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as 14.1 x R_J + D_J
(4) Absolute phase jitter (p-p)

5.4 Crystal

A parallel, 20-pF load capacitor should be used if a crystal source is used.

VSSOSC should not be connected to the PCB ground plane.

A 40-MHz crystal can be used.

Table 5-2. Crystal Specification

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
T_{tosc_i}	Frequency tolerance	Operational temperature	–50		50	ppm
	Frequency stability	1 year aging	–50		50	ppm
C_L	Load capacitance		12	20	24	pF

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDDR18/ VDDA18	Steady-state supply voltage	–0.3 to 2.45	V
VDD	Steady-state supply voltage	–0.3 to 1.4	V
VDD33/ VDDA33	Steady-state supply voltage	–0.3 to 3.8	V

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDR18	Digital 1.8 supply voltage	1.71	1.8	1.89	V
VDDA18	Analog 1.8 supply voltage	1.62	1.8	1.89	V
VDD	Digital 1.1 supply voltage	1.045	1.1	1.155	V
VDD33	Digital 3.3 supply voltage	3	3.3	3.6	V
VDDA33	Analog 3.3 supply voltage	3	3.3	3.6	V
VBUS	Voltage at VBUS PAD	0		1.155	V
T_A	Operating free-air temperature range	0		70	°C
T_J	Operating junction temperature range	0		105	°C
	HBM ESD			1000	V
	CDM ESD			500	V

6.3 DC Electrical Characteristics for 3.3-V Digital I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
T_R	Rise time	5 pF			1.5	ns
T_F	Fall time	5 pF			1.53	ns
I_{OL}	Low-level output current	VDD33 = 3.3 V, T_J = 25°C		6		mA
I_{OH}	High-level output current	VDD33 = 3.3 V, T_J = 25°C		–6		mA
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OL} = –2 mA	2.4			V
V_O	Output voltage		0		VDD33	V
RECEIVER						
V_I	Input voltage		0		VDD33	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Input hysteresis		200			mV
t_T	Input transition time (T_R and T_F)				10	ns
I_I	Input current	V_I = 0 V to VDD33			12	µA
C_I	Input capacitance	VDD33 = 3.3 V, T_J = 25°C		0.384		pF

7 POWER CONSUMPTION

All transfers are to a SATA Gen II SSD. A SATA Gen I target yields an approximate 10-mA power savings on the 1.1-V rail.

Table 7-1. SuperSpeed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL IDLE CURRENT (mA)(2)
VDD11(3)	319	308
VDD18(4)	58	58
VDD33(5)	6	6

(1) Transferring data via SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.
(2) SATA Gen II SSD attached no active transfer. No SATA power management, U0 only.
(3) All 1.1-V power rails connected together.
(4) All 1.8-V power rails connected together.
(5) All 3.3-V power rails connected together.

Table 7-2. High Speed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL IDLE CURRENT (mA)(2)
VDD11(3)	197	193
VDD18(4)	45	36
VDD33(5)	14	14

(1) Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.
(2) SATA Gen II SSD attached no active transfer. No SATA power management.
(3) All 1.1-V power rails connected together.
(4) All 1.8-V power rails connected together.
(5) All 3.3-V power rails connected together.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB9260PVP	NRND	Production	HTQFP (PVP) | 64	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB9260
TUSB9260PVP.A	NRND	Production	HTQFP (PVP) | 64	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB9260

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

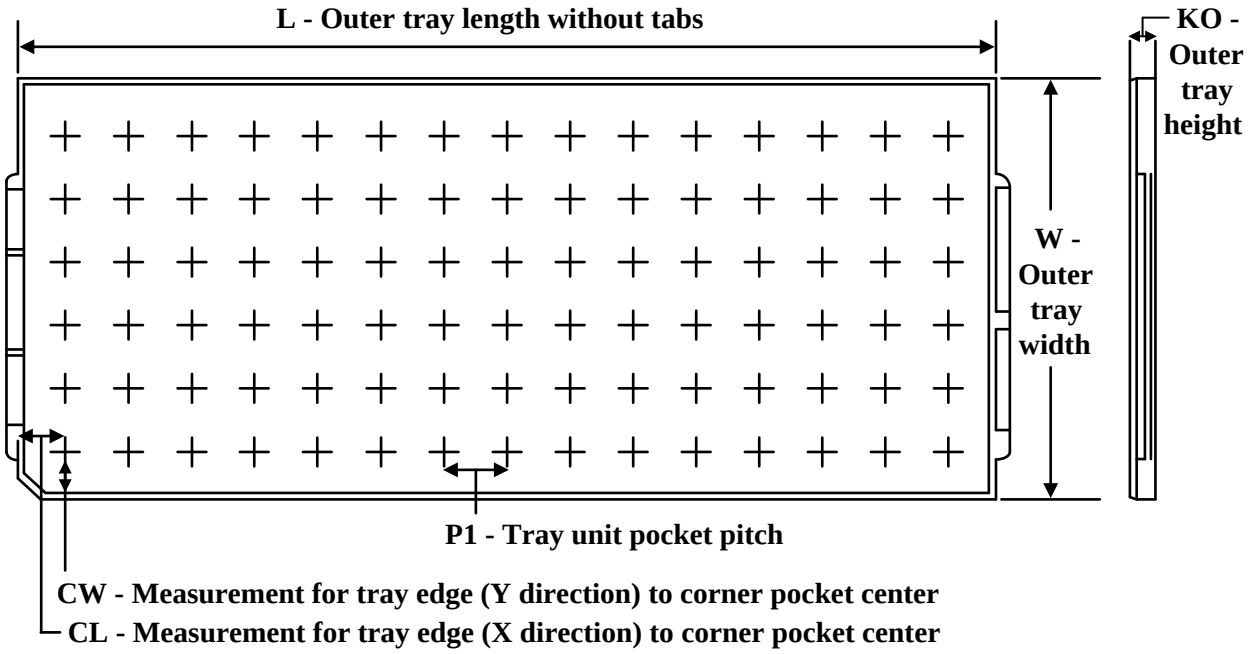
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

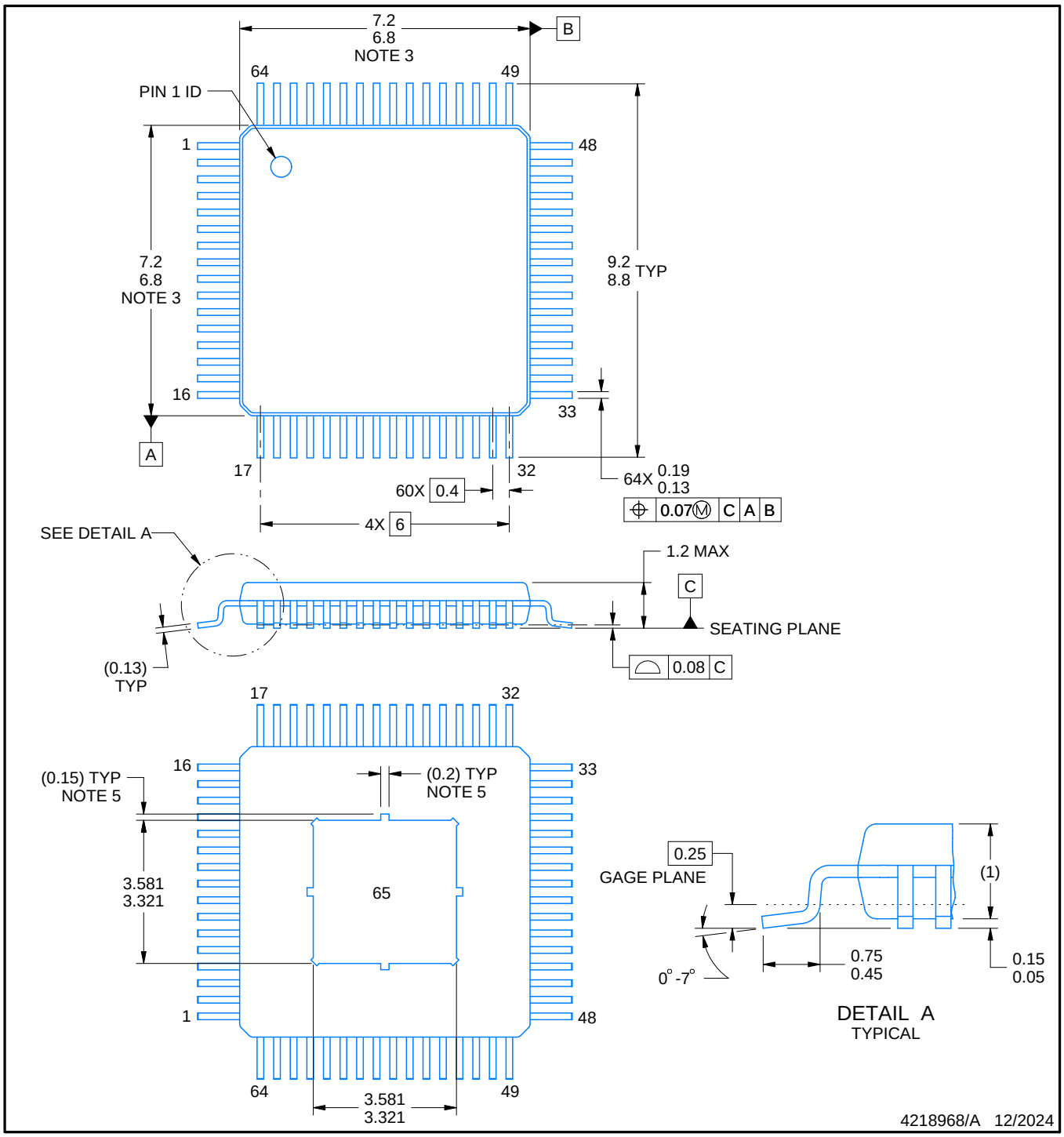
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TUSB9260PVP	PVP	HTQFP	64	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TUSB9260PVP.A	PVP	HTQFP	64	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PVP0064A

PowerPAD™ HTQFP - 1.2 mm max height

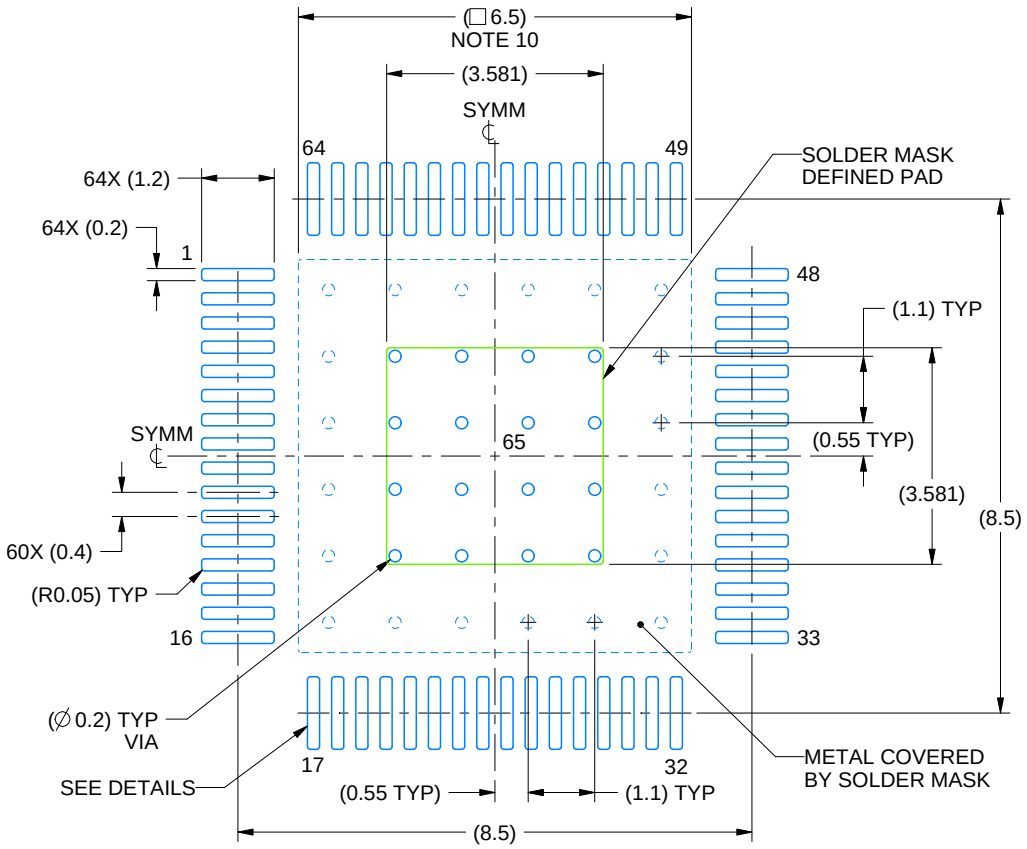
PLASTIC QUAD FLATPACK



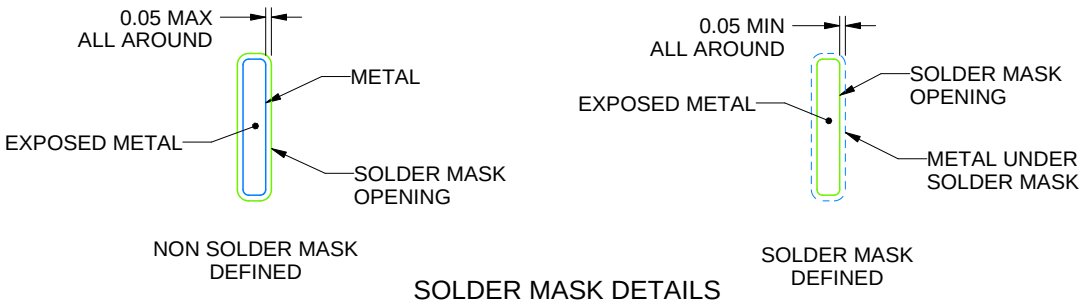
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

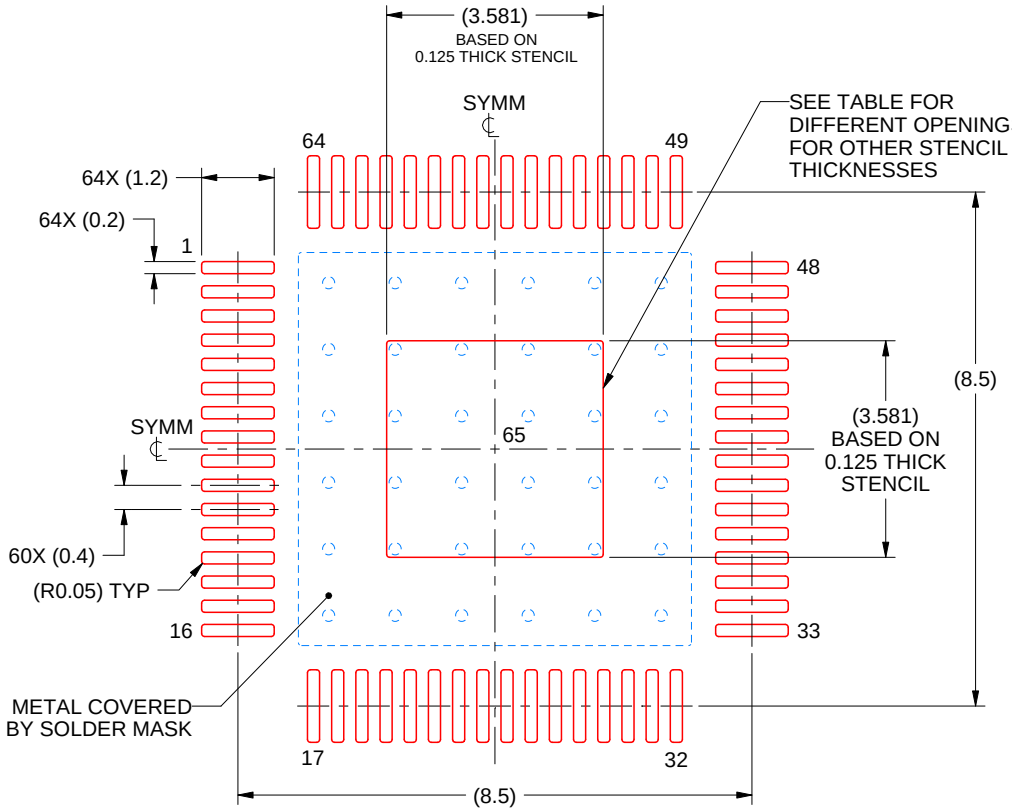


SOLDER MASK DETAILS

4218968/A 12/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.004 X 4.004
0.125	3.581 X 3.581 (SHOWN)
0.150	3.269 X 3.269
0.175	3.026 X 3.026

4218968/A 12/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025