SMPTE-259M/DVB-ASI Scrambler/Controller

Features

- **Fully compatible with SMPTE-259M**
- **Fully compatible with DVB-ASI**
- **Operates from a single +5V supply**
- **44-pin PLCC package**
- **Encodes both 8- and 10-bit parallel digital streams for 27M characters/sec (270 Mbits/sec serial)**
- **Operates with CY7B9234 SMPTE HOTLink® serializer/transmitter**
- **$\times^9 + \times^4 + 1$ scrambler and NRZI encoder may be bypassed for raw data output**

Functional Description

SMPTE-259M Operation

The CY7C9235A is a CMOS integrated circuit designed to encode SMPTE-125M bit-parallel digital characters (or other data formats) using the SMPTE-259M encoding rules. Following encoding, the characters are output as bit-parallel characters ready for serialization. The encoded outputs of the CY7C9235A are designed to be directly mated to a CY7B9234 HOTLink transmitter, which then converts the bit-parallel characters into a SMPTE-259M compatible high-speed serial data stream.

This device performs both TRS (sync) detection and filtering, data scrambling with the SMPTE-259M $\times^9 + \times^4 + 1$ algorithm, and NRZ-to-NRZI encoding. These functions operate at a 27 MHz character rate. For those systems operating with non-SMPTE-259M compliant video streams (or for diagnostic purposes), the scrambler and NRZI encoding functions can be disabled.

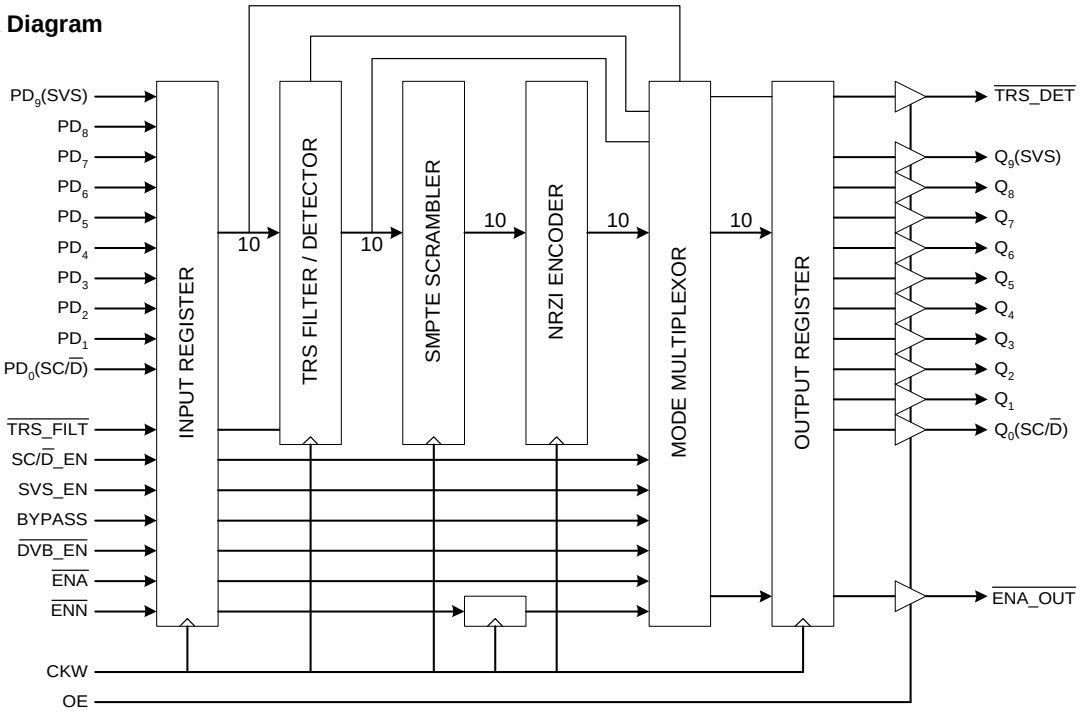
DVB-ASI Operation

The CY7C9235A also contains the necessary multiplexers, control inputs, and outputs, to sequence out a DVB-ASI compliant video stream. DVB-ASI operation is enabled through activation of a single input signal. This allows a single serial output port to support both SMPTE and DVB data streams under software or hardware control.

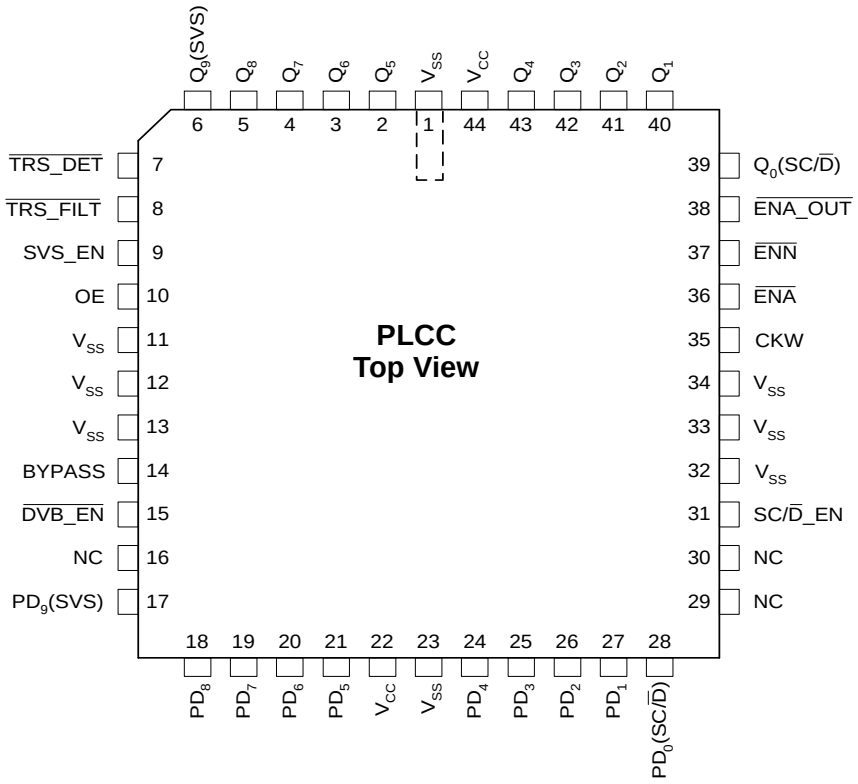
In DVB-ASI mode the CY7C9235A operates with two enable signals ($\overline{ENA}$ and $\overline{ENN}$) to allow data to be presented from either synchronous (clocked) or asynchronous FIFOs. When data is not available, the CY7C9235A ensures that the proper fill character (K28.5) is generated by the attached CY7B9234 serializer.

The CY7C9235A operates from a single +5V supply. It is available in a 44-pin PLCC space saving package.

Logic Block Diagram



Pin Configuration



Pin Descriptions CY7C9235A SMPTE-259M Encoder

Name	I/O	Description
ENA	Input	**Enable Parallel Data**. If ENA is LOW at the rising edge of CKW, the data present on the $PD_{0–9}$ inputs is latched, and routed to the $Q_{0–9}$ outputs. This pin is only interpreted when DVB_EN is active (LOW). If the CY7C9235A is only used in SMPTE-259M mode this signal should be tied to V_{SS}.
ENN	Input	**Enable Next Parallel Data**. If ENN is LOW at the rising edge of CKW, the data present on the $PD_{0–9}$ inputs at the next rising edge of TXCLK is latched, and routed to the $Q_{0–9}$ outputs. This pin is only interpreted when DVB_EN is active (LOW). If the CY7C9235A is only used in SMPTE-259M mode this signal should be tied to V_{SS}.
BYPASS	Input	**Bypass SMPTE Encoding**. BYPASS is ignored if DVB_EN is active (LOW). If BYPASS is HIGH at the rising edge of CKW (and DVB_EN is HIGH), the data latched into the input register is routed around both the SMPTE scrambler and the NRZI encoder and presented to the output register. If BYPASS is LOW at the rising edge of the CKW clock (and DVB_EN is HIGH), the data present in the input register is routed through the SMPTE scrambler and NRZI encoder.
TRS_DET	Output	**TRS Character Detected**. This output indicates when a character used in the TRS sequence is detected in the input register. If the data contains any of the reserved characters of 000–003 or 3FC–3FF in 10-bit hex, the output will be LOW for one clock period. If the character in the input register is any other pattern (or DVB_EN is LOW) this output will remain HIGH.
TRS_FILT	Input	**TRS Character Filter**. This signal controls an internal filter that converts the low-order two bits of all TRS characters to same state as the upper eight bits. This allows a proper 30-bit TRS ID to be generated when the CY7C9235A is operated with 8-bit or non-standard video streams. When this signal is LOW, all characters from 000–003 are converted to 000, and all characters from 3FC–3FF are converted to 3FF. When TRS_FILT is disabled (HIGH), all characters are passed to the scrambler without modification. This signal has no effect when DVB_EN is active (LOW).
SVS_EN	Input	**Send Violation Symbol Enable**. This input is only valid when DVB_EN is active (LOW). If SVS_EN is HIGH and a HIGH input is present on PD_9, Q_9 will also be high on a following clock cycle, forcing the CY7B9234 serializer to generate an invalid 8B/10B character. If SVS_EN is LOW, the level present on PD_9 is ignored and Q_9 is forced to a LOW state.

Pin Descriptions CY7C9235A SMPTE-259M Encoder (continued)

Name	I/O	Description
SC/$\overline{D}$_EN	Input	**Special Character/Data Select Enable**. This input is only valid when $\overline{DVB\_EN}$ is active (LOW). If SC/$\overline{D}$_EN is HIGH and a HIGH input is present on PD_0, Q_0 will also be high on a following clock cycle, forcing the CY7B9234 serializer to generate an 8B/10B control character as selected by the character present on the PD_{8-1} inputs. If SC/$\overline{D}$_EN is LOW, the level present on PD_0 is ignored and Q_0 is forced to a LOW (data only) state.
PD_9(SVS)	Input	**Parallel Data 9 or Send Violation Symbol**. This is the MSB of the input data field. It is latched in the input register at the rising edge of CKW. When $\overline{DVB\_EN}$ is active (LOW) and SVS_EN is HIGH, this latched input is routed to the output register bit Q_9 (SVS). When $\overline{DVB\_EN}$ is active (LOW) and SVS_EN is LOW, output register bit Q_9 (SVS) is forced to a LOW (zero) level. When $\overline{DVB\_EN}$ is inactive (HIGH), this latched input is routed to the scrambler and NRZI encoder.
PD_{8-1}	Input	**Parallel Data 8 through 1**. The signals present at the PD_{8-1} inputs are latched in the input register at the rising edge of CKW. When $\overline{DVB\_EN}$ is HIGH, these signals are the middle eight bits of the SMPTE 10-bit data field, and are then routed to the scrambler and NRZI encoder. When $\overline{DVB\_EN}$ is active (LOW), these signals are full DVB-ASI data bus, and are then routed to the Q_{8-1} outputs.
PD_0(SC/$\overline{D}$)	Input	**Parallel Data 0 or Special Code/Data Select**. This is the LSB of the input data field. It is latched in the input register at the rising edge of CKW. When $\overline{DVB\_EN}$ is active (LOW) and SC/$\overline{D}$_EN is HIGH, this input is routed to output register bit Q_0 (SVS). When $\overline{DVB\_EN}$ is active (LOW) and SC/$\overline{D}$_EN is LOW, output register bit Q_0 (SC/$\overline{D}$) is forced to a LOW (zero) level. When $\overline{DVB\_EN}$ is inactive (HIGH), this input data bit is routed through the input register and the scrambler and NRZI encoder.
Q_9(SVS)	Output	**Output Bit 9**. This is the MSB of the output register. It should be connected directly to the CY7B9234 serializer input signal SVS(Dj).
Q_{8-1}	Output	**Output Bits 8 through 1**. These signals should be connected directly to the CY7B9234 serializer input signals D_{7-0} respectively.
Q_0(SC/$\overline{D}$)	Output	**Output Bit 0**. This is the LSB of the output register. It should be connected directly to the CY7B9234 serializer input signal SC/$\overline{D}$(Da).
$\overline{DVB\_EN}$	Input	**DVB Mode Enable**. This signal is sampled by the rising edge of the CKW clock. If $\overline{DVB\_EN}$ is active (LOW), the data present on the PD_{0-9}, ENA, and $\overline{ENN}$ inputs are latched and routed to the Q_{0-9} and ENA_OUT outputs.
CKW	Input	**Clock Write**. This clock controls all synchronous operations of the CY7C9235A. It operates at the character rate which is equivalent to one tenth the serialized bit-rate. This clock also connects directly to the CKW input of the CY7B9234 serializer.
$\overline{ENA\_OUT}$	Output	**Enable Parallel Data Out**. This output attached directly to the CY7B9234 $\overline{ENA}$ input, and identifies when valid data is available at the CY7C9235A outputs. If used only for SMPTE-259M data streams, this output may be left open, with the $\overline{ENA}$ input to the CY7B9234 directly connected to V_{SS}.
OE	Input	**Output Enable**. When this signal is HIGH all outputs are driven to their normal logic levels. When LOW, all outputs are placed in a High-Z state.
V_{CC}		**Power**.
V_{SS}		**Ground**.

CY7C9235A Description

Input Register

The input register is clocked by the rising edge of CKW. This register captures the data present at the $PD_{0–9}$ inputs on every clock cycle. In addition to the data inputs, all control inputs except OE are also captured at each rising edge of CKW. This includes BYPASS, $\overline{DVB\_EN}$, SVS_EN, SC/D_EN, $\overline{TRS\_DET}$, $\overline{TRS\_FILT}$, $\overline{ENN}$, and $\overline{ENA}$.

TRS Filter

The TRS Filter is used to convert all 8-bit TRS characters (000–003 and 3FC–3FF in 10-bit hex) to their full 10-bit value. If $\overline{TRS\_FILT}$ is active (LOW) and any of these values are detected in the input register, the lower two bits are forced to either zeros or ones respectively. This allows the encoder to be used with both 8- and 10-bit SMPTE character streams.

If $\overline{TRS\_FILT}$ is HIGH, the filter function is disabled and all characters are passed from the input register to the SMPTE scrambler unmodified.

TRS Detector

When operated in SMPTE mode ($\overline{DVB\_EN}$ is HIGH), the TRS detector looks for the most significant eight bits of the input register to be either all ones or all zeros. If either of these values are detected, the $\overline{TRS\_DET}$ output will go LOW following the rising edge of CKW, and remain LOW until a character is detected in the input register that is not all zeros or ones, or $\overline{DVB\_EN}$ is latched LOW.

SMPTE Scrambler

The SMPTE scrambler implements a parallel encoded version of a linear-feedback shift register. It encodes the data present in the input register using the $x^9 + x^4 + 1$ polynomial to increase the transition density of the serial data stream and to decrease the DC-content of the transmitted serial bit stream.

NRZI Encoder

The scrambled data is also fed through an NRZ-to-NRZI encoder. This also increases the transition density of the serial data stream, decreases the DC-content of the transmitted serial bit stream, and makes the serial stream insensitive to polarity inversions.

DVB-ASI Operation

The CY7C9235A is designed to operate in both SMPTE-259M and DVB-ASI environments. When operated in SMPTE-only environments, the DVB control inputs may be tied to either V_{CC} or V_{SS} as needed to place them in a known state. When not used for DVB operation, the $\overline{ENA}$, $\overline{ENN}$, SVS_EN, and SC/D_EN inputs many be tied to either V_{CC} or V_{SS}. $\overline{DVB\_EN}$ must be tied or driven HIGH.

DVB-ASI operation is enabled by asserting $\overline{DVB\_EN}$ LOW. This signal is latched by the rising edge of the CKW clock. When the CY7C9235A is placed in DVB mode, the SMPTE and NRZI encoders are bypassed, and the data latched into the input register is routed directly to the output register.

Error Propagation

For those DVB-ASI implementations that do not require propagation of detected errors, the Q_9 output may be forced to a zero by setting SVS_EN LOW. When SVS_EN is HIGH (and the encoder is in DVB mode) the PD_9 data latched into the input register is routed to the output register and to the CY7B9234 SVS input.

Command Code Generation

The DVB-ASI interface does not normally transmit any command characters other than the K28.5 code that is used both for synchronization and as a fill character when data is not being transmitted. These K28.5 characters may be generated by two methods; by controlling when the CY7C9235A is enabled using the $\overline{ENA}$ and $\overline{ENN}$ inputs, or by placing a C5.0 character on the $PD_{9–0}$ inputs when one of the two enables is active.

If the generation of K28.5 fill characters is to be controlled using the $\overline{ENA}$ or $\overline{ENN}$ inputs, the SC/D_EN input should be driven LOW or connected to V_{SS}. This will insure that the PD_0 data bit is not routed to the output register by forcing the Q_0 output to always be LOW.

If the generation of a K28.5 characters is controlled by transmission of a C5.0 character, the SC/D_EN input must be HIGH to allow the PD_0 input to be propagated to the Q_0 output.

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –40°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to +7.0V

Output Current into Outputs ..... 16 mA

DC Input Voltage ..... –0.5V to +7.0V

Static Discharge Voltage ..... > 2001 V (per MIL-STD-883, Method 3015)

DC Input Current ..... ± 20 mA

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

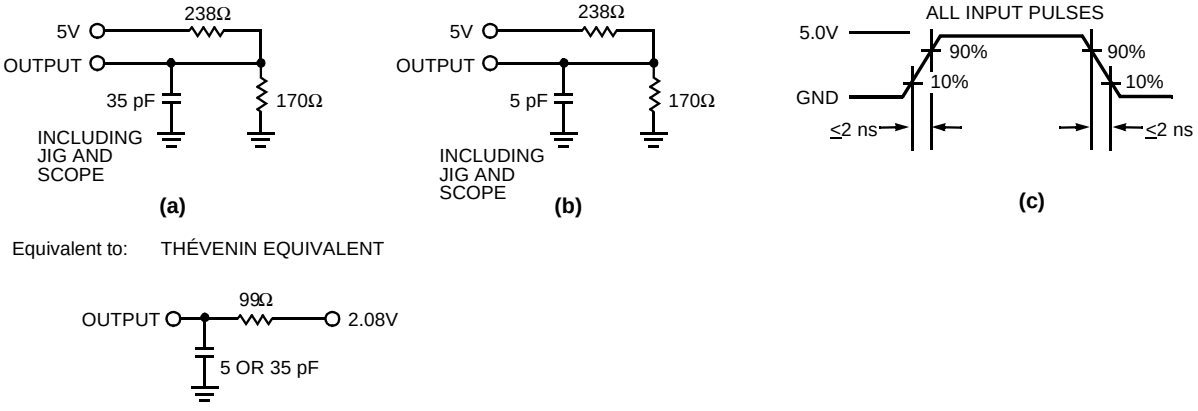
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH} = –3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[2]	2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[2]	–0.5	0.8	V
I_{IX}	Input Load Current	V_I = V_{CC} or V_{SS}	–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or V_{SS}	–50	+50	µA
I_{OS}	Output Short Circuit Current[3,4]	V_{CC} = Max., V_{OUT} = 0.5V	–30	–160	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 5.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 5.0V at f = 1 MHz	12	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz	12	pF

AC Test Loads and Waveforms



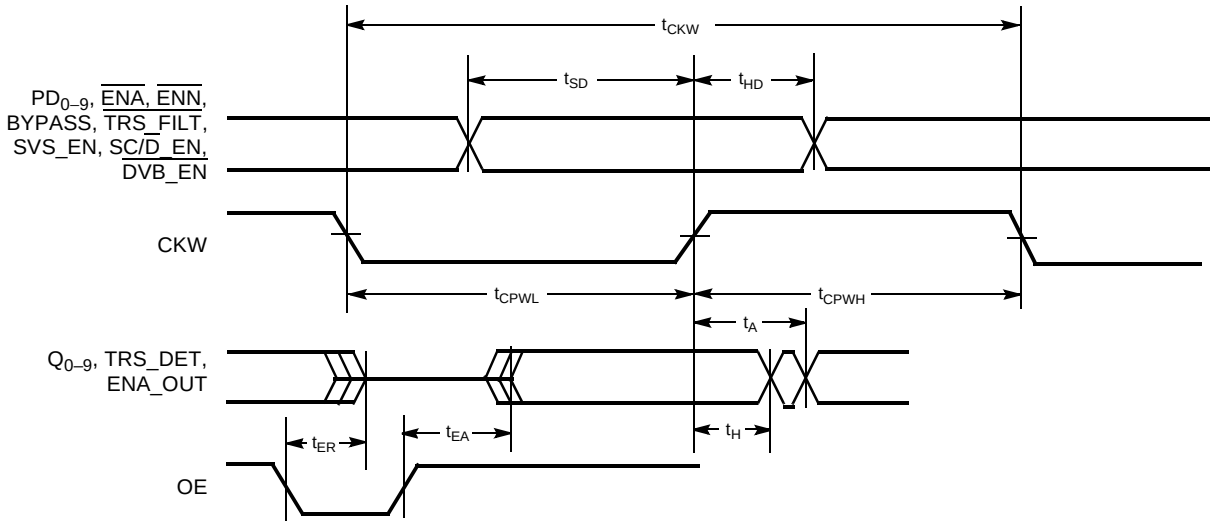
Notes:

1. **Single Power Supply:** The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range [5]

Parameter	Description	Min.	Max.	Unit
t_{SD}	Data Set-Up Time	10		ns
t_{HD}	Data Hold Time	0		ns
t_{CPWH}	CKW Pulse Width HIGH	14.5		ns
t_{CPWL}	CPW Pulse Width LOW	14.5		ns
t_{CKW}	Write Clock Period	30	62.5	ns
t_A	Access Time		10	ns
t_H	Data Output Hold Time From CKW Rise	1		ns
t_{EA}	Input to Output Enable		24	ns
t_{ER}	Input to Output Disable[6]		24	ns

Switching Waveform



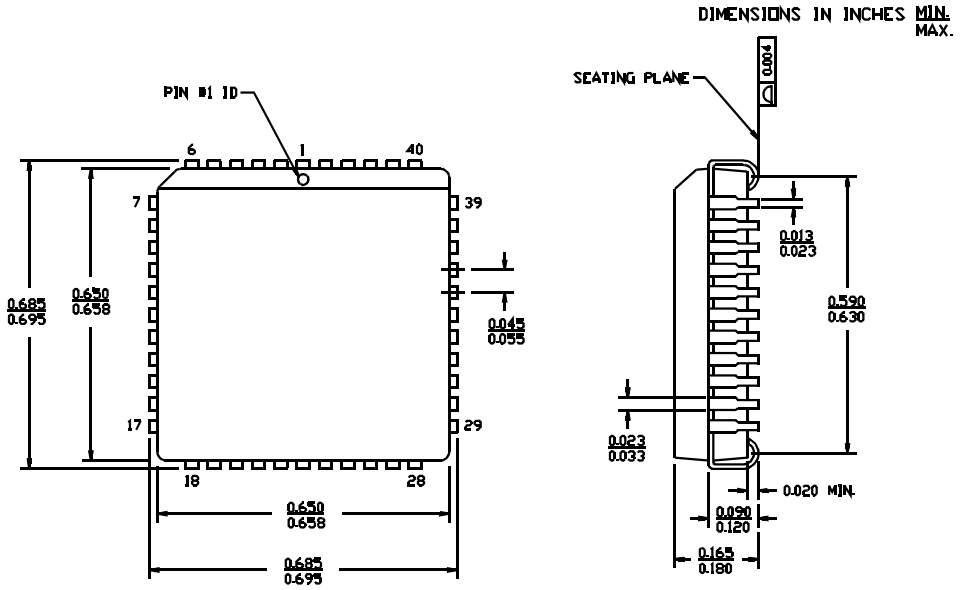
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C9235A	J67	44-pin Plastic Leaded Chip Carrier	Commercial

Notes:
5. All AC parameters are with all outputs switching.
6. Test load (b) used for this parameter. Test load (a) used for all other AC parameters.

Package Diagram

44-Lead Plastic Leaded Chip Carrier J67



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Document History Page

Document Title: CY7C9235A SMPTE-259M/DVB-ASI Scrambler/Controller Document Number: 38-020182				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129111	12/09/03	LAR	Pin-to-pin compatible with CY7C9235