Am6081

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

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DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am8086 and the Am2900 Families
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current outputs
- Output current mode multiplexer with logic selection
- 2-Bit status latch for output select and code select
- Choice of 8 coding formats
- Fast settling current output – 200ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift – ±5ppm/°C
- Wide range multiplying capability –2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- Output range selection with on chip multiplexer
- High speed data latch – 80ns min write time

GENERAL DESCRIPTION

The Am6081 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, a 2-bit status latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

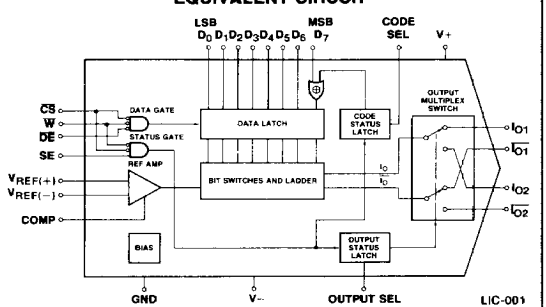
The converter allows a choice of 8 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A pair of high voltage compliance, dual complementary current output channels is provided and is selected by the output status command. The output multiplexer also allows analog bus connection of several converters, range or output load selection, and time-shared operation between D/A and A/D functions. The data and status latches are high speed which makes the Am6081 capable of interfacing with high speed microprocessors. The DE and SE control signals allow the data and status latches to be updated individually or simultaneously.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6081 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

Applications for the Am6081 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT

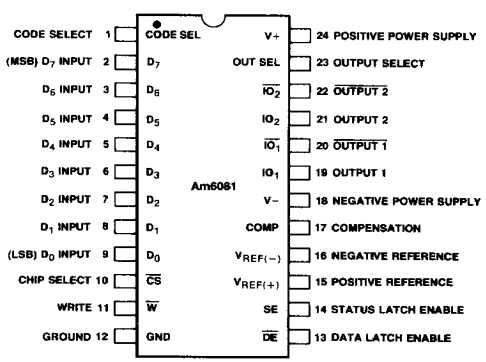


ORDERING INFORMATION*

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	−55°C to +125°C	±.1% ±.19%	AM6081ADM AM6081DM
Hermetic DIP	0°C to +70°C	±.1% ±.19%	AM6081ADC AM6081DC
Molded DIP	0°C to +70°C	±.1% ±.19%	AM6081APC AM6081PC

*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAM
Top View
D-24-1, P-24-1



Note: Pin 1 is marked for orientation.

LIC-002

Am6081 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
$\overline{CS}$	Chip Select – This active low input signal enables the Am6081. Writing into the data or status latches occurs only when the device is selected.
$\overline{DE}$	Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.
SE	Status Latch Enable – This active high input is used to enable the status latches. The $\overline{CS}$, SE, and $\overline{W}$ must be active in order to write into the status latches.
$\overline{W}$	Write – This active low control signal enables the data and status latches when the $\overline{CS}$, $\overline{DE}$, and SE inputs are active.
D_0-D_7	D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.
CODE SEL	Code Select – Input to the CODE SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When CODE SEL latch = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.
OUT SEL	Output Select – Input to the OUT SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When the OUT SEL latch is low, the channel 1 output pair (I_{O1}, $\overline{I_{O1}}$) is selected. When the OUT SEL latch is high, the channel 2 output pair (I_{O2}, $\overline{I_{O2}}$) is selected.
$V_{REF(+)}$ $V_{REF(-)}$	Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.
COMP	Compensation – Frequency compensating terminal for the reference amplifier.
I_{O1}, $\overline{I_{O1}}$ I_{O2}, $\overline{I_{O2}}$	These high impedance current output pairs are selected by the output select latch. I_{O1} and I_{O2} are true outputs and $\overline{I_{O1}}$ and $\overline{I_{O2}}$ are complementary outputs.

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

STATUS LATCH CONTROL

$\overline{CS}$	$\overline{W}$	SE	CODE SEL and OUT SEL Latch
0	0	1	Transparent
X	X	0	Latched
X	1	X	Latched
1	X	X	Latched

CODE SELECT AND OUTPUT SELECT

CODE SEL	OUT SEL	Function
0	–	MSB Inverted (Note 1)
1	–	MSB Non-inverted
–	0	Output Channel 1
–	1	Output Channel 2

X = Don't Care

Note 1. 1 LSB balance current is added to the $\overline{I_O}$ output.

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6081ADM, Am6081DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6081ADC, Am6081DC Am6081APC, Am6081PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs (V_{15}, V_{16})	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{15} to V_{16})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{15})	1.25mA

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	8 bits
Monotonicity	8 bits

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

Parameter	Description	Conditions	Am6081A Min.	Am6081A Typ.	Am6081A Max.	Am6081 Min.	Am6081 Typ.	Am6081 Max.	Unit
	Resolution	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
	Monotonicity	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
D.N.L.	Differential Nonlinearity		–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity		–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{15} = R_{16} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$ or $I_{FS2} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{OSS}	Output Switch Symmetry	$I_{FS1} - I_{FS2}$ or $\overline{I_{FS1}} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current		–	0.01	1.0	–	0.01	2.0	μA
I_{DIS}	Output Disable Current	Output of mpx "Off" Channels	–	0.01	0.05	–	0.01	0.05	μA
I_{RR}	Reference Current Range	V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{16}	Reference Bias Current		–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{15(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5V to +5.5V, V− = −15V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$		V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	
V+	Power Supply Range	I_{REF} = 0.5mA, V_{OUT} = 0V	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−4.5	−18	–	−4.5	
I+	Power Supply Current	V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
P_D	Power Dissipation	V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
		V+ = +5V, V− = −15V	–	160	222	–	160	222	
		V+ = +15V, V− = −15V	–	258	369	–	258	369	

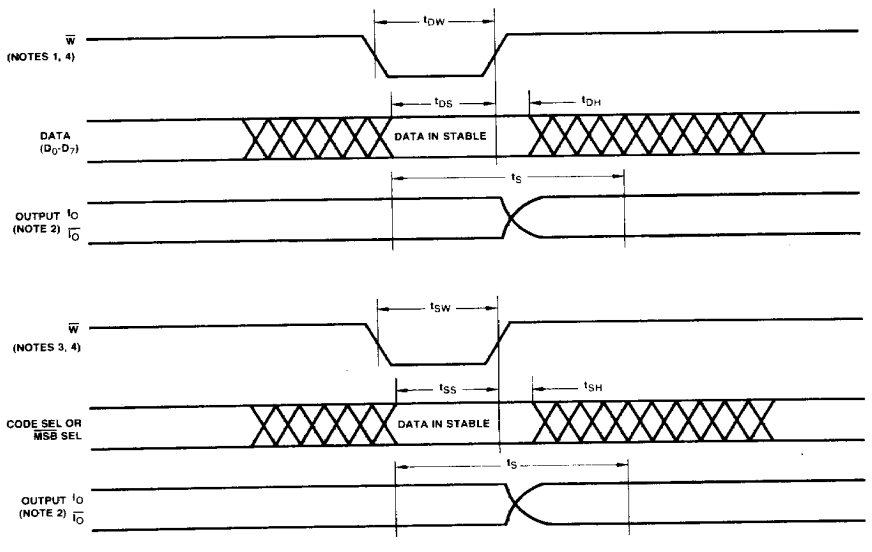
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Typ.	Max.	Military Temp. Grades Min.	Typ.	Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to $\pm$½LSB		200			200		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		90	180		90	180	ns
t_{PHL}		All bits switched			90	180		90	180	
t_{OS}	Output Switch Settling Time		$T_A = 25°C$ to $\pm$1/2LSB of I_{FS}		250			250		ns
t_{OP}	Output Switch Propagation Delay		$T_A = 25°C$, 50% to 50%		150	300		150	300	ns
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns
t_{SH}	Status Hold Time		See timing diagram	10	−70		10	−70		ns
t_{SS}	Status Set Up Time		See timing diagram	200	100		230	100		ns
t_{SW}	Status Write Time		See timing diagram	200	100		230	100		ns

Notes:
1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within $\pm$1/2 LSB. All bits switched on or off.
3. t_{SW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low and SE high, all three signals must be active to enable the latch and any signal going inactive will latch the data.
4. The internal time delays from $\overline{CS}$, $\overline{W}$, SE and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



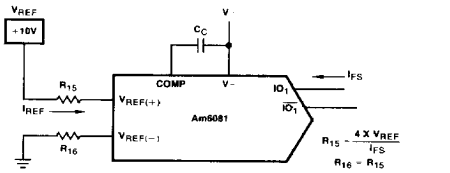
LIC-003

APPLICATION HINTS

1. Reference current and reference resistor

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{15} is:

$$R_{15} = \frac{4 \times 10 \text{ Volt}}{2mA} = 20K\Omega$$



LIC-004

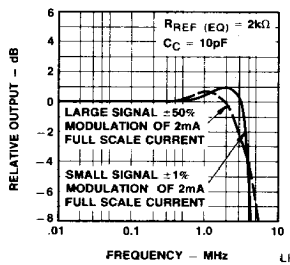
2. Reference amplifier compensation

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

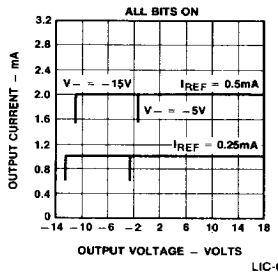
R_{REF} (kΩ)	C_C (pF)
20	100
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response



LIC-005

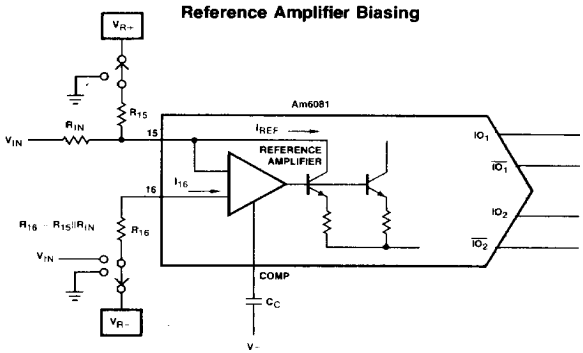
Output Voltage Compliance



LIC-006

A 0.01μF capacitor is recommended for the fixed reference operation.

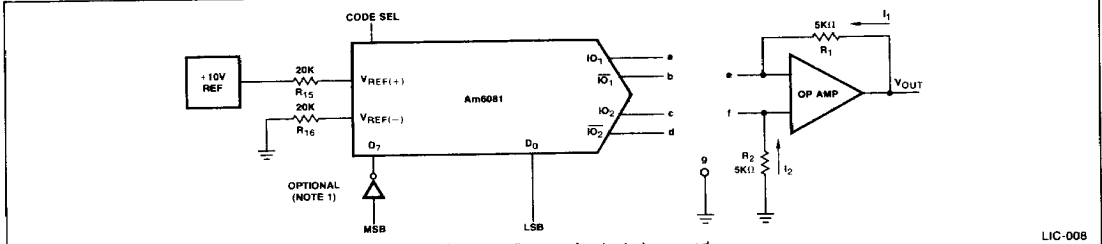
Reference Amplifier Biasing



LIC-007

Reference Configuration	R_{15}	R_{16}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{15}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{15}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{15}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $C = 5pF \times R_{15(EQ)}$ (in kΩ). For $R_{15} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{15} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 15 should be 800Ω or less and an additional resistor may be connected from pin 15 to ground to lower the impedance.



Note: Connect all unused outputs to ground.

CODE FORMAT		CODE SEL	OUT SEL	CONNECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	0	a-e b-g	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
					Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
			1	c-e d-g													
	Complementary binary: one polarity with complementary input code, true zero output.	1	0	a-g b-e	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
					Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
					Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
			1	c-g d-e													
SIGNED MAGNITUDE	Signed magnitude binary: 8 bits + sign reflected code, overlapping true zero output.	1		a-e c-f	Positive full scale	1	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	1	1	1	1	1	1	1	1	0	1.984	.000	9.920
					(+) Zero scale	1	0	0	0	0	0	0	0	0	.000	.000	.000
					(−) Zero scale	0	0	0	0	0	0	0	0	0	.000	.000	.000
					Negative full scale − LSB	0	1	1	1	1	1	1	1	0	.000	1.984	−9.920
					Negative full scale	0	1	1	1	1	1	1	1	1	.000	1.992	−9.960
	Complementary signed magnitude: 8 bits + sign complementary reflected code, overlapping true zero output.	1		b-e d-f	Positive full scale	1	0	0	0	0	0	0	0	0	1.992	.000	9.960
					Positive full scale − LSB	1	0	0	0	0	0	0	0	1	1.984	.000	9.920
					(+) Zero scale	1	1	1	1	1	1	1	1	1	.000	.000	.000
					(−) Zero scale	0	1	1	1	1	1	1	1	1	.000	.000	.000
					Negative full scale − LSB	0	0	0	0	0	0	0	0	1	.000	1.984	−9.920
					Negative full scale	0	0	0	0	0	0	0	0	0	.000	1.992	−9.960
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
					(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
					(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
			1	c-e d-f	Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.880
					(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
					(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.880
			1	c-e d-f	Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
					+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
					− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.080
			1	c-e d-f	Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.920
					Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.000
	2's complement: offset half scale true zero output MSB complemented.	0	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
					+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
					−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.080
			1	c-e d-f	Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.920
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.000

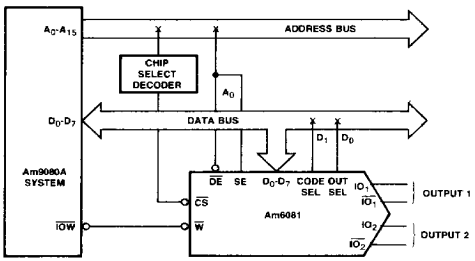
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of the two features is desired for these codes.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.
2. The sign on any of the sign-magnitude codes may be changed by reversing the output terminal pair.
3. The polarity of the unipolar codes may be changed by driving the opposite side of the balanced load.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM: SEPARATE UPDATE OF DATA AND STATUS



SELECT OUTPUT PORT 1

MVI A, 2 : SET STATUS TO 0 (SELECT OUTPUT 1)
OUT 1 : SEND STATUS
MOV A, M : GET DATA FROM MEMORY
OUT 0 : SEND DATA

SELECT OUTPUT PORT 2

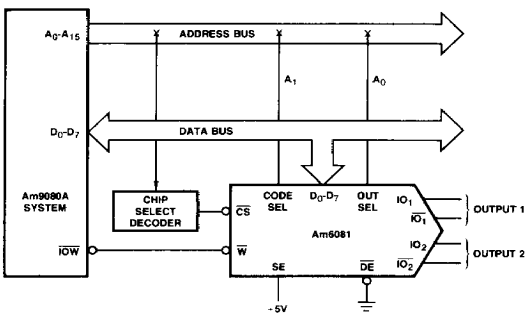
MVI A, 3 : SET STATUS TO 1 (SELECT OUTPUT 2)
OUT 1 : SEND STATUS
MOV A,M : GET DATA FROM MEMORY
OUT 0 : SEND DATA

SELECT OUTPUT PORT 2 AND 2's COMPLEMENT CODE

MVI A, 1 : SET STATUS TO 3 (OUTPUT 2, MSB COMP)
OUT 1 : SEND STATUS
MOV A, M : GET DATA FROM MEMORY
OUT 0 : SEND DATA

LIC-009

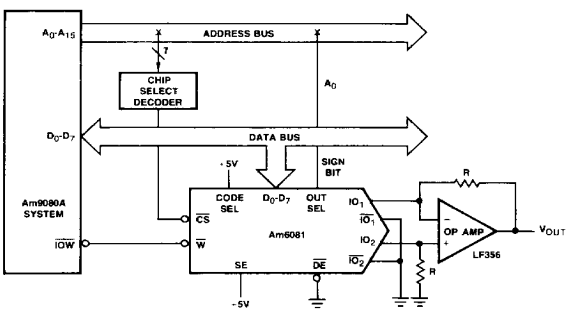
Am9080A DATA SYSTEM: SIMULTANEOUS UPDATE OF DATA AND STATUS



MOV A, M : GET DATA IN ACCUMULATOR
OUT 0 : OUTPUT DATA TO PORT 1, 2'S COMPLEMENT
OUT 1 : OUTPUT DATA TO PORT 2, 2'S COMPLEMENT
OUT 2 : OUTPUT DATA TO PORT 1, STRAIGHT BINARY
OUT 3 : OUTPUT DATA TO PORT 2, STRAIGHT BINARY

LIC-010

Am9080A DATA SYSTEM: 8-BIT PLUS SIGN CONVERSION

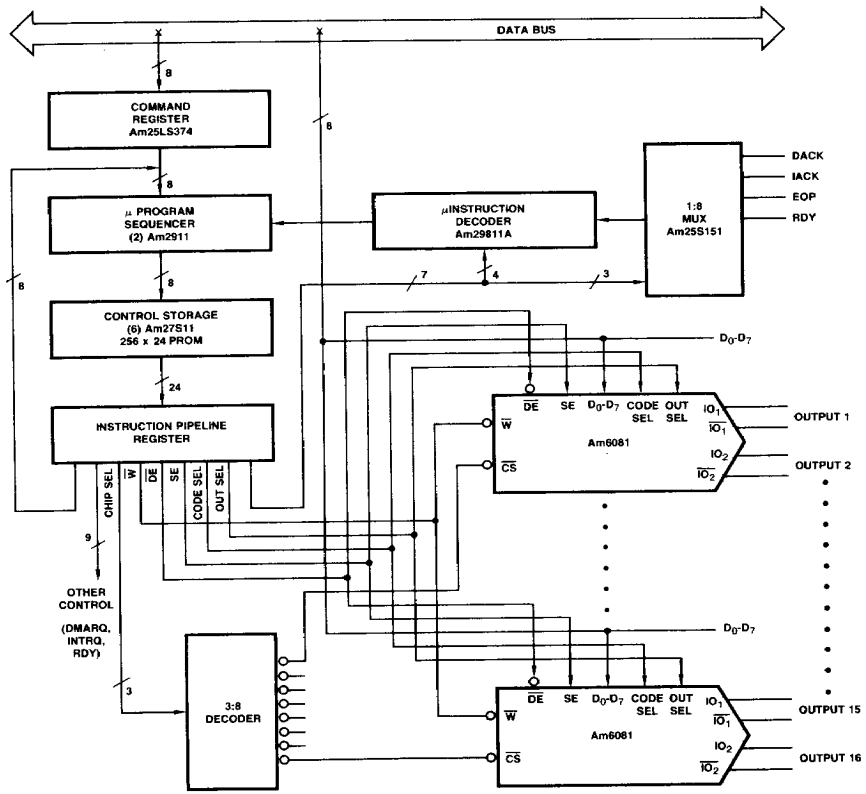


MOV A, M : LOAD MAGNITUDE (8-BITS)
OUT 0 : SEND POSITIVE OUTPUT
OUT 1 : SEND NEGATIVE OUTPUT

LIC-011

SYSTEM APPLICATIONS (Cont.)

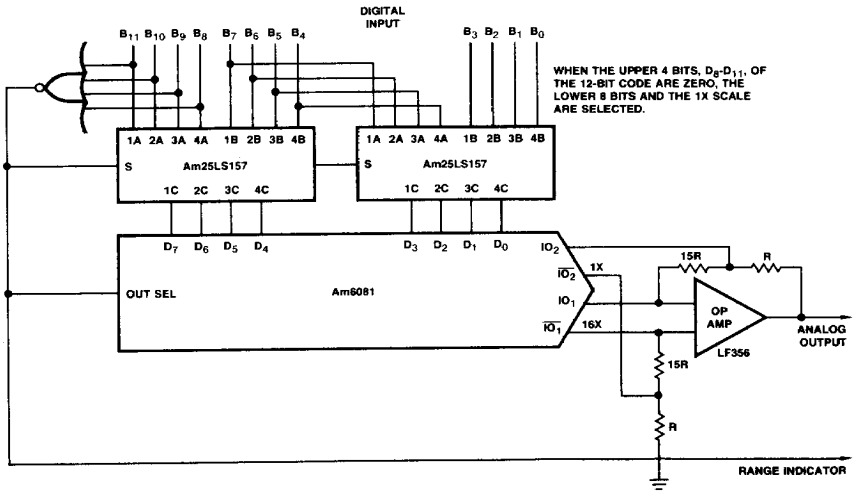
Am2900 DATA SYSTEM: MULTIPLE ANALOG OUTPUTS



LIC-012

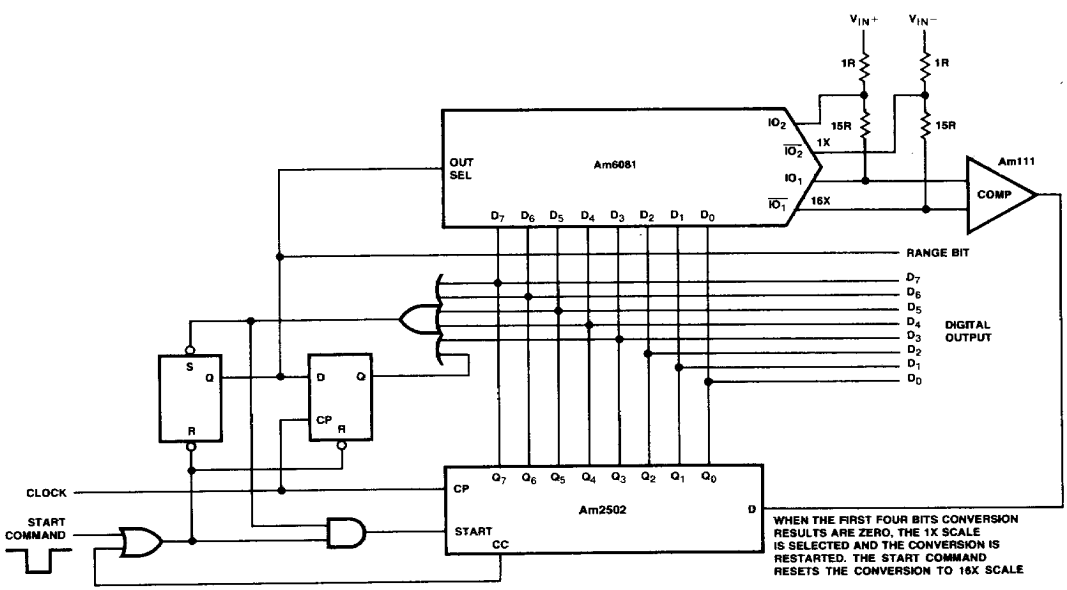
SYSTEM APPLICATIONS (Cont.)

D/A CONVERSION WITH 12-BIT DYNAMIC RANGE



LIC-013

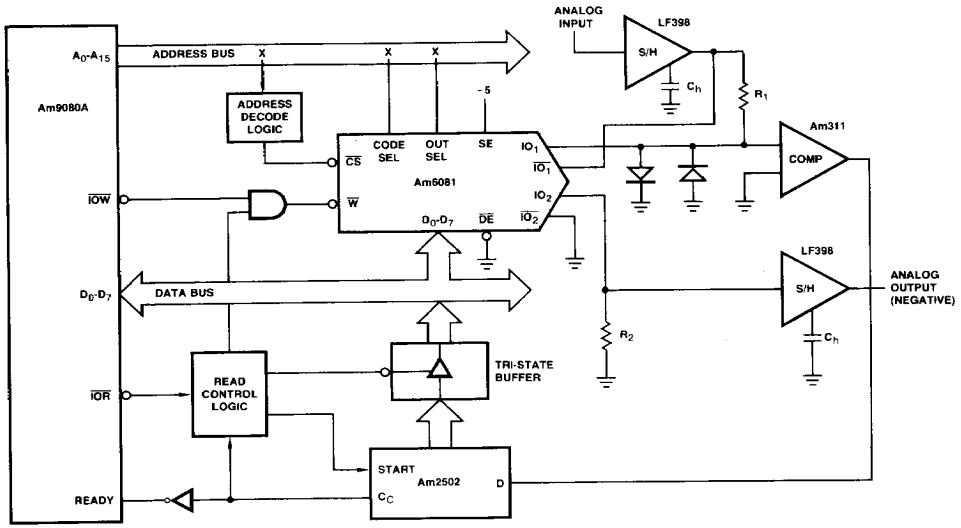
A/D CONVERSION WITH AUTO RANGING AND DIFFERENTIAL INPUT



LIC-014

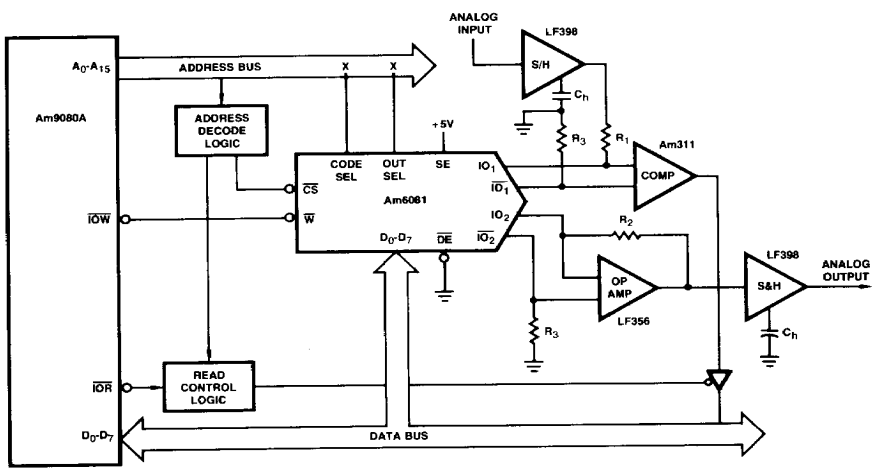
SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL TRANSCEIVER WITH HARDWARE CONTROLLED SUCCESSIVE APPROXIMATION A/D CONVERSION



LIC-015

ANALOG/DIGITAL TRANSCEIVER WITH SOFTWARE CONTROLLED A/D CONVERSION



LIC-016

Am9080A SOFTWARE FOR A/D AND D/A CONVERSION USING Am6081

```
SEQ     SOURCE STATEMENT
 0 PORT1    EQU 00H
 1 PORT3    EQU 02H
 2 PORT2    EQU 01H
 3          ORG 3E50H
 4 START:   LXI SP,STAKS-16   ;INITIAL STAKS POINTER
 5 SAMPLE:  CALL ADCON        ;CALL A/D CONVERSATION
 6          CMA
 7          CALL DACON        ;CALL D/A CONVERSION
 8          JMP SAMPLE        ;NEXT SAMPLE
 9 ADCON:   XRA A             :CLEAR ACC
10          MOV D,A           ;CLEAR D REG
11          STC               ;SET CARRY
12          RAR               ;SET BIT 7 TO 1
13          MOV B,A           ;STORE TEST BIT AT B REGISTER
14 LOOP:    MOV E,A           ;STORE TEST WORD
15          CMA
16          OUT PORT1         ;OUTPUT TO A/D
17          IN PORT3          ;INPUT FROM COMP
18          CMA
19          CRA A             ;SET SIGN FLAG
20          JM NEXT           ;IF SMALLER GO TO NEXT BIT
21          MOV D,E           ;SAVE RESULT
22 NEXT:    MOV A,B           ;GET NEXT TRIAL BIT
23          RAR               ;SHIFT RIGHT ONCE
24          RC                ;RETURN ON CARRY
25          MOV B,A           ;STORE TEST BIT
26          ADD D             ;ACCUMULATE RESULT
27          JMP LOOP          ;TRY NEXT BIT
28 DACON:   OUT PORT 2        ;OUTPUT TO D/A
29          MVI C,05H         ;LOAD C REG WITH TIME
30          DCR C             ;TIME DELAY
31          RZ                ;RETURN
32 FILT:    RET
33 STAKS:   DS 16
34          END START
```

ADVANCED MICRO DEVICES DATA CONVERSION PRODUCTS

Digital to Analog Converters

AmDAC-08	– 8-Bit High Speed Multiplying D/A Converter
Am1508/1408	– 8-Bit Multiplying D/A Converter
Am6070	– 8-Bit Companding D/A Converter for Control Systems (μ-law)
Am6072	– 8-Bit Companding D/A Converter for Telecommunications (μ-law)
Am6080	– 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
Am6081	– 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
*Am6689	– 8-Bit, Ultra High Speed D/A Converter (ECL)
*Am6012	– 12-Bit High Speed Multiplying D/A Converter

Analog to Digital Converters

*Am6688	– 4-Bit Quantizer (Ultra High Speed A/D Converter)

Successive Approximation Registers

Am2502	– 8-Bit Successive Approximation Registers
Am2503	– 8-Bit Successive Approximation Registers
Am2504	– 12-Bit Successive Approximation Registers

Sample and Hold Amplifiers

LF198/398	–Monolithic Sample and Hold Amplifier
*Am6098	–Precision Sample and Hold Amplifier

Comparators

LM111/311	– Precision Voltage Comparator
LM119/319	– Dual Comparator
Am686	– High Speed Voltage Comparator

High Speed Operational Amplifiers

Am118/318	– High Speed Operational Amplifier
LF155/156/157	– JFET Input Operational Amplifiers
LF355/356/357	– JFET Input Operational Amplifiers

* To be announced.

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Data Transceiver
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Signal Processing

CRT Displays
Floating Point Analog Processors
IF Gain Control
Four Quadrant Multiplexer
8 x 8 Digital Multiplication
Line Driver

A/D Converters

Ratiometric ADC
Differential Input ADC
Multiple Input Range ADC
Two Channel ADC
Microprocessor Controlled ADC

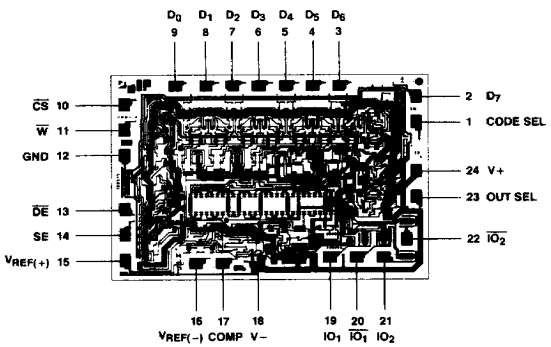
Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC
Two Channel DAC
Multiple Output Range DAC

Metallization and Pad Layout



DIE SIZE: 0.083" X 0.121"