

CY74FCT825T

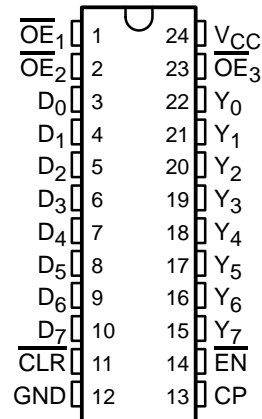
8-BIT BUS-INTERFACE REGISTER

WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29825
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- 64-mA Output Sink Current
32-mA Output Source Current
- High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops
- Buffered Common Clock-Enable (\overline{EN}) and Asynchronous-Clear (\overline{CLR}) Inputs
- 3-State Outputs

Q PACKAGE
(TOP VIEW)



description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT825T is an 8-bit buffered register with all the CY74FCT823T controls, plus multiple enables (\overline{OE}_1 , \overline{OE}_2 , \overline{OE}_3) to allow multiuser control of the interface, e.g., \overline{CS} , DMA, and RD/WR. This device is ideal for use as an output port requiring high I_{OL}/I_{OH} .

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT825CTQCT	FCT825C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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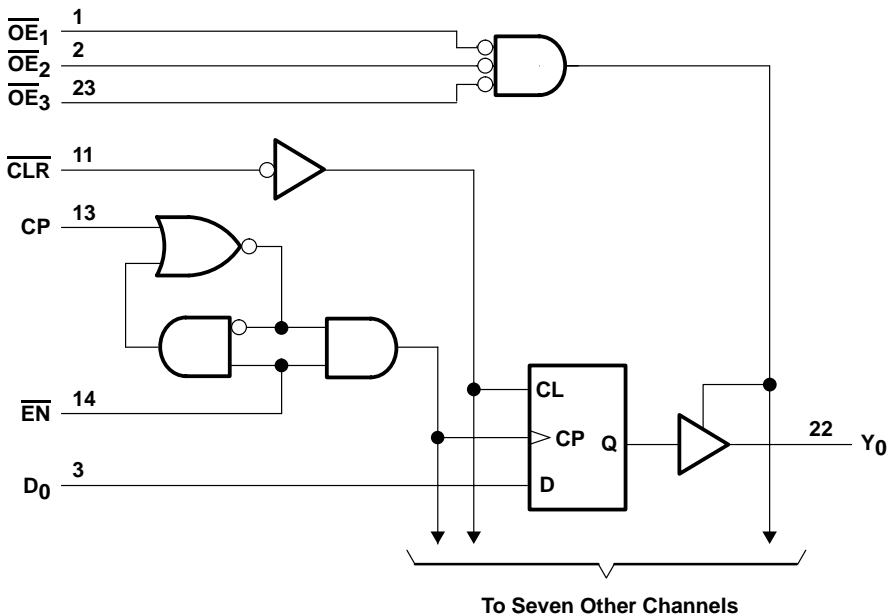
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PIN DESCRIPTION		
NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is low and $\overline{\text{OE}}$ is low, Q outputs are low. When $\overline{\text{CLR}}$ is high, data can be entered into the register.
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{\text{EN}}$	I	Clock enable. When $\overline{\text{EN}}$ is low, data on the D input is transferred to the Q output on the low-to-high clock transition. When $\overline{\text{EN}}$ is high, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output control. When $\overline{\text{OE}}$ is high, the Y outputs are in the high-impedance state. When $\overline{\text{OE}}$ is low, true register data is present at the Y outputs.

FUNCTION TABLE							
INPUTS					INTERNAL OUTPUTS		FUNCTION
OE	CLR	EN	D	CP	Q	Y	
H	H	L	L	↑	L	Z	Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = High logic level, L = Low logic level, X = Don't care, NC = No change, ↑ = Low-to-high transition, Z = High-impedance state

logic diagram (positive logic)



CY74FCT825T
8-BIT BUS-INTERFACE REGISTER
WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note1)	61°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–32	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



CY74FCT825T

8-BIT BUS-INTERFACE REGISTER

WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V, I _{IN} = −18 mA		−0.7		−1.2	V
V _{OH}	V _{CC} = 4.75 V	I _{OH} = −32 mA	2		V	
		I _{OH} = −15 mA	2.4	3.3		
V _{OL}	V _{CC} = 4.75 V, I _{OL} = 64 mA		0.3		0.55	V
V _{hys}	All inputs		0.2			V
I _I	V _{CC} = 5.25 V,	V _{IN} = V _{CC}			5	μA
I _{IH}	V _{CC} = 5.25 V,	V _{IN} = 2.7 V			±1	μA
I _{IL}	V _{CC} = 5.25 V,	V _{IN} = 0.5 V			±1	μA
I _{OZH}	V _{CC} = 5.25 V,	V _{OUT} = 2.7 V			10	μA
I _{OZL}	V _{CC} = 5.25 V,	V _{OUT} = 0.5 V			−10	μA
I _{OS} ‡	V _{CC} = 5.25 V,	V _{OUT} = 0 V	−60	−120	−225	mA
I _{off}	V _{CC} = 0 V,	V _{OUT} = 4.5 V			±1	μA
I _{CC}	V _{CC} = 5.25 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} − 0.2 V	0.1		0.2	mA
ΔI _{CC}	V _{CC} = 5.25 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open		0.5		2	mA
I _{CCD} ¶	V _{CC} = 5.25 V, One bit switching at 50% duty cycle, Outputs open, OE = EN = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V		0.06		0.12	mA/MHz
I _C [#]	V _{CC} = 5.25 V, Outputs open, OE = EN = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V	0.7	1.4	mA
			V _{IN} = 3.4 V or GND	1.2	3.4	
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V	1.6	3.2	
			V _{IN} = 3.4 V or GND	3.9	12.2	
C _i			5		10	pF
C _o			9		12	pF

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY74FCT825T
8-BIT BUS-INTERFACE REGISTER
WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST LOAD	CY74FCT825AT		CY74FCT825BT		CY74FCT825CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CP	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	7		6		6		ns
		$\overline{\text{CLR}}$ low		6		6		6		
t_{su}	Setup time, before CP \uparrow	Data	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	4		3		3		ns
		$\overline{\text{EN}}$		4		3		3		
t_h	Hold time, after CP \uparrow	Data	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	2		1.5		1.5		ns
		$\overline{\text{EN}}$		2		0		0		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ before CP \uparrow	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	6		6		6		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT825AT		CY74FCT825BT		CY74FCT825CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	10		7.5		6		ns
t_{PHL}				10		7.5		6		
t_{PLH}	CP	Y	$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$	20		15		12.5		ns
t_{PHL}				20		15		12.5		
t_{PLH}	$\overline{\text{CLR}}$	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	14		9		8		ns
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	12		8		7		ns
t_{PZL}				12		8		7		
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$	23		15		12.5		ns
t_{PZL}				23		15		12.5		
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 5 \text{ pF}$, $R_L = 500 \Omega$	7		6.5		6		ns
t_{PLZ}				7		6.5		6		
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	8		7.5		6.5		ns
t_{PLZ}				8		7.5		6.5		

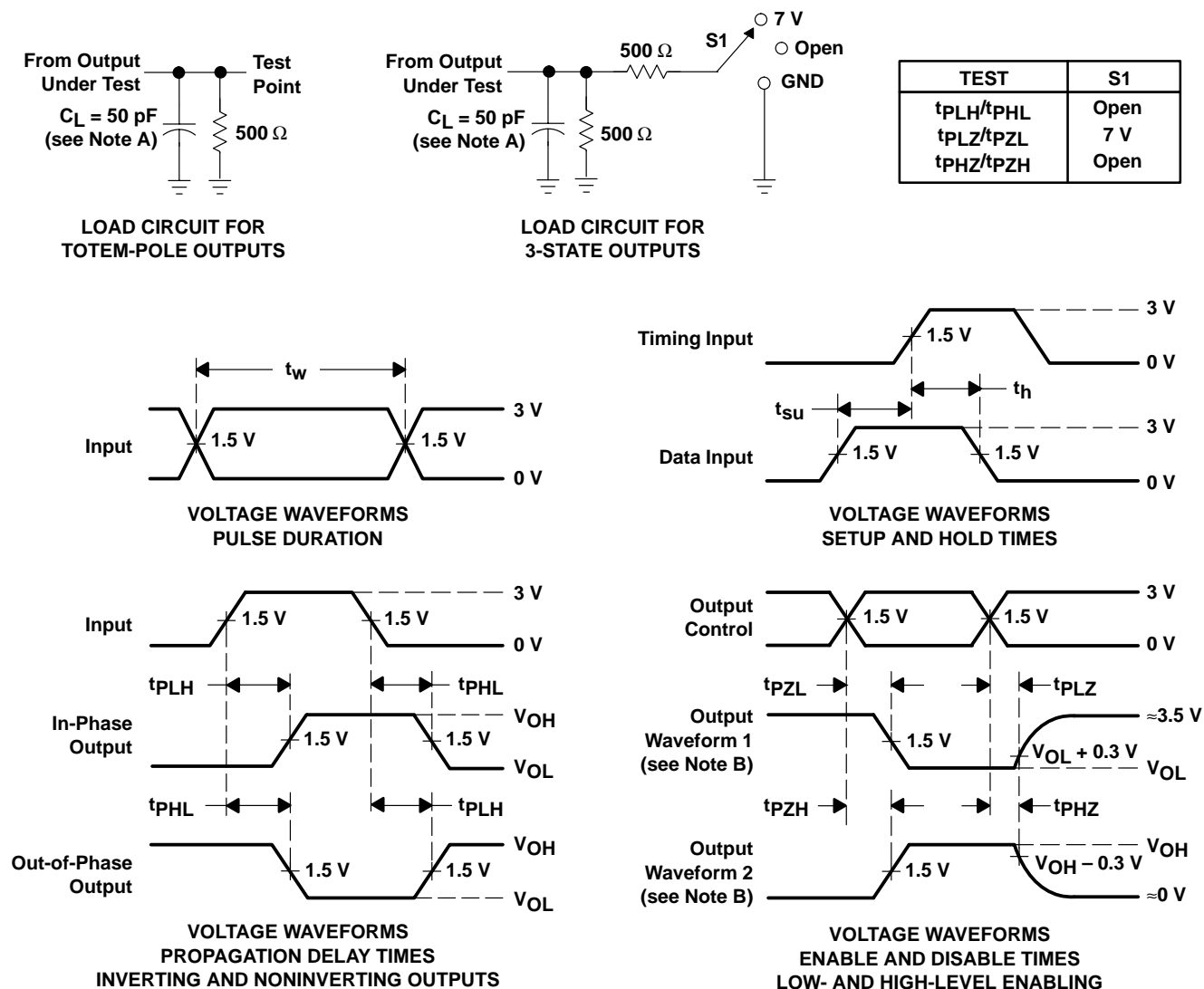
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WITH 3-STATE OUTPUTS

SCCS070A – OCTOBER 2001 – REVISED NOVEMBER 2001

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT825ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT825A	Samples
CY74FCT825CTQCT	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT825C	Samples
CY74FCT825CTQCTG4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT825C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT825CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT825CTQCT	SSOP	DBQ	24	2500	367.0	367.0	38.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

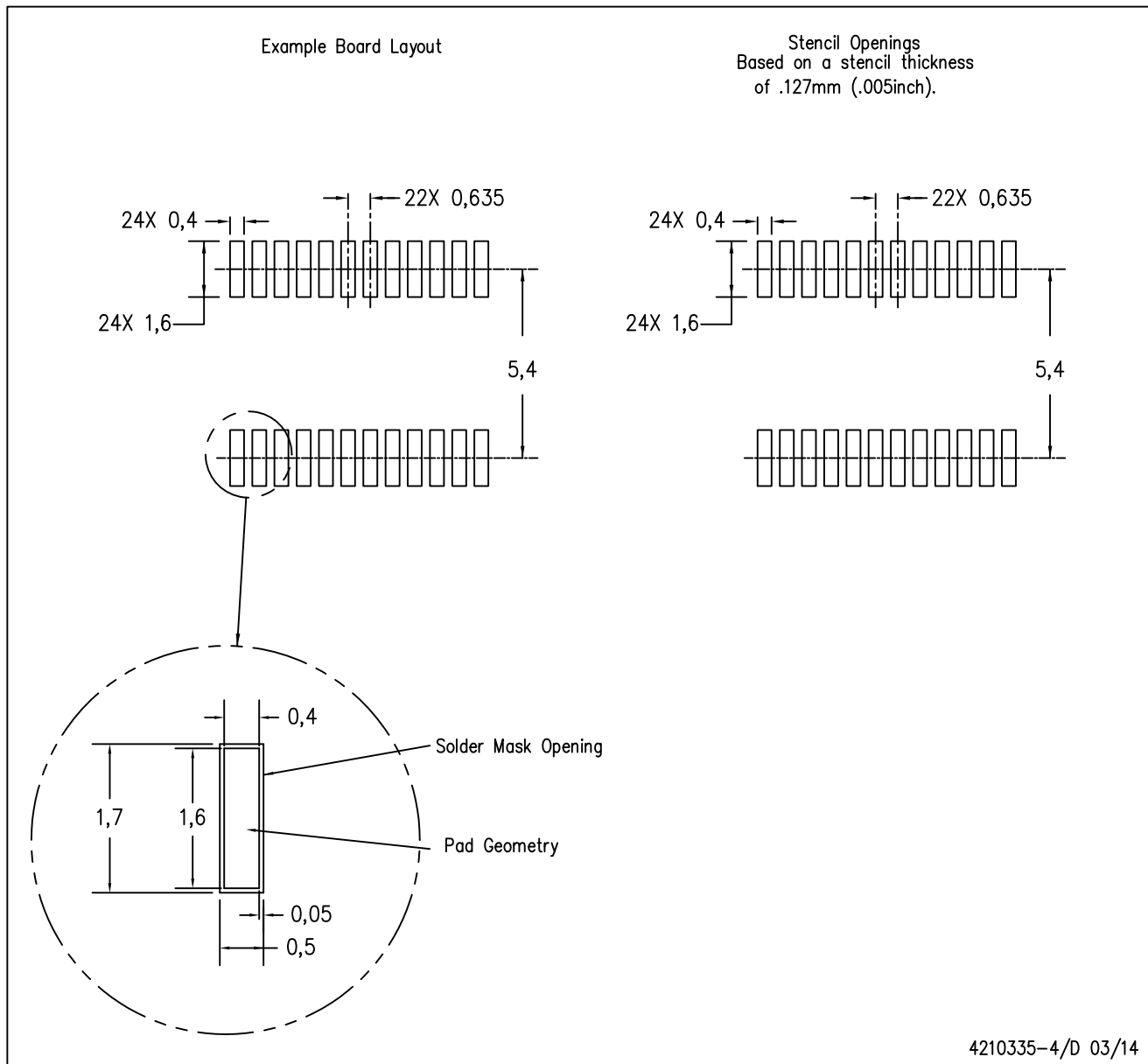
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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