



**CYPRESS** *PRELIMINARY*

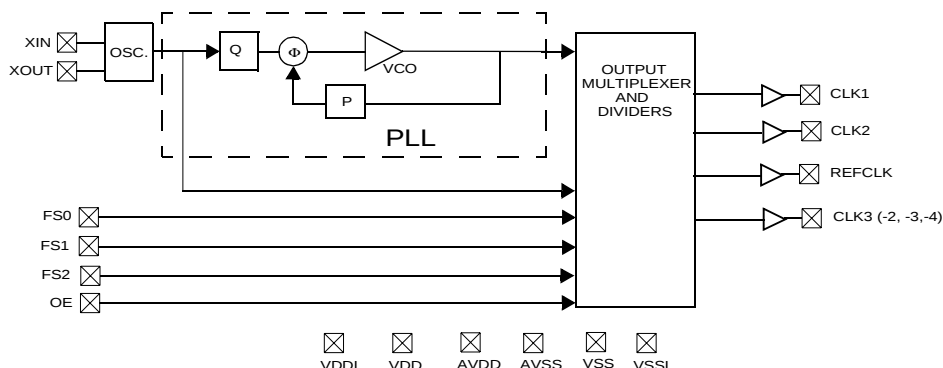
**CY24206**

# MediaClock™ DTV, STB Clock Generator

| Features                            | Benefits                                                     |
|-------------------------------------|--------------------------------------------------------------|
| • Integrated phase-locked loop      | Internal PLL with up to 400-MHz internal operation           |
| • Low-jitter, high-accuracy outputs | Meets critical timing requirements in complex system designs |
| • 3.3V operation                    | Enables application compatibility                            |

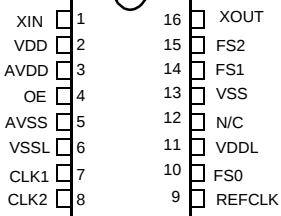
| Part Number | Outputs | Input Frequency | Output Frequency Range                                                                                                                                                                                                                        |
|-------------|---------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CY24206-1   | 3       | 27 MHz          | 1 copy 27-MHz reference clock output<br>1 copy of 81-/81.081-/74.175-/74.250-MHz (frequency selectable)<br>1 copy of 27-/27.027-/24.725-/24.75-MHz (frequency selectable)                                                                     |
| CY24206-2   | 4       | 27 MHz          | 1 copy 27-MHz reference clock output<br>1 copy of 81-/81.081-/74.175-/74.250-MHz (frequency selectable)<br>1 copy of 27-/27.027-/24.725-/24.75-MHz (frequency selectable)<br>1 copy of 27-/27.027-/74.175-/74.25-MHz (frequency selectable)   |
| CY24206-3   | 4       | 27 MHz          | 1 copy 27-MHz reference clock output<br>1 copy of 81-/81.081-/74.17582-/74.250-MHz (frequency selectable)<br>1 copy of 27-/27.027-/24.725-/24.75-MHz (frequency selectable)<br>1 copy of 27-/27.027-/74.175-/74.25-MHz (frequency selectable) |
| CY24206-4   | 4       | 27 MHz          | 1 copy 27-MHz reference clock output<br>1 copy of 81-/81.081-/74.17582-/74.250-MHz (frequency selectable)<br>1 copy of 27-/27.027-/24.725-/24.75-MHz (frequency selectable)<br>1 copy of 27-/27.027-/74.175-/74.25-MHz (frequency selectable) |

## Logic Block Diagram

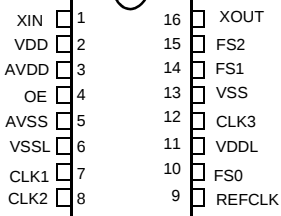


## Pin Configurations

### CY24206-1 16-pin TSSOP



### CY24206-2,3,4 16-pin TSSOP



**Frequency Select Options**

| FS2 | FS1 | FS0 | CLK1 (-1,-2) | CLK1 (-3,-4) | CLK2            | CLK3 (-2, -3,-4) | REFCLK | Units |
|-----|-----|-----|--------------|--------------|-----------------|------------------|--------|-------|
| 0   | 0   | 0   | 81           | 81           | 27 (CLK1/3)     | 27 (CLK1/3)      | 27     | MHz   |
| 0   | 0   | 1   | 81.081       | 81.081       | 27.027 (CLK1/3) | 27.027 (CLK1/3)  | 27     | MHz   |
| 0   | 1   | 0   | 74.175       | 74.17582     | 24.725 (CLK1/3) | 74.17582 (CLK1)  | 27     | MHz   |
| 0   | 1   | 1   | 74.250       | 74.25        | 24.75 (CLK1/3)  | 74.25 (CLK1)     | 27     | MHz   |
| 1   | 0   | 0   | 81           | 81           | 27              | 27 (CLK1/3)      | 27     | MHz   |
| 1   | 0   | 1   | 81.081       | 81.081       | 27              | 27.027 (CLK1/3)  | 27     | MHz   |
| 1   | 1   | 0   | 74.175       | 74.1758      | 27              | 74.175 (CLK1)    | 27     | MHz   |
| 1   | 1   | 1   | 74.250       | 74.25        | 27              | 74.25 (CLK1)     | 27     | MHz   |

**Pin Description**

| Name             | Pin Number | Description                                                            |
|------------------|------------|------------------------------------------------------------------------|
| XIN              | 1          | Reference Crystal Input.                                               |
| V <sub>DD</sub>  | 2          | Voltage Supply.                                                        |
| AV <sub>DD</sub> | 3          | Analog Voltage Supply.                                                 |
| OE               | 4          | Output Enable, weak internal pull-up. 0 = outputs off, 1 = outputs on. |
| AV <sub>SS</sub> | 5          | Analog Ground.                                                         |
| V <sub>SSL</sub> | 6          | VDDL Ground.                                                           |
| CLK1 (-1,-2)     | 7          | 81-/81.081-/74.175-/74.250-MHz Clock Output (frequency selectable).    |
| CLK1 (-3,-4)     | 7          | 81-/81.081-/74.17582-/74.25-MHz Clock Output (frequency selectable).   |
| CLK2             | 8          | 27-/27.027-/24.725-/24.75-MHz Clock Output (frequency selectable).     |
| REFCLK           | 9          | Reference Clock Output.                                                |
| FS0              | 10         | Frequency Select 0, weak internal pull-up.                             |
| V <sub>DDL</sub> | 11         | Voltage Supply.                                                        |
| N/C (-1)         | 12         | No Connect.                                                            |
| CLK3 (-2,-3,-4)  | 12         | 27-/27.027-/74.175-/74.25-MHz Clock Output (frequency selectable).     |
| VSS              | 13         | Ground.                                                                |
| FS1              | 14         | Frequency Select 1, weak internal pull-up.                             |
| FS2              | 15         | Frequency Select 2, weak internal pull-up.                             |
| XOUT             | 16         | Reference Crystal Output.                                              |

**Absolute Maximum Conditions**

| Parameter        | Description              | Min.                   | Max.                   | Unit |
|------------------|--------------------------|------------------------|------------------------|------|
| V <sub>DD</sub>  | Supply Voltage           | -0.5                   | 7.0                    | V    |
| V <sub>DDL</sub> | I/O Supply Voltage       |                        | 7.0                    | V    |
| T <sub>J</sub>   | Junction Temperature     |                        | 125                    | °C   |
|                  | Digital Inputs           | AV <sub>SS</sub> - 0.3 | AV <sub>DD</sub> + 0.3 | V    |
|                  | Electro-Static Discharge | 2                      |                        | kV   |

**Recommended Operating Conditions**

| Parameter                                            | Description           | Min.  | Typ. | Max.  | Unit |
|------------------------------------------------------|-----------------------|-------|------|-------|------|
| V <sub>DD</sub> /AV <sub>DDL</sub> /V <sub>DDL</sub> | Operating Voltage     | 3.135 | 3.3  | 3.465 | V    |
| T <sub>A</sub>                                       | Ambient Temperature   | 0     |      | 70    | °C   |
| C <sub>LOAD</sub>                                    | Max. Load Capacitance |       |      | 15    | pF   |
| f <sub>REF</sub>                                     | Reference Frequency   |       | 27   |       | MHz  |

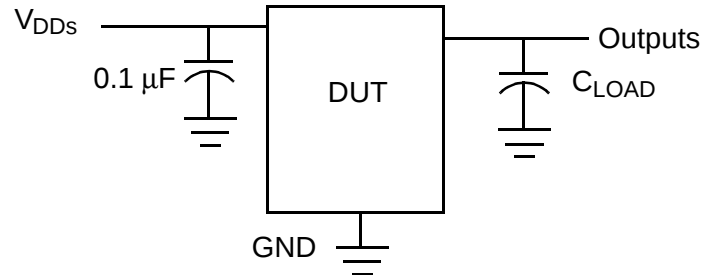
## DC Electrical Specifications

| Parameter <sup>[1]</sup> | Name                       | Description                                         | Min. | Typ. | Max. | Unit       |
|--------------------------|----------------------------|-----------------------------------------------------|------|------|------|------------|
| $I_{OH}$                 | Output High Current        | $V_{OH} = V_{DD} - 0.5$ , $V_{DD}/V_{DDL} = 3.3V$   | 12   | 24   |      | mA         |
| $I_{OL}$                 | Output Low Current         | $V_{OL} = 0.5$ , $V_{DD}/V_{DDL} = 3.3V$            | 12   | 24   |      | mA         |
| $I_{IH}$                 | Input High Current         | $V_{IH} = V_{DD}$                                   | –    | 5    | 10   | $\mu A$    |
| $I_{IL}$                 | Input Low Current          | $V_{IL} = 0V$                                       | –    | –    | 50   | $\mu A$    |
| $V_{IH}$                 | Input High Voltage         | CMOS levels, 70% of $V_{DD}$                        | 0.7  |      |      | VDD        |
| $V_{IL}$                 | Input Low Voltage          | CMOS levels, 30% of $V_{DD}$                        |      |      | 0.3  | VDD        |
| $I_{VDD}$                | Supply Current             | $AV_{DD}/V_{DD}$ Current                            |      |      | 25   | mA         |
| $I_{VDDL}$               | Supply Current             | $V_{DDL}$ Current                                   |      |      | 20   | mA         |
| $R_{UP}$                 | Pull-up resistor on Inputs | $V_{DD} = 3.14$ to $3.47V$ , measured $V_{IN} = 0V$ |      | 100  | 150  | k $\Omega$ |

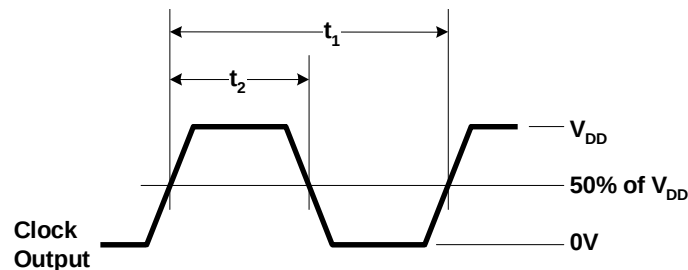
## AC Electrical Specifications

| Parameter <sup>[1]</sup> | Name              | Description                                                                                              | Min. | Typ. | Max. | Unit |
|--------------------------|-------------------|----------------------------------------------------------------------------------------------------------|------|------|------|------|
| DC                       | Output Duty Cycle | Duty Cycle is defined in <i>Figure 1</i> ; $t_1/t_2$ , 50% of $V_{DD}$                                   | 45   | 50   | 55   | %    |
| ER                       | Rising Edge Rate  | Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$ , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> . | 0.8  | 1.4  |      | V/ns |
| EF                       | Falling Edge Rate | Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$ , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> . | 0.8  | 1.4  |      | V/ns |
| $t_9$                    | Clock Jitter      | CLK1, CLK2 Peak-Peak period jitter                                                                       |      | 200  |      | ps   |
| $t_{10}$                 | PLL Lock Time     |                                                                                                          |      |      | 3    | ms   |

## Test and Measurement Set-up



## Voltage and Timing Definitions



**Figure 1. Duty Cycle Definitions**

### Note:

1. Not 100% tested.

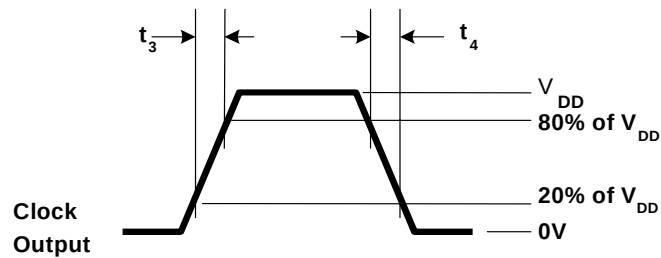


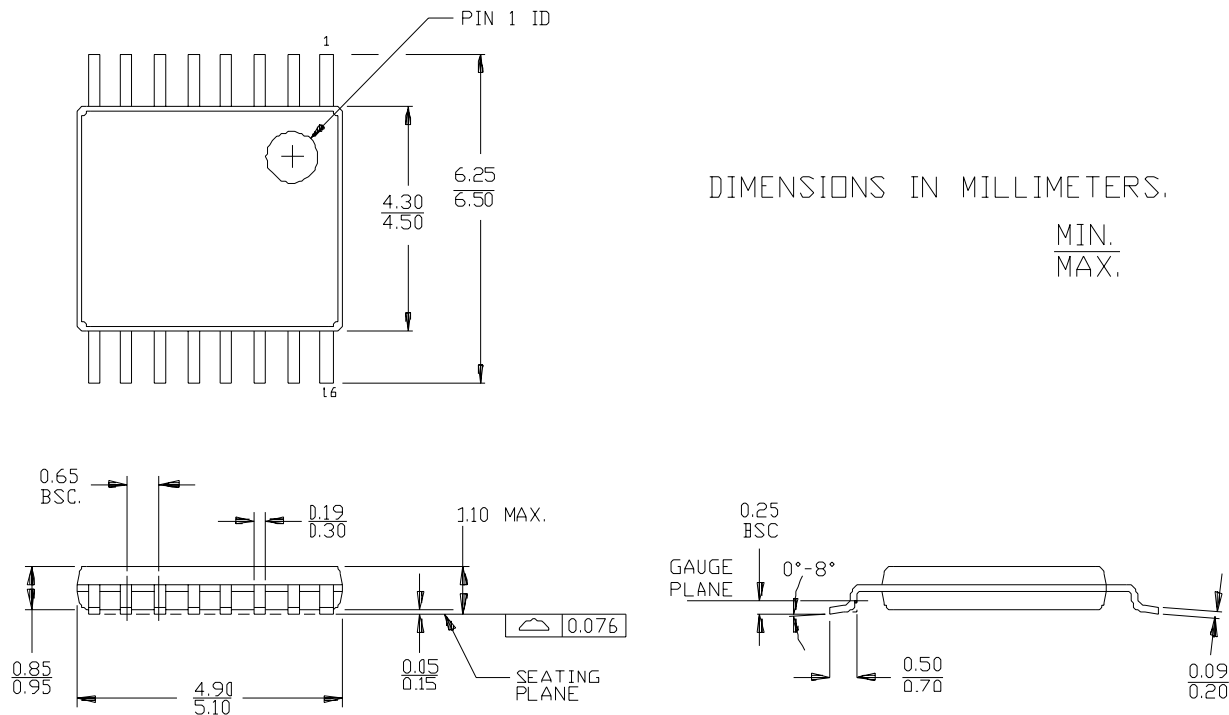
Figure 2.  $ER = (0.6 \times V_{DD}) / t_3$ ,  $EF = (0.6 \times V_{DD}) / t_4$

## Ordering Information

| Ordering Code | Package Name | Package Type                 | Operating Range | Operating Voltage |
|---------------|--------------|------------------------------|-----------------|-------------------|
| CY24206ZC-1   | Z16          | 16-Pin TSSOP                 | Commercial      | 3.3V              |
| CY24206ZC-1T  | Z16          | 16-Pin TSSOP – Tape and Reel | Commercial      | 3.3V              |
| CY24206ZC-2   | Z16          | 16-Pin TSSOP                 | Commercial      | 3.3V              |
| CY24206ZC-2T  | Z16          | 16-Pin TSSOP – Tape and Reel | Commercial      | 3.3V              |
| CY24206ZC-3   | Z16          | 16-Pin TSSOP                 | Commercial      | 3.3V              |
| CY24206ZC-3T  | Z16          | 16-Pin TSSOP – Tape and Reel | Commercial      | 3.3V              |
| CY24206ZC-4   | Z16          | 16-Pin TSSOP                 | Commercial      | 3.3V              |
| CY24206ZC-4T  | Z16          | 16-Pin TSSOP – Tape and Reel | Commercial      | 3.3V              |

## Package Drawing and Dimensions

### 16-Lead Thin Shrink Small Outline Package (4.40 MM Body) Z16



51-85091-1\*\*

MediaClock is a trademark of Cypress Semiconductor Corporation. All product and company names mentioned in this document may be the trademarks of their respective holders.

**Document History Page**

| <b>Document Title: CY24206 MediaClock™ DTV, STB Clock Generator</b><br><b>Document Number: 38-07451</b> |                |                   |                        |                              |
|---------------------------------------------------------------------------------------------------------|----------------|-------------------|------------------------|------------------------------|
| <b>REV.</b>                                                                                             | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b> |
| **                                                                                                      | 120901         | 12/10/02          | CKN                    | New Data Sheet               |
| *A                                                                                                      | 123046         | 03/03/03          | CKN                    | Added -4 to data sheet       |