

SPOC+ 12V

BTS56033-LBA

SPI Power Controller

Data Sheet

Rev. 1.0, 2013-03-24

Automotive

## Revision History

Page or Item	Subjects (major changes since previous revision)
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**Rev. 1.0, 2013-03-24**

All	Data Sheet released
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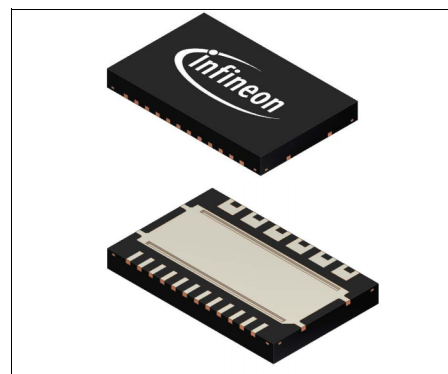




## 1 Overview

### Features

- 8 bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for four channels
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Very low stand-by current
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified



**TSON-24-3**

Package	Marking
TSON-24-3	BTS56033-LBA

### Description

The SPOC+ BTS56033-LBA is a six channel high-side smart power switch in TSON-24-3 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive exterior lamps up to 27 W and 10 W, or the equivalent LED light.

**Table 1-1 Product Summary**

Operating Voltage Power Switch	$V_S$	5.5 ... 28 V
Logic Supply Voltage	$V_{DD}$	3.8 ... 5.5 V
Over Voltage Protection	$V_{S(AZ,min)}$	42 V
Maximum Stand-By Current at 25 °C	$I_{S(OFF)}$	3 $\mu$ A
Maximum ON State Resistance at $T_j = 150$ °C Channel 2, 3, 4	$R_{DS(ON,max)}$	78 m $\Omega$
Maximum ON State Resistance at $T_j = 150$ °C Channel 1, 5, 6	$R_{DS(ON,max)}$	220 m $\Omega$
SPI Access Frequency	$f_{SCLK(max)}$	2.5 MHz

Configuration and status diagnosis are done via SPI. An 8 bit serial peripheral interface (SPI) is used. The SPI is daisy chain capable.

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over temperature flag per output is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to  $V_S$  diagnosis.

Channels 2, 3 and 4 can be configured to bulb or LED mode for maximum flexibility.

The SPOC+ BTS56033-LBA provides a fail-safe feature via a Limp Home Input (LHI) pin and direct INput pins.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

### Applications

- High-side power switch for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for standard exterior lighting like position light, tail light, brake light, parking light, license plate light, indicators and equivalent in the LED technology
- Replaces electromechanical relays, fuses and discrete circuits

### Protective Functions

- Reverse battery protection with external components
- Short circuit to ground protection
- Stable behavior at under voltage
- Current limitation
- Absolute and dynamic temperature sensor
- Thermal shutdown with latch after a limited amount of retries
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

### Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio ( $k_{ILIS}$ ) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode
- Feedback on over temperature via SPI
- Short circuit to  $V_S$  detection
- Monitoring of Input pins status

### Application Specific Functions

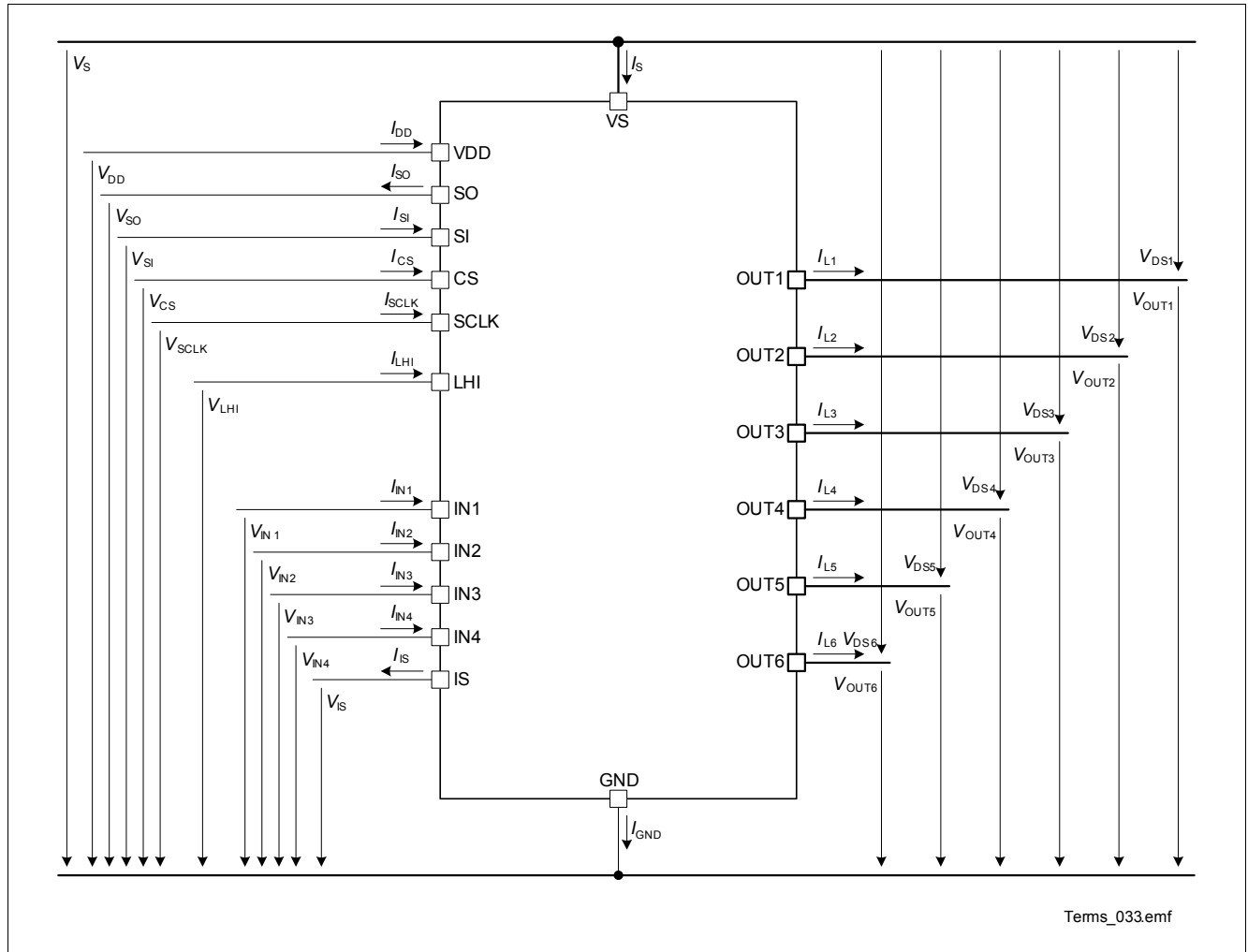
- Fail-safe activation via LHI pin and control via input pins
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs
- LED mode selection available
- SPI with daisy chain capability
- Switch bypass monitoring for detecting short circuit to  $V_S$





## 2.1 Terms

Figure 2-2 shows all terms used in this data sheet, with associated convention for positive values.



**Figure 2-2 Voltage and Current Definition**

In all tables of electrical characteristics, symbols related to channels without channel number are valid for each channel separately (e.g.  $V_{DS}$  specification is valid for  $V_{DS1} \dots V_{DS6}$ ).

All SPI register bits are marked as follows: ADDR.PARAMETER (e.g. HWCR.STB) with the exception of the bits in the Diagnosis frames which are marked only with PARAMETER (e.g. VSMON).

### 3 Pin Configuration

#### 3.1 Pin Assignment SPOC+ BTS56033-LBA

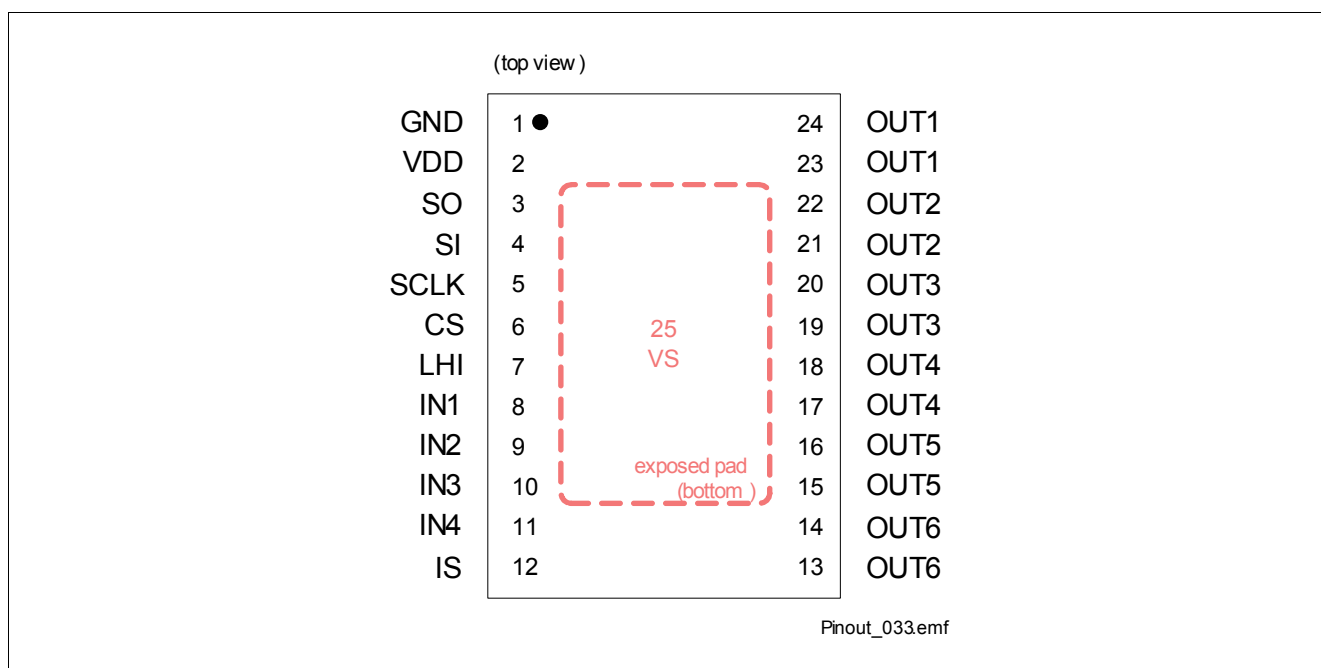


Figure 3-1 Pin Configuration TSON-24-3

## 3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
<b>Power Supply Pins</b>			
25	VS	–	Positive power supply for high-side power switch
1	GND	–	Ground connection
2	VDD	–	Logic supply (5 V)
<b>SPI &amp; Diagnosis Pins</b>			
3	SO	O	Serial output of SPI interface
4	SI	I	Serial input of SPI interface ("high" active)
5	SCLK	I	Serial clock of SPI interface ("high" active)
6	CS	I	Chip select of SPI interface ("low" active); Integrated pull up do VDD
12	IS	O	Current sense output signal
<b>Limp Home Input Pin (integrated pull-down, leave unused Limp Home Input pin unconnected)</b>			
7	LHI	I	Limp home activation signal ("high" active)
<b>Parallel Input Pins (integrated pull-down, leave unused pins unconnected)</b>			
8	IN1	I	Input signal of channel 1 ("high" active)
9	IN2	I	Input signal of channel 2 ("high" active)
10	IN3	I	Input signal of channel 3 ("high" active)
11	IN4	I	Input signal of channel 4 ("high" active)
<b>Power Output Pins</b>			
23, 24 <sup>1)</sup>	OUT1	O	Protected high-side power output of channel 1
21, 22 <sup>1)</sup>	OUT2	O	Protected high-side power output of channel 2
19, 20 <sup>1)</sup>	OUT3	O	Protected high-side power output of channel 3
17, 18 <sup>1)</sup>	OUT4	O	Protected high-side power output of channel 4
15, 16 <sup>1)</sup>	OUT5	O	Protected high-side power output of channel 5
13, 14 <sup>1)</sup>	OUT6	O	Protected high-side power output of channel 6

1) All outputs pins of each channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

$T_j = -40$  to  $+150$  °C; all voltages with respect to ground

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 2, 3, 4:  $R_L = 6.8 \Omega$  (33  $\Omega$  when **LGCR.LEDn** = 1)

Channel 1, 5, 6:  $R_L = 18 \Omega$

**Table 4-1 Absolute Maximum Ratings** <sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage							
Power supply voltage	$V_S$	-0.3		28	V	—	P_4.1.1
Logic supply voltage	$V_{DD}$	-0.3		5.5	V	—	P_4.1.2
Reverse polarity voltage	$-V_{S(\text{rev})}$	—		16	V	<sup>2)</sup> $T_{j\text{Start}} = 25\text{ }^{\circ}\text{C}$ $t \leq 2\text{ min.}$ See <b>Chapter 10</b> for setup	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(\text{SC})}$	0		24	V	<sup>3)</sup> $R_{\text{ECU}} = 20\text{ m}\Omega$ $l = 0\text{ or }5\text{ m}$ $R_{\text{Cable}} = 16\text{ m}\Omega/\text{m}$ $L_{\text{Cable}} = 1\text{ }\mu\text{H}/\text{m}$	P_4.1.4
Permanent short circuit Number channel activations All channels	$n_{\text{RSC1}}$	-		100	k	<sup>3)</sup> $V_{DD} = 5\text{ V}$ $t_{\text{ON}} = 300\text{ms}$	P_4.1.6
Voltage at power transistor	$V_{DS}$	—		42	V	—	P_4.1.8
Supply voltage for load dump protection	$V_{S(\text{LD})}$	—		42	V	<sup>4)</sup> $R_l = 2\text{ }\Omega$ $t = 400\text{ ms}$	P_4.1.9
Current through ground pin	$I_{\text{GND}}$	-100		25	mA	$t \leq 2\text{ min.}$	P_4.1.10
Current through VDD pin	$I_{DD}$	-25		12	mA	$t \leq 2\text{ min.}$	P_4.1.11
Power Stages							
Load current	$ I_L $	—		$I_{L(\text{LIM})}$	A	<sup>5)</sup>	P_4.1.12
Maximum energy dissipation single pulse - $I_{L(\text{nom})}$ Channel 2, 3, 4	$E_{AS}$	—		45	mJ	<sup>6)</sup> $T_{j(0)} = 150\text{ }^{\circ}\text{C}$ $I_{L(0)} = I_{L(\text{nom})} =$ P_6.6.17	P_4.1.15
Maximum energy dissipation single pulse - $I_{L(\text{nom})}$ Channel 1, 5, 6	$E_{AS}$	—		20	mJ	<sup>7)</sup> $T_{j(0)} = 150\text{ }^{\circ}\text{C}$ $I_{L(0)} = I_{L(\text{nom})} =$ P_6.6.18	P_4.1.16

## Electrical Characteristics

Table 4-1 Absolute Maximum Ratings (cont'd)<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Diagnosis Pin							
Voltage at sense pin IS	$V_{IS}$	-0.3		$V_S$	V	–	P_4.1.24
Current through sense pin IS	$I_{IS}$	-10		40	mA	$t \leq 2$ min.	P_4.1.25
Input Pins							
Voltage at input pins	$V_{IN}$	-0.3		6.0	V	–	P_4.1.26
Current through input pins	$I_{IN}$	-0.75		0.75	mA	–	P_4.1.27
Current through input pins	$I_{IN}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.28
SPI Pins							
Voltage at chip select pin	$V_{CS}$	-0.3		6.0	V	–	P_4.1.29
Current through chip select pin	$I_{CS}$	-0.75		0.75	mA	–	P_4.1.30
Current through chip select pin	$I_{CS}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.31
Voltage at serial input pin	$V_{SI}$	-0.3		6.0	V	–	P_4.1.32
Current through serial input pin	$I_{SI}$	-0.75		0.75	mA	–	P_4.1.33
Current through serial input pin	$I_{SI}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.34
Voltage at serial clock pin	$V_{SCLK}$	-0.3		6.0	V	–	P_4.1.35
Current through serial clock pin	$I_{SCLK}$	-0.75		0.75	mA	–	P_4.1.36
Current through serial clock pin	$I_{SCLK}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.37
Current through serial output pin SO	$I_{SO}$	-0.75		0.75	mA	–	P_4.1.38
Current through serial output pin SO	$I_{SO}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.39
Limp Home Input Pin							
Voltage at Limp Home Input pin	$V_{LHI}$	-0.3		6.0	V	–	P_4.1.40
Current through Limp Home Input pin	$I_{LHI}$	-0.75		0.75	mA	–	P_4.1.41
Current through Limp Home Input pin	$I_{LHI}$	-2.0		2.0	mA	$t \leq 2$ min.	P_4.1.42
Temperatures							
Junction temperature	$T_j$	-40		150	°C	–	P_4.1.45
Dynamic temperature increase while switching	$\Delta T_j$	–		60	K	–	P_4.1.46
Storage temperature	$T_{stg}$	-55		150	°C	–	P_4.1.47
ESD Susceptibility							
ESD susceptibility HBM OUT pins vs. VS	$V_{ESD}$	-4		4	kV	<sup>8)</sup> HBM	P_4.1.48
ESD susceptibility HBM all pins vs. VDD	$V_{ESD}$	-1.5		1.5	kV	<sup>8)</sup> HBM	P_4.1.54
ESD susceptibility HBM other pins vs. GND incl. OUT pins vs. GND	$V_{ESD}$	-2		2	kV	<sup>8)</sup> HBM	P_4.1.49

## Electrical Characteristics

**Table 4-1 Absolute Maximum Ratings (cont'd)<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ESD Resistivity to GND	$V_{\text{ESD}}$	-500		500	V	<sup>9)</sup> CDM	P_4.1.51
ESD Resistivity Pin 1, 12, 13, 24 (corner pins) to GND	$V_{\text{ESD}1, 12, 13, 24}$	-750		750	V	<sup>9)</sup> CDM	P_4.1.52

- 1) Not subject to production test, specified by design.
- 2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip and package) was simulated on a 76.4 \* 114.3 \* 1.5 mm board with 2 inner copper layers (2 \* 70 µm Cu, 2 \* 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.
- 3) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability at the end of this document.
- 4)  $R_i$  is the internal resistance of the load dump pulse generator.
- 5) Current limitation is a protection feature. Protection features are not designed for continuous repetitive operation.
- 6) Pulse shape represents inductive switch off:  $I_{D(t)} = I_D(0) \times (1 - t / t_{\text{pulse}})$ ;  $0 < t < t_{\text{pulse}}$
- 7) Pulse shape represents inductive switch off:  $I_{D(t)} = I_D(0) \times (1 - t / t_{\text{pulse}})$ ;  $0 < t < t_{\text{pulse}}$
- 8) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001-2010
- 9) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.



## 4.2 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4-2 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	$R_{thJSP}$	–	2	–	K/W	<sup>1)</sup> $T_{j(0)} = 105\text{ °C}$ measured to pin 25	P_4.2.1
Junction to Ambient	$R_{thJA}$	–	21	–	K/W	<sup>1)2)</sup> $T_{j(0)} = 105\text{ °C}$	P_4.2.2

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.4 \* 114.3 \* 1.5 mm board with 2 inner copper layers (2 \* 70 µm Cu, 2 \* 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

## 5 Power Supply

The SPOC+ BTS56033-LBA is supplied by two voltage sources:  $V_S$  and  $V_{DD}$ . The  $V_S$  supply line is used by the power switches. The  $V_{DD}$  supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins  $V_{DD}$  and GND is recommended as shown in [Chapter 10](#).

There is a power-on reset function implemented for the  $V_{DD}$  logic power supply which affect SPI registers status (see P\_5.3.17), and a undervoltage shutdown for  $V_S$  influencing the status of the outputs (see P\_5.3.2 and [Chapter 7.4](#) for further details). After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as  $V_{DD}$  is provided in the specified range independent of  $V_S$ . The first SPI transmission after a reset contains at pin SO the Standard Diagnosis information, with the transmission error bit **TER** set.

### 5.1 Power Supply Modes

The following table shows all possible power supply modes for  $V_S$ ,  $V_{DD}$  and the pin LHI.

Power Supply Modes	Off	Off	SPI on	Reset	Off	Limp Home Mode without SPI	Normal operation	Limp Home Mode with SPI <sup>1)</sup>
$V_S$	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V
$V_{DD}$	0 V	0 V	5 V	5 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	5 V	0 V	5 V
Power stage, protection	–	–	–	–	–	✓ <sup>2)</sup>	✓	✓ <sup>3)</sup>
Limp Home	–	–	–	–	–	✓	–	✓
SPI (logic)	–	–	✓	Reset	Reset	Reset	✓	Reset
Stand-by current	–	–	–	–	✓	–	✓ <sup>4)</sup>	–
Idle current	–	–	–	–	–	–	✓ <sup>5)</sup>	–
Diagnosis	–	–	–	–	–	–	✓	✓ <sup>6)</sup>

1) SPI read only.

2) Protection with unlimited reactivation and without latch off.

3) Protection with limited reactivation and latch off.

4) When **DCR.MUX** = 111<sub>B</sub>

5) When all channels are in OFF-state and **DCR.MUX** ≠ 111<sub>B</sub>.

6) Current sense disabled in Limp Home Mode.

#### 5.1.1 Stand-by Mode

Stand-by mode is entered as soon as the current sense multiplexer (**DCR.MUX**) is in default (stand-by) position<sup>1)</sup>. As soon as stand-by mode is entered, register **STB** is set. All channels are deactivated in stand-by mode. Refer to the [Chapter 5.2.3](#) for further information.

#### 5.1.2 Idle Mode

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and  $V_{DD}$  supply is available.

1) Not affected by the inputs state

### 5.1.3 Device Wake-up

To wake-up the device, the current sense multiplexer (**DCR.MUX**) is programmed to a value different from default position (stand-by).

Limp Home Input (LHI = "high") will wake-up the device and is working without  $V_{DD}$  supply. As a result, channels can be activated via the dedicated input pins.

## 5.2 Reset

There are several reset triggers implemented in the device. They reset the SPI registers and errors flags to their default values.

The first SPI transmission after any kind of reset contains at pin SO the Standard Diagnosis information, the transmission error bit **TER** is set.

### 5.2.1 Power-On Reset

The power-on reset is released, when  $V_{DD}$  voltage level is higher than  $V_{DD(min)}$ . The SPI interface can be accessed after wake up time  $t_{WU(PO)}$ .

### 5.2.2 Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as **HWCR.RST** bit is set to 1, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time  $t_{CS(td)}$  plus reset command delay time  $t_{d(RST)}$ .

### 5.2.3 Limp Home Mode

The Limp Home Mode will be activated as soon as the pin LHI is set to "high" for a time longer than  $t_{LHI(ac)}$ .

In Limp Home Mode, the SPI write-registers are reset. To prevent unexpected SPI reset by a non consistent signal at LHI pin,  $V_S$  monitoring is implemented.

The monitoring allows in Limp Home Mode, to reset the SPI write-registers, if LHI is set to "high" for longer than  $t_{LHI(ac)}$  and  $V_S > V_{SMON}$  (P\_5.3.12). Otherwise any glitch on LHI is filtered and has no effect on the SPI.

After an SPI reset, Output OUTn will follow the input INn configuration only for the channels where an direct INput pin is present. All other channels will be switched OFF. For application example refer to **Chapter 10**. The SPI interface is operating normally, so the Limp Home register bit LHI as well as the error flags can be read, but any write command will be ignored.

For the protection functions in Limp Home Mode, refer to **Chapter 7.1.1**.

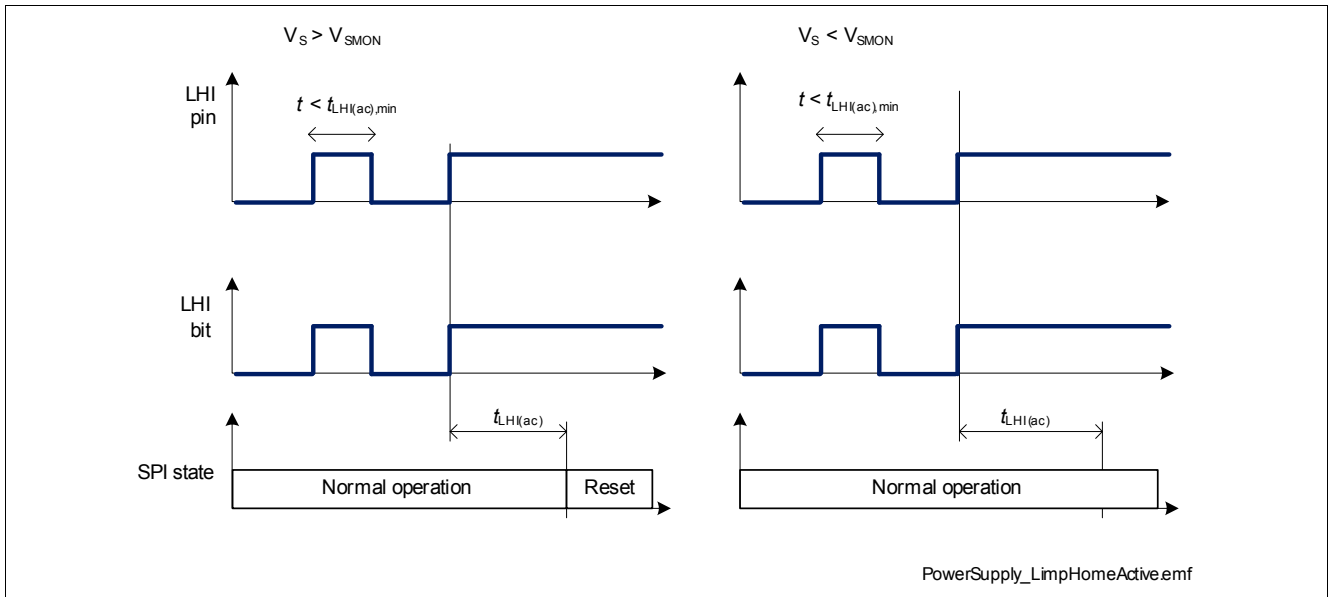


Figure 5-1 Limp Home Activation as function of  $V_S$

### 5.3 Electrical Characteristics

Unless otherwise specified:  $V_S = 7\text{ V to }18\text{ V}$ ,  $V_{DD} = 3.8\text{ V to }5.5\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $V_{DD} = 4.3\text{ V}$ ,  $T_j = 25\text{ °C}$

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 2, 3, 4:  $R_L = 6.8\text{ }\Omega$  (33  $\Omega$  when **LGCR.LEDn** = 1)

Channel 1, 5, 6:  $R_L = 18\text{ }\Omega$

**Table 5-1 Electrical Characteristics Power Supply**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Operating voltage power switch	$V_{S(OP)}$	5.5	—	28 <sup>1)</sup>	V	$V_{DS} < 0.5\text{ V}$	P_5.3.1
Undervoltage shutdown	$V_{S(UV)}$	—	—	4.5	V	OUTn = ON From $V_{DS} < 1\text{ V}$ to $I_{Ln} = 0\text{ A}$ (see <b>Figure 7-5</b> )	P_5.3.2
Undervoltage shutdown Hysteresis	$V_{S(HYS)}$	—	350	—	mV	<sup>1)</sup>	P_5.3.3
Stand-by current for whole device with loads	$I_{VS(STB)}$	—	0.1	3	μA	<sup>1)</sup> $V_{DD} = 0\text{ V}$ $V_{LHI} = 0\text{ V}$ $T_j = 25\text{ °C}$	P_5.3.7
Stand-by current for whole device with loads	$I_{VS(STB)}$	—	0.1	3	μA	<sup>1)</sup> $V_{DD} = 0\text{ V}$ $V_{LHI} = 0\text{ V}$ $T_j \leq 85\text{ °C}$	P_5.3.8
Stand-by current for whole device with loads	$I_{VS(STB)}$	—	4	58	μA	$V_{DD} = 0\text{ V}$ $V_{LHI} = 0\text{ V}$ $T_j = 150\text{ °C}$	P_5.3.26
Idle current for whole device with loads, all channels off.	$I_{VS(idle)}$	—	2.5	8	mA	$V_{DD} = 5\text{ V}$ <b>DCR.MUX</b> = 110 <sub>B</sub>	P_5.3.10
Operating current for whole device	$I_{GND}$	—	10	25	mA	$f_{SCLK} = 0\text{ MHz}$	P_5.3.28
$V_S$ threshold for Limp Home validation	$V_{SMON}$	0.6	1.2	1.8	V	<b>VSMON</b> = 1	P_5.3.12
VDD pin							
Logic supply voltage	$V_{DD}$	3.8	—	5.5 <sup>1)</sup>	V	$f_{SCLK} = 2\text{ MHz}$	P_5.3.13
Logic supply current Normal operation	$I_{DD}$	—	125	270	μA	$f_{SCLK} = 0\text{ MHz}$ $V_{CS} = V_{DD} = 5\text{ V}$ <b>DCR.MUX</b> ≠ 111 <sub>B</sub>	P_5.3.14
Logic Stand-by current	$I_{DD(STB)}$	—	40	90	μA	$f_{SCLK} = 0\text{ MHz}$ $V_{CS} = V_{DD} = 5\text{ V}$ <b>DCR.MUX</b> = 111 <sub>B</sub>	P_5.3.16

**Table 5-1 Electrical Characteristics Power Supply (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-On reset threshold voltage	$V_{DD(PO)}$	2.0	2.8	3.8	V	SI = 0 V SCLK = 0 V CS = 0 V SO from 0 to Z	P_5.3.17
<b>LHI Input Characteristics</b>							
L-input level at pin LHI	$V_{LHI(L)}$	-0.3	–	1.0	V	LHI = 1 (see Chapter 9.6.1)	P_5.3.18
H-input level at pin LHI	$V_{LHI(H)}$	2.6	–	6.0	V	–	P_5.3.19
L-input current through pin LHI	$I_{LHI(L)}$	3	27	75	μA	$V_{LHI} = 1.0 \text{ V}$	P_5.3.20
H-input current through pin LHI	$I_{LHI(H)}$	7	30	75	μA	$V_{LHI} = 2.6 \text{ V}$	P_5.3.21
<b>Timings</b>							
Power-On wake up time	$t_{WU(PO)}$	–	200	–	μs	<sup>1)</sup>	P_5.3.22
Limp Home acknowledgement time	$t_{LHI(ac)}$	5	–	200	μs	$V_{DD} = 5 \text{ V}$ polling of Standard Diagnosis (see Chapter 9.6.1) until LHI = STB = 1	P_5.3.23
Reset command delay time	$t_{d(RST)}$	–	–	100	μs	<sup>1)</sup>	P_5.3.25

1) Not subject to production test, specified by design.

*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature.*

*Typical values show the typical parameters expected from manufacturing at  $V_S = 13.5 \text{ V}$ ,  $V_{DD} = 4.3 \text{ V}$  and  $T_j = 25 \text{ °C}$*

## 6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs with charge pumps. There are six channels implemented in the device. Each channel can be switched on via SPI register `OUT` or via an input pin, when available. Channels 2, 3 and 4 provide a load type configuration for bulbs or LEDs in register `LGCR` (see [Chapter 9.7.3](#)). The load type configuration can be changed in ON- as well as in OFF-state.

### 6.1 Output ON-State Resistance

The ON-state resistance  $R_{DS(ON)}$  depends on the supply voltage  $V_S$  as well as on the junction temperature  $T_j$ . [Figure 6-1](#), [Figure 6-2](#) (channels 2, 3 and 4), [Figure 6-3](#), [Figure 6-4](#) (channels 1, 5 and 6) show those dependencies. The behavior in reverse polarity mode is described in [Chapter 7](#).

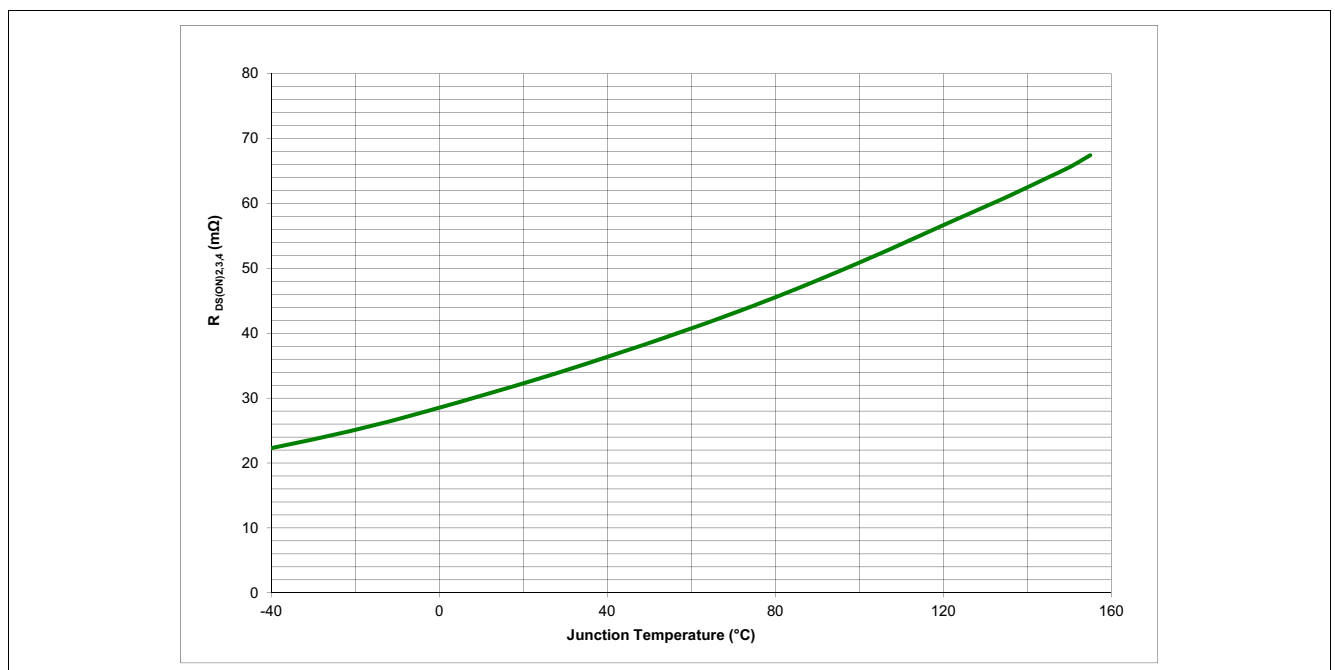


Figure 6-1 Typical On-State Resistance as function of  $T_j$  (ch. 2, 3, 4)



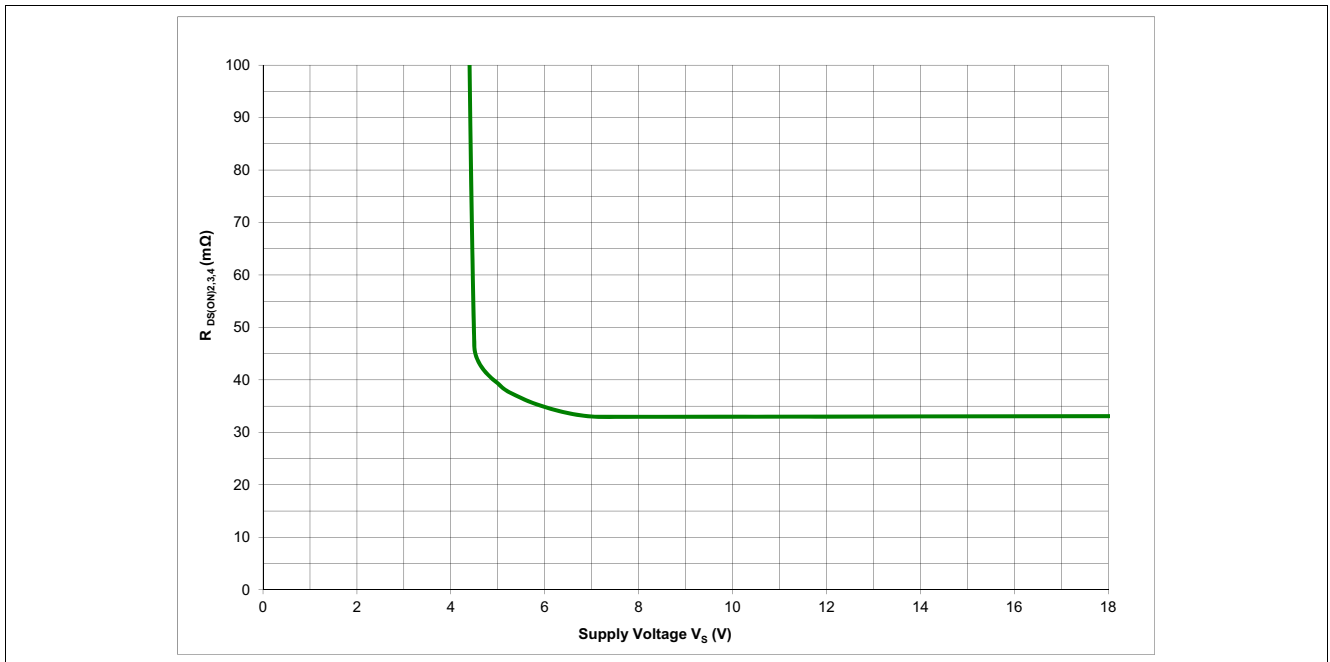


Figure 6-2 Typical On-State Resistance as function of  $V_S$  (ch. 2, 3, 4)

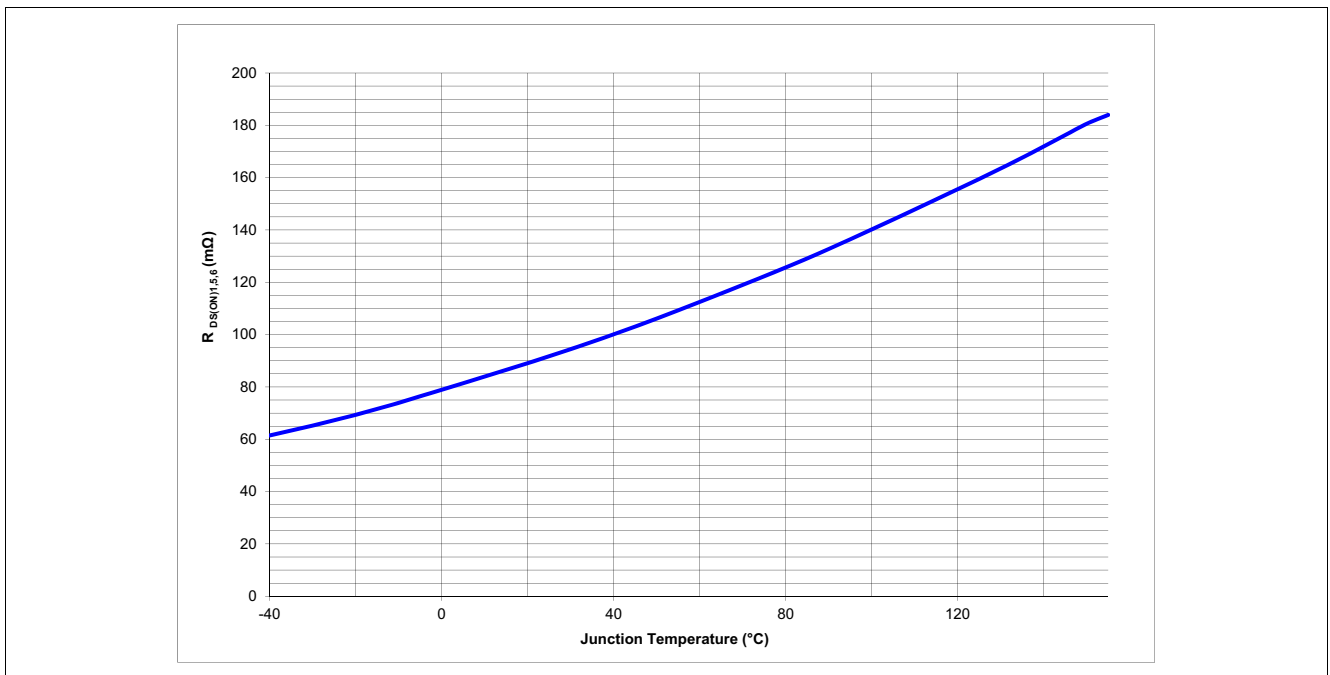


Figure 6-3 Typical On-State Resistance as function of  $T_J$  (ch. 1, 5, 6)

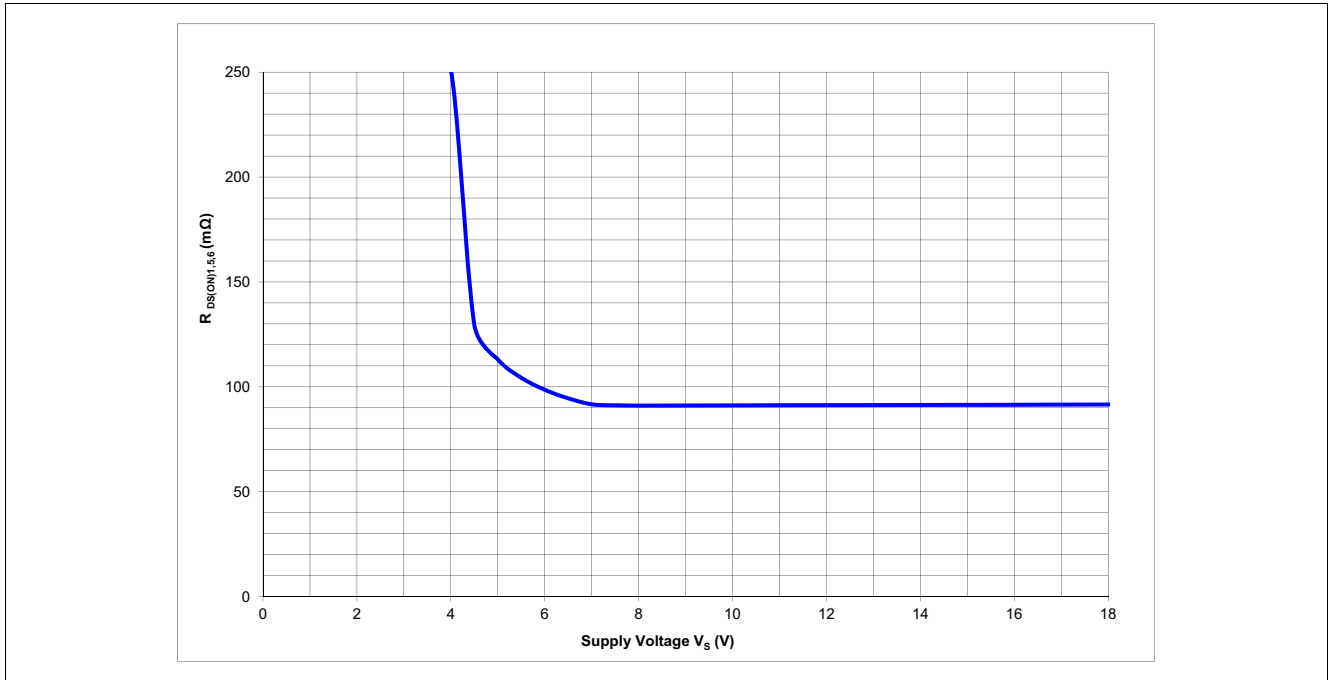


Figure 6-4 Typical On-State Resistance as function of  $V_S$  (ch. 1, 5, 6)

## 6.2 Input Circuit

There are two ways of using the input pins in combination with the OUT register by programming bit **HWCR.COL** in register **HWCR** (see [Chapter 9.7.5](#)).

- **HWCR.COL** = 0: A channel is switched ON either by the according **OUT** register bit or by the input pin.
- **HWCR.COL** = 1: A channel is switched ON by the according **OUT** register bit only, when the input pin is "high". In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register **OUT** (see [Chapter 9.7.1](#)).

The default state (**HWCR.COL** = 0) is the OR-combination of the input signal and the SPI-bit. In Limp Home Mode (LHI pin set to "high") the combinatorial logic is switched to OR-mode to enable a channel activation via the input pins only.

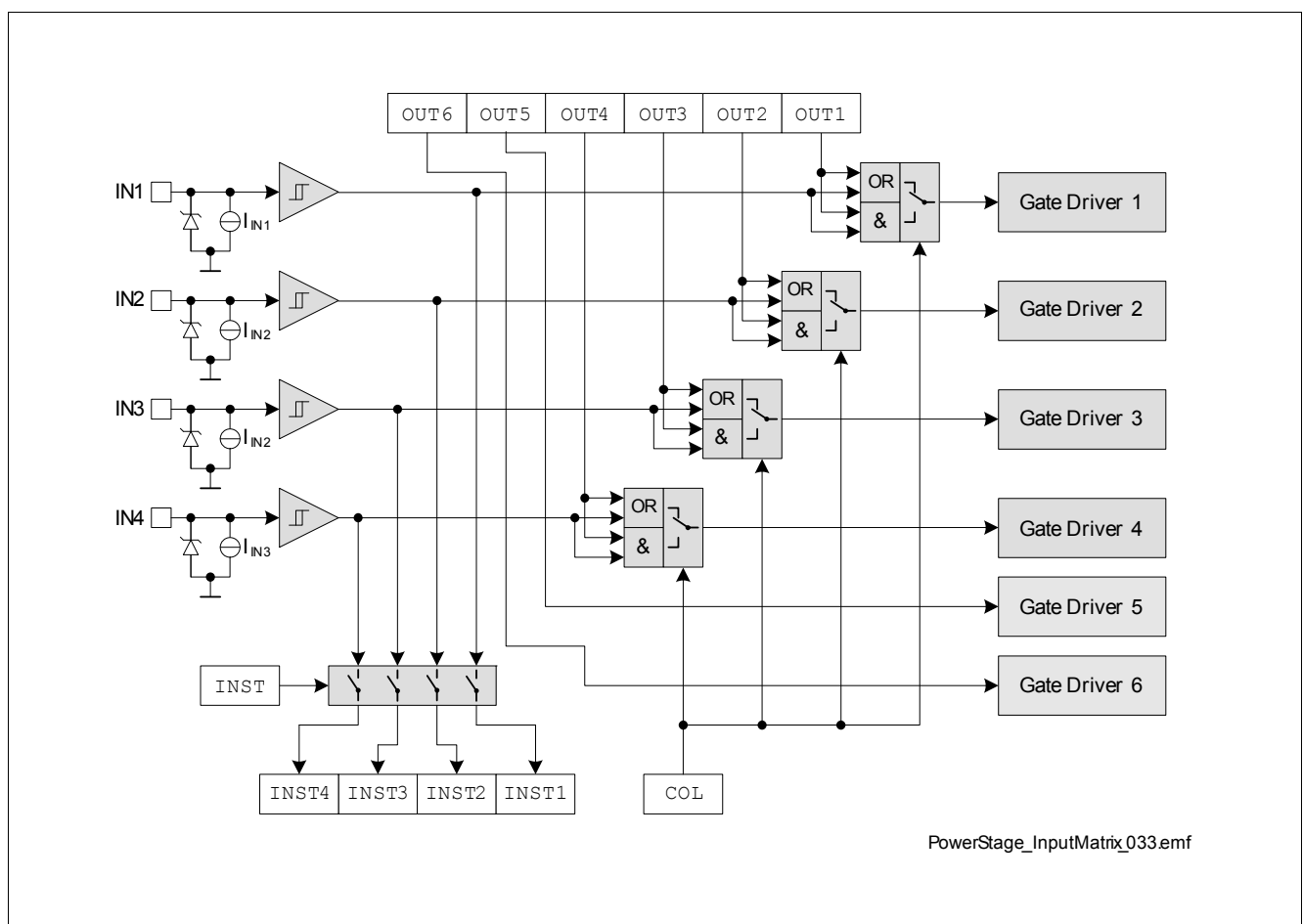
[Figure 6-5](#) shows the complete input switch matrix.

The zener diode protects the input circuit against ESD pulses. The current sink to ground ensures that the input signal is low in case of an open input pin.

## 6.3 Input Status Monitor

The level of the input stage can be monitored via the input status monitor. The input status is indicated in the **OUT** register for the available input pin. After setting the bit **SWCR.SWR**, the readout the output register **OUT** shows the state of the input pins.

*The input status monitor is operational only when SPOC+ BTS56033-LBA is not in stand-by operation. During stand-by operation this function is not supported.*



**Figure 6-5** Input Switch Matrix

## 6.4 Power Stage Output

The power stages are built to be used in high side configuration (Figure 6-6).

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission. Defined slew rates allow lowest EMC emissions during PWM operation at low switching losses.

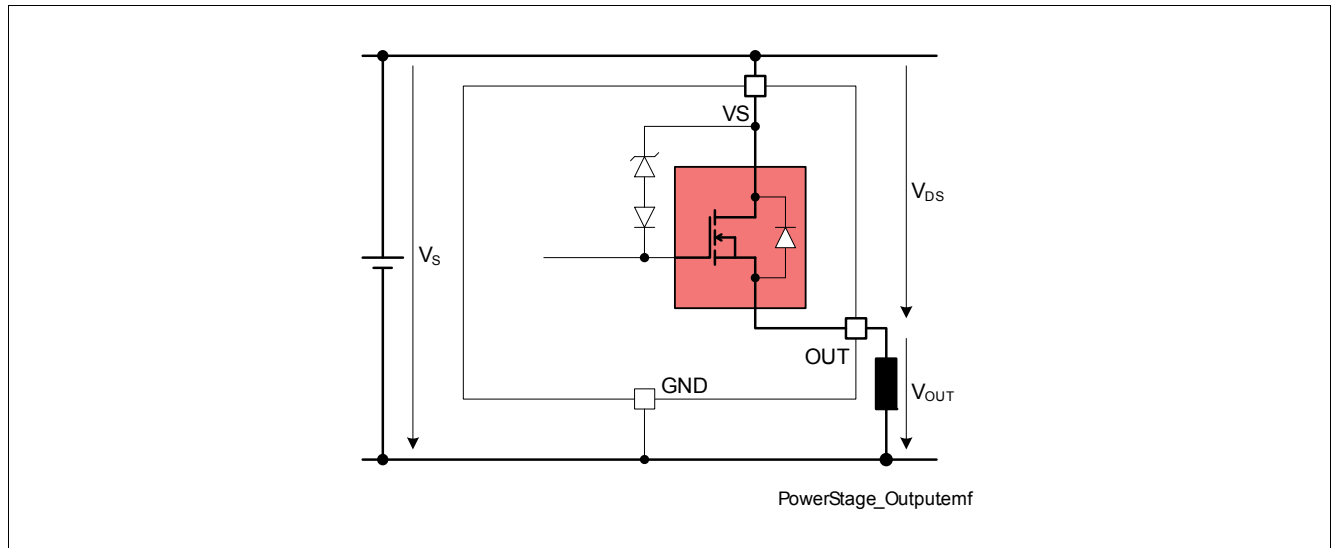


Figure 6-6 Power Stage Output

### 6.4.1 Bulb and LED Mode

Channels 2, 3 and 4 can be configured in bulb and LED mode via the SPI initialization registers `LGCR` when `SWCR.SWR = 0`. The default state is `LGCR.LEDn = 0`. During LED mode the following parameters are changed for an optimized functionality with LED loads: ON-state resistance  $R_{DS(ON)}$ , switching timings ( $t_{delay(ON)}$ ,  $t_{delay(OFF)}$ ,  $t_{ON}$ ,  $t_{OFF}$ ), slew rates  $dV/dt_{ON}$  and  $dV/dt_{OFF}$ , load current protections  $I_{L(LIM)}$  and current sense ratio  $k_{ILIS}$ .

### 6.4.2 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

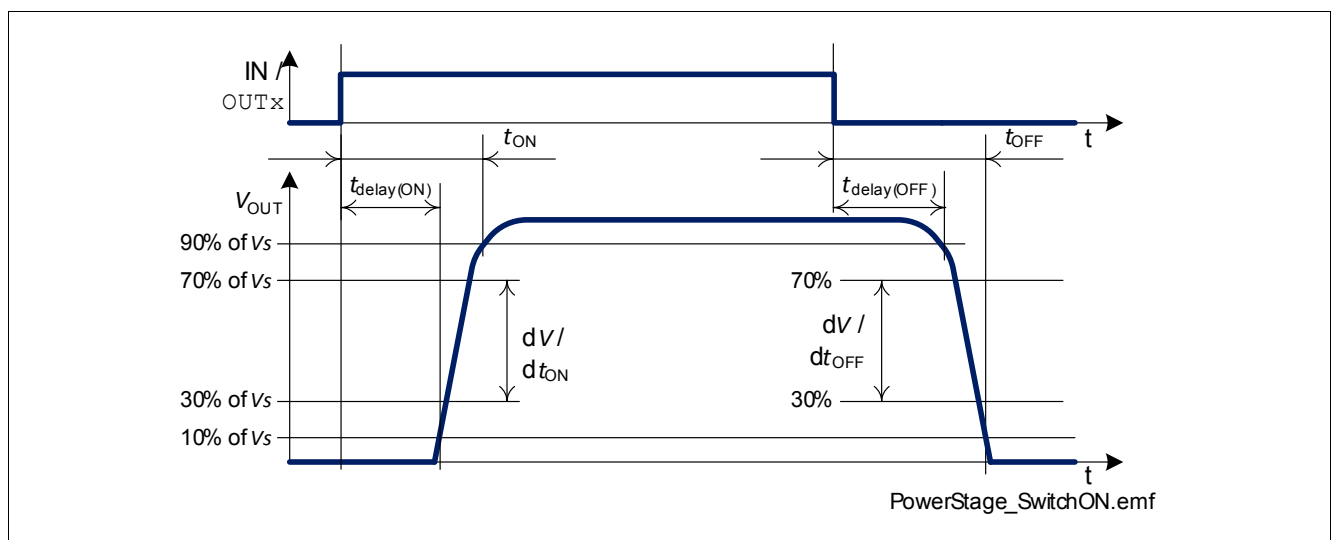


Figure 6-7 Switching a Load (resistive)

### 6.4.3 Switching Inductive Loads

When switching off inductive loads with high-side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, there is a voltage clamp mechanism implemented which limits that negative output voltage to a certain level ( $V_{DS(CL)}$  ([Chapter 6.5](#))). See [Figure 6-6](#) for details. Please refer also to [Chapter 7.3](#). The maximum allowed load inductance is limited.

### 6.4.4 Switching Channels in Parallel

In case of appearance of a short circuit with channels in parallel driving a single load, SPOC+ BTS56033-LBA output stages are not synchronized in the restart event. When all channels connected to the same load are in temperature limitation, the channel which has cooled down the fastest doesn't wait for the other ones to be cooled down as well to restart. Thus, it is not recommended to use the device with channels in parallel.

## 6.5 Electrical Characteristics

Unless otherwise specified:  $V_S = 7\text{ V to }18\text{ V}$ ,  $V_{DD} = 3.8\text{ V to }5.5\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $V_{DD} = 4.3\text{ V}$ ,  $T_j = 25\text{ °C}$

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 2, 3, 4:  $R_L = 6.8\text{ }\Omega$  (33  $\Omega$  when **LGCR.LEDn** = 1)

Channel 1, 5, 6:  $R_L = 18\text{ }\Omega$

**Table 6-1 Electrical Characteristics Power Stages**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Characteristics							
On-State resistance Channel 2, 3, 4	$R_{DS(ON)}$	–	39	–	mΩ	<sup>1)</sup> $V_S = 9\text{ V to }18\text{ V}$ $I_L = 2.6\text{ A}$ $T_j = 25\text{ °C}$ LGCR.LEDn = 0	P_6.6.9
On-State resistance Channel 2, 3, 4	$R_{DS(ON)}$	–	–	78	mΩ	$V_S = 9\text{ V to }18\text{ V}$ $I_L = 2.6\text{ A}$ $T_j = 150\text{ °C}$ LGCR . LEDn = 0	P_6.6.10
On-State resistance Channel 2, 3, 4	$R_{DS(ON)}$	–	137	–	mΩ	<sup>1)</sup> $V_S = 9\text{ V to }18\text{ V}$ $I_L = 0.6\text{ A}$ $T_j = 25\text{ °C}$ LGCR.LEDn = 1	P_6.6.11
On-State resistance Channel 2, 3, 4	$R_{DS(ON)}$	–	–	275	mΩ	$V_S = 9\text{ V to }18\text{ V}$ $I_L = 0.6\text{ A}$ $T_j = 150\text{ °C}$ LGCR . LEDn = 1	P_6.6.12
On-State resistance Channel 1, 5, 6	$R_{DS(ON)}$	–	110	–	mΩ	<sup>2)</sup> $V_S = 9\text{ V to }18\text{ V}$ $I_L = 2\text{ A}$ $T_j = 25\text{ °C}$	P_6.6.13
On-State resistance Channel 1, 5, 6	$R_{DS(ON)}$	–	–	220	mΩ	$V_S = 9\text{ V to }18\text{ V}$ $I_L = 2\text{ A}$ $T_j = 150\text{ °C}$	P_6.6.14
Nominal load current Channel 2, 3, 4  (all channels active)	$I_{L(nom)}$	–	2	–	A	<sup>1)</sup> $T_A = 85\text{ °C}$ $T_j < 150\text{ °C}$	P_6.6.17
Nominal load current Channel 1, 5, 6  (all channels active)	$I_{L(nom)}$	–	1.2	–	A	<sup>2)</sup> $T_A = 85\text{ °C}$ $T_j < 150\text{ °C}$	P_6.6.18
Output clamp	$V_{DS(CL)}$	42	47	54	V	$I_L = 20\text{ mA}$	P_6.6.19

Table 6-1 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current per channel $T_j \leq 85^\circ\text{C}$ Channel 2, 3, 4	$I_{L(\text{OFF})}$	–	0.02	0.5	$\mu\text{A}$	<sup>3)</sup> $V_{\text{IN}} = 0\text{ V}$ or floating <b>OUT.OUT</b> <sub>n</sub> = 0 $T_j \leq 85^\circ\text{C}$ Stand-by or idle mode	P_6.6.22
Output leakage current per channel $T_j \leq 85^\circ\text{C}$ Channel 1, 5, 6	$I_{L(\text{OFF})}$	–	0.02	0.5	$\mu\text{A}$	<sup>4)</sup> $V_{\text{IN}} = 0\text{ V}$ or floating <b>OUT.OUT</b> <sub>n</sub> = 0 $T_j \leq 85^\circ\text{C}$ Stand-by or idle mode	P_6.6.23
Output leakage current per channel $T_j = 150^\circ\text{C}$ Channel 2, 3, 4	$I_{L(\text{OFF})}$	–	1.5	10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$ or floating <b>OUT . OUT</b> <sub>n</sub> = 0 $T_j = 150^\circ\text{C}$ Stand-by or idle mode	P_6.6.26
Output leakage current per channel $T_j = 150^\circ\text{C}$ Channel 1, 5, 6	$I_{L(\text{OFF})}$	–	0.8	10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$ or floating <b>OUT . OUT</b> <sub>n</sub> = 0 $T_j = 150^\circ\text{C}$ Stand-by or idle mode	P_6.6.27

#### Input Characteristics

L-input level	$V_{\text{IN(L)}}$	-0.3	–	1.0	V	–	P_6.6.28
H-input level	$V_{\text{IN(H)}}$	2.6	–	6.0	V	–	P_6.6.29
L-input current	$I_{\text{IN(L)}}$	3	27	75	$\mu\text{A}$	$V_{\text{IN}} = 1.0\text{ V}$	P_6.6.30
H-input current	$I_{\text{IN(H)}}$	7	30	75	$\mu\text{A}$	$V_{\text{IN}} = 2.6\text{ V}$	P_6.6.31

#### Timings

Turn-ON delay to 10% $V_S$ (Logical propagation delay from input IN <sub>n</sub> to output OUT <sub>n</sub> ) Channel 2, 3, 4	$t_{\text{delay(ON)}}$	10	30	70	$\mu\text{s}$	$V_S = 13.5\text{ V}$ <b>LGCR . LED</b> <sub>n</sub> = 0	P_6.6.36
Turn-ON delay to 10% $V_S$ (Logical propagation delay from input IN <sub>n</sub> to output OUT <sub>n</sub> ) Channel 2, 3, 4	$t_{\text{delay(ON)}}$	3	10	25	$\mu\text{s}$	$V_S = 13.5\text{ V}$ <b>LGCR . LED</b> <sub>n</sub> = 1	P_6.6.37
Turn-ON delay to 10% $V_S$ (Logical propagation delay from input IN <sub>n</sub> to output OUT <sub>n</sub> ) Channel 1, 5, 6	$t_{\text{delay(ON)}}$	10	30	70	$\mu\text{s}$	$V_S = 13.5\text{ V}$	P_6.6.38



**Table 6-1 Electrical Characteristics Power Stages** (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn-OFF delay to 90% $V_S$ (Logical propagation delay from input INn to output OUTn) Channel 2, 3, 4	$t_{\text{delay(OFF)}}$	10	30	70	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 0$	P_6.6.43
Turn-OFF delay to 90% $V_S$ (Logical propagation delay from input INn to output OUTn) Channel 2, 3, 4	$t_{\text{delay(OFF)}}$	3	10	25	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 1$	P_6.6.44
Turn-OFF delay to 90% $V_S$ (Logical propagation delay from input INn to output OUTn) Channel 1, 5, 6	$t_{\text{delay(OFF)}}$	10	30	70	$\mu\text{s}$	$V_S = 13.5 \text{ V}$	P_6.6.45
Turn-ON time to 90% $V_S$ Channel 2, 3, 4	$t_{\text{ON}}$	30	75	180	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 0$	P_6.6.50
Turn-ON time to 90% $V_S$ Channel 2, 3, 4	$t_{\text{ON}}$	10	25	55	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 1$	P_6.6.51
Turn-ON time to 90% $V_S$ Channel 1, 5, 6	$t_{\text{ON}}$	30	75	180	$\mu\text{s}$	$V_S = 13.5 \text{ V}$	P_6.6.52
Turn-OFF time to 10% $V_S$ Channel 2, 3, 4	$t_{\text{OFF}}$	30	75	180	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 0$	P_6.6.57
Turn-OFF time to 10% $V_S$ Channel 2, 3, 4	$t_{\text{OFF}}$	10	25	55	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 1$	P_6.6.58
Turn-OFF time to 10% $V_S$ Channel 1, 5, 6	$t_{\text{OFF}}$	30	75	180	$\mu\text{s}$	$V_S = 13.5 \text{ V}$	P_6.6.59
Turn-ON/OFF matching Channel 2, 3, 4	$t_{\text{ON}} - t_{\text{OFF}}$	-30	0	50	$\mu\text{s}$	$V_S = 13.5 \text{ V}$ $\text{LGCR.LEDn} = 0$	P_6.6.68

**Table 6-1 Electrical Characteristics Power Stages** (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn-ON/OFF matching Channel 2, 3, 4	$t_{ON} - t_{OFF}$	-20	0	20	$\mu s$	$V_S = 13.5 V$ $LGCR.LEDn = 1$	P_6.6.69
Turn-ON/OFF matching Channel 1, 5, 6	$t_{ON} - t_{OFF}$	-30	0	50	$\mu s$	$V_S = 13.5 V$	P_6.6.70
Turn-ON slew rate 30% to 70% $V_S$ Channel 2, 3, 4	$dV/dt_{ON}$	0.1	0.25	0.5	V/ $\mu s$	$V_S = 13.5 V$ $LGCR.LEDn = 0$	P_6.6.75
Turn-ON slew rate 30% to 70% $V_S$ Channel 2, 3, 4	$dV/dt_{ON}$	0.35	0.88	1.75	V/ $\mu s$	$V_S = 13.5 V$ $LGCR.LEDn = 1$	P_6.6.76
Turn-ON slew rate 30% to 70% $V_S$ Channel 1, 5, 6	$dV/dt_{ON}$	0.1	0.25	0.5	V/ $\mu s$	$V_S = 13.5 V$	P_6.6.77
Turn-OFF slew rate 70% to 30% $V_S$ Channel 2, 3, 4	$-dV/dt_{OFF}$	0.1	0.25	0.5	V/ $\mu s$	$V_S = 13.5 V$ $LGCR.LEDn = 0$	P_6.6.82
Turn-OFF slew rate 70% to 30% $V_S$ Channel 2, 3, 4	$-dV/dt_{OFF}$	0.35	0.88	1.75	V/ $\mu s$	$V_S = 13.5 V$ $LGCR.LEDn = 1$	P_6.6.83
Turn-OFF slew rate 70% to 30% $V_S$ Channel 1, 5, 6	$-dV/dt_{OFF}$	0.1	0.25	0.5	V/ $\mu s$	$V_S = 13.5 V$	P_6.6.84

**Output Voltage Drop**

Output voltage drop limitation at small load currents Channel 2, 3, 4	$V_{DS(NL)}$	-	10	25	mV	$I_L = 50 mA$ $LGCR.GBRn = 1$	P_6.6.94
Output voltage drop limitation at small load currents Channel 1, 5, 6	$V_{DS(NL)}$	-	15	30	mV	$I_L = 20 mA$	P_6.6.95

1) Not subject to production test, specified by design.

2) Not subject to production test, specified by design.

3) Tested at  $T_j = -40^\circ C$

4) Tested at  $T_j = -40\text{ °C}$

## 7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

### 7.1 Over Load Protection

The load current  $I_L$  is limited by the device itself in case of over load or short circuit to ground. There are multiple steps of current limitation which are selected automatically depending on the voltage  $V_{DS}$  across the power DMOS. Please note that  $V_{OUT} = V_S - V_{DS}$ . Please refer to following figures for details.

Current limitation to the value  $I_{L(LIM)}$  is realized by increasing the resistance of the output channel, which leads to fast DMOS temperature rise.

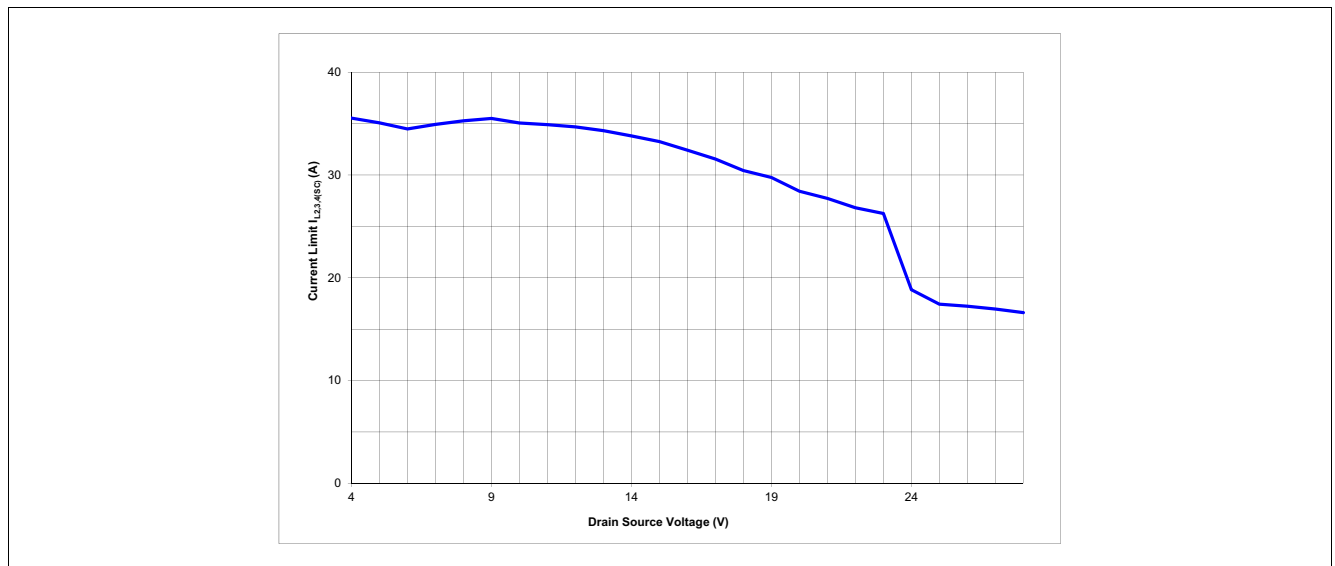


Figure 7-1 Current Limitation Channel 2, 3, 4 (typical values)

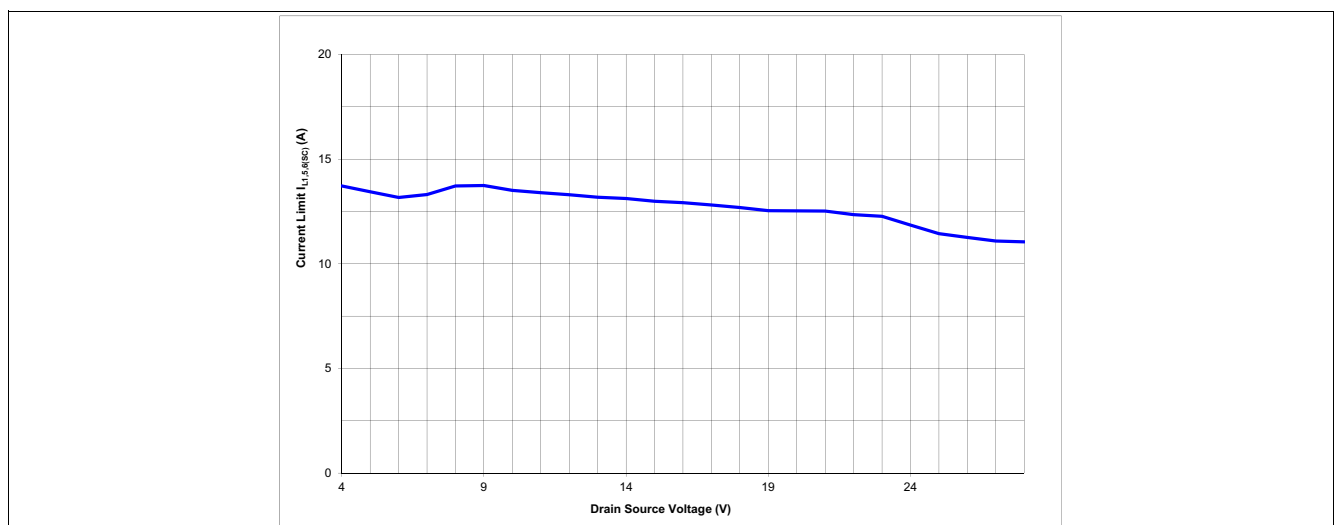


Figure 7-2 Current Limitation Channels 1, 5, 6 (typical values)

### 7.1.1 Over Temperature Protection

Each channel incorporates both an absolute  $T_{j(SC)}$  and a dynamic  $\Delta T_{j(SW)}$  temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value.

Each time a channel is switched OFF the error counter of that channel will be incremented by one. The number of automatic reactivations is limited by  $n_{\text{retry}}$ . If this number of retries is reached the channel turns OFF and latches OFF.

The error information related to the given channel will be available on the Standard Diagnosis and Errors Diagnosis. After switching OFF and latching OFF, the only way to switch ON again, is to clear all thermal counters and errors on all channels by setting **HWCR.CTC** bit to 1. If the channel is active (either **OUT.OUT<sub>n</sub>** = 1 or **IN<sub>n</sub>** = 1) it will be turned on immediately after the SPI command.

For the condition  $n < n_{\text{retry}}$  the counter of automatic reactivations will be reset by every channel activation if **HWCR.RCR** bit is set to 1.

In Limp Home Mode, the thermal counters of the protection functions are still operative only if  $V_{DD}$  is provided in the specified range. Otherwise the counters are not active and all channels are in „unlimited restart“ mode.

It is not possible to reset the counters using **HWCR.CTC** bit as long as the SPI is in Limp Home Mode, even if the  $V_{DD}$  is provided.

Refer to [Figure 7-3](#) and [Figure 7-4](#) for details.

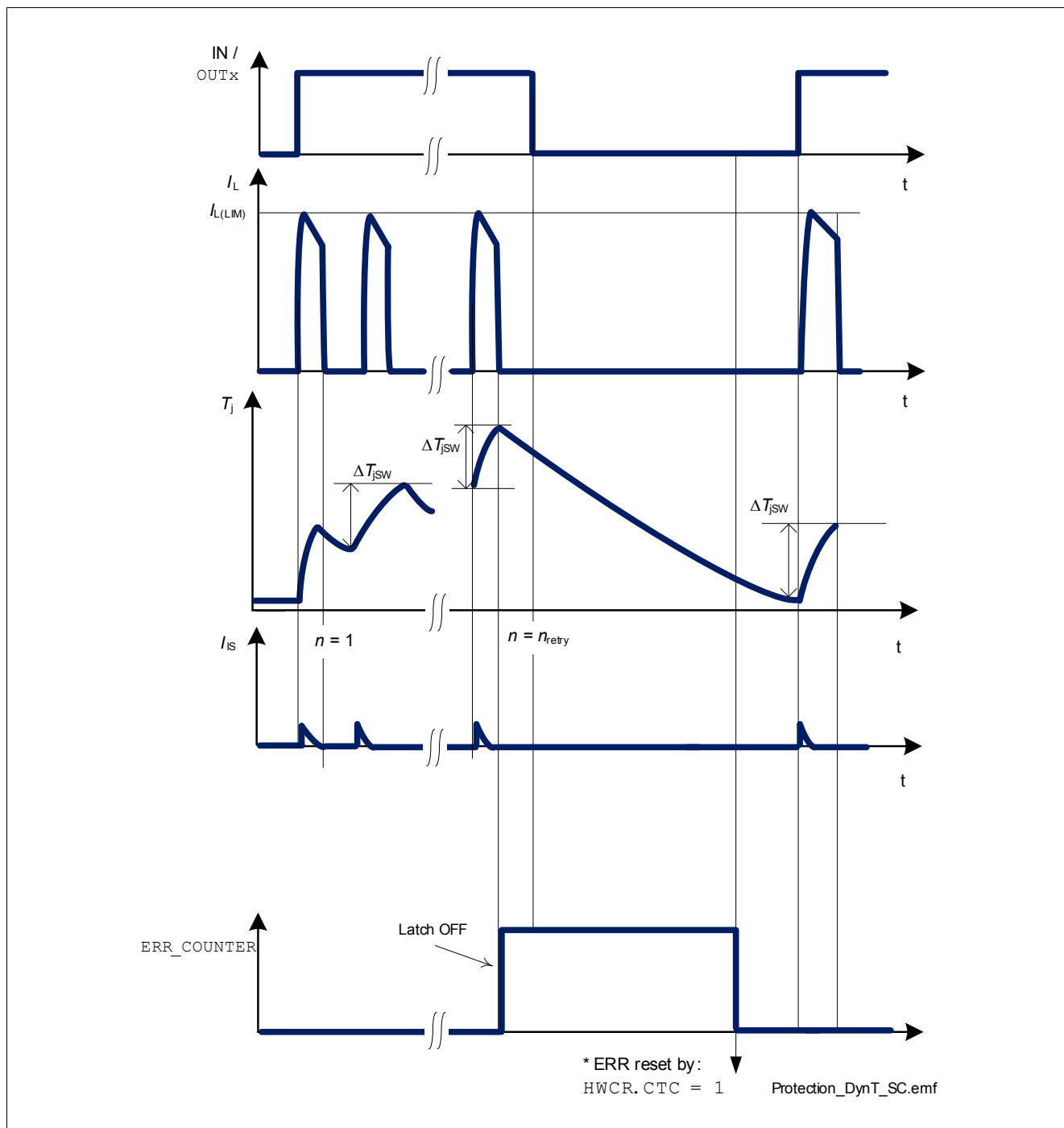


Figure 7-3 Dynamic Temperature Sensor Operations - Short Circuit

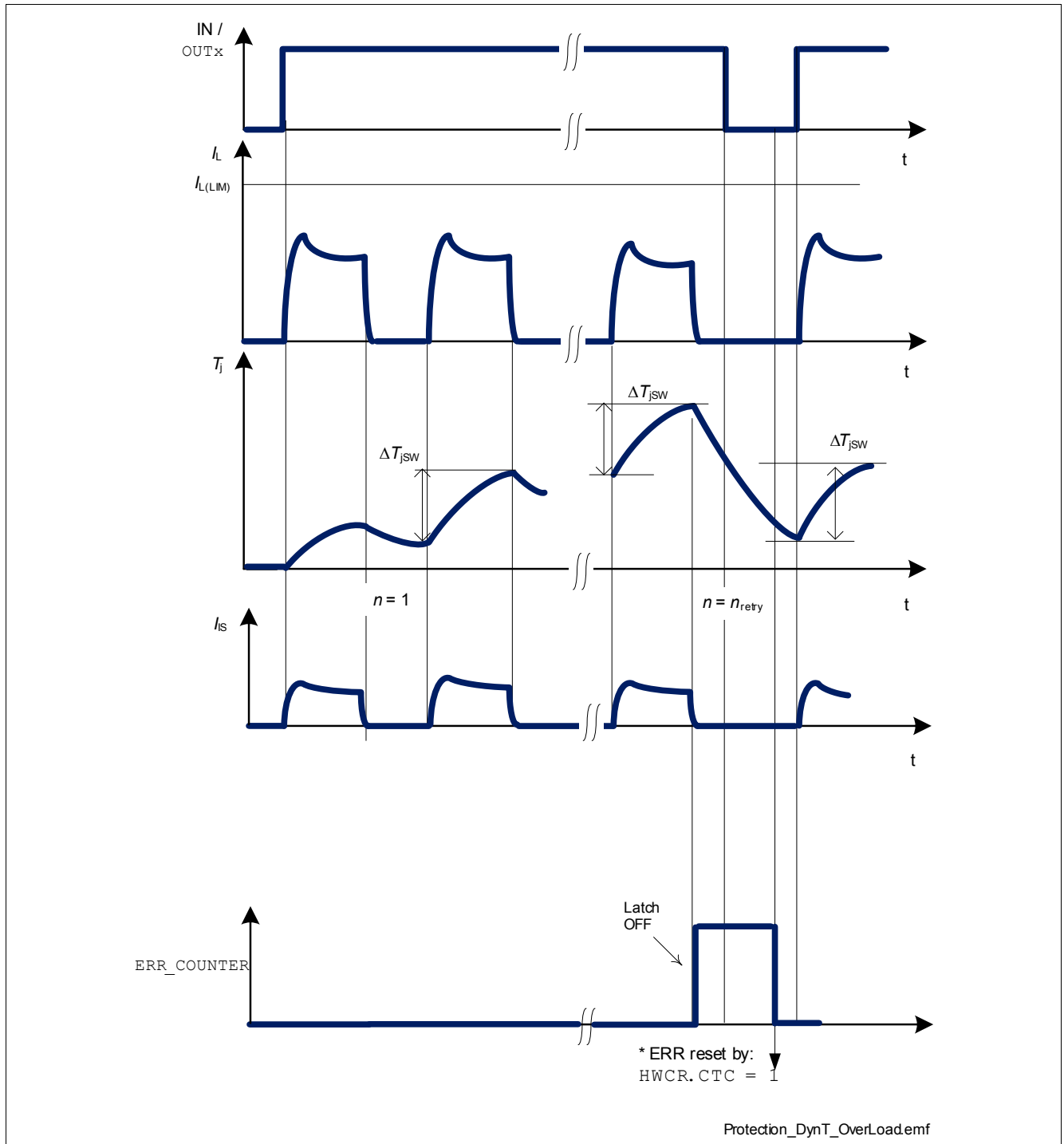


Figure 7-4 Dynamic Temperature Sensor Operations - Overload Condition

## 7.2 Reverse Polarity Protection

In reverse polarity condition, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads. The current through ground pin GND, sense pin IS, logic power supply pin  $V_{DD}$ , SPI pins, input pins and Limp Home Input pin has to be limited as well (please refer to the maximum ratings listed on [Chapter 4.1](#)).



*Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.*

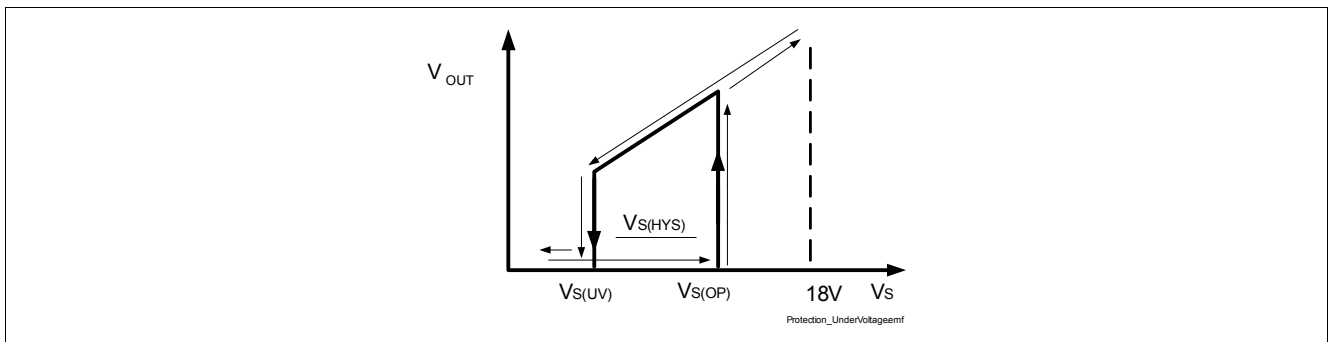
### 7.3 Over Voltage Protection

In the case of supply voltages between  $V_{S(SC)max}$  and  $V_{S(AZ)}$  the output transistors are still operational and follow the input or the `OUT` register. Parameters are not warranted and lifetime is reduced compared to nominal voltage supply.

In addition to the output clamp for inductive loads as described in [Chapter 6.4.3](#), there is a clamp mechanism available for over voltage protection for the logic and all channels.

### 7.4 Undervoltage Protection

Between  $V_{S(UV)}$  and  $V_{S(OP)}$ , the undervoltage mechanism is triggered.  $V_{S(OP)}$  represents the minimum voltage where the switching ON and OFF can take place.  $V_{S(UV)}$  represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism  $V_{S(UV)}$ , the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism  $V_{S(OP)}$ , then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until  $V_S$  is in the nominal range. [Figure 7-5](#) sketches the undervoltage mechanism.



**Figure 7-5 Undervoltage Behavior**

### 7.5 Loss of Ground

In case of complete loss of the device ground connection, but loads connected to ground, the SPOC+ BTS56033-LBA securely changes to or stays in OFF-state. Please refer to [Chapter 10](#) where an application setup is described.

### 7.6 Loss of $V_S$

In case of loss of  $V_S$  connection in ON-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from  $V_S$  to ground. For example, a suppressor diode is recommended between  $V_S$  and GND.

## 7.7 Electrical Characteristics

Unless otherwise specified:  $V_S = 7\text{ V to }18\text{ V}$ ,  $V_{DD} = 3.8\text{ V to }5.5\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_S = 13.5\text{ V}$ ,  $V_{DD} = 4.3\text{ V}$ ,  $T_j = 25\text{ °C}$

Typical resistive loads connected to the outputs (unless otherwise specified):

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 2, 3, 4:  $R_L = 6.8\text{ }\Omega$  (33  $\Omega$  when **LGCR.LED**<sub>n</sub> = 1)

Channel 1, 5, 6:  $R_L = 18\text{ }\Omega$

**Table 7-1 Electrical Characteristics Protection Functions**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over Load Protection							
Channel 2, 3, 4	$I_{L(LIM)}$	25	32	44	A	1) $V_{DS} = 5\text{ V}$ LGCR.LEDn = 0	P_7.7.9
Load current limitation Channel 2, 3, 4	$I_{L(LIM)}$	—	16	—	A	1) $V_{DS} = 26\text{ V}$ LGCR.LEDn = 0	P_7.7.10
Load current limitation Channel 2, 3, 4	$I_{L(LIM)}$	6.5	9	16	A	$V_{DS} = 5\text{ V}$ $T_j = -40\text{ °C}$ LGCR.LEDn = 1	P_7.7.11
Load current limitation Channel 2, 3, 4	$I_{L(LIM)}$	—	4.5	—	A	1) $V_{DS} = 26\text{ V}$ LGCR.LEDn = 1	P_7.7.12
Load current limitation Channel 1, 5, 6	$I_{L(LIM)}$	9	12	16	A	$V_{DS} = 5\text{ V}$ $T_j = -40\text{ °C}$	P_7.7.13
Over Temperature Protection							
Thermal shut down temperature	$T_{j(SC)}$	150	170	200	°C	1)	P_7.7.14
Thermal hysteresis of thermal shutdown	$\Delta T_{j(SC)}$	—	20	—	K	1)	P_7.7.15
Dynamic temperature increase limitation while switching	$\Delta T_{j(SW)}$	—	80	—	K	1)	P_7.7.16
Number of automatic retries at dynamic temperature sensor or over temperature shut down	$n_{\text{retry}}$	—	8	9		1)	P_7.7.17
Reverse Polarity							
Drain source diode voltage during reverse polarity Channel 2, 3, 4	$V_{DS(REV)}$	400	650	800	mV	$I_L = I_{L(nom)} =$ P_6.6.17 $T_j = 150\text{ °C}$	P_7.7.20

## Protection Functions

Table 7-1 Electrical Characteristics Protection Functions (cont'd)

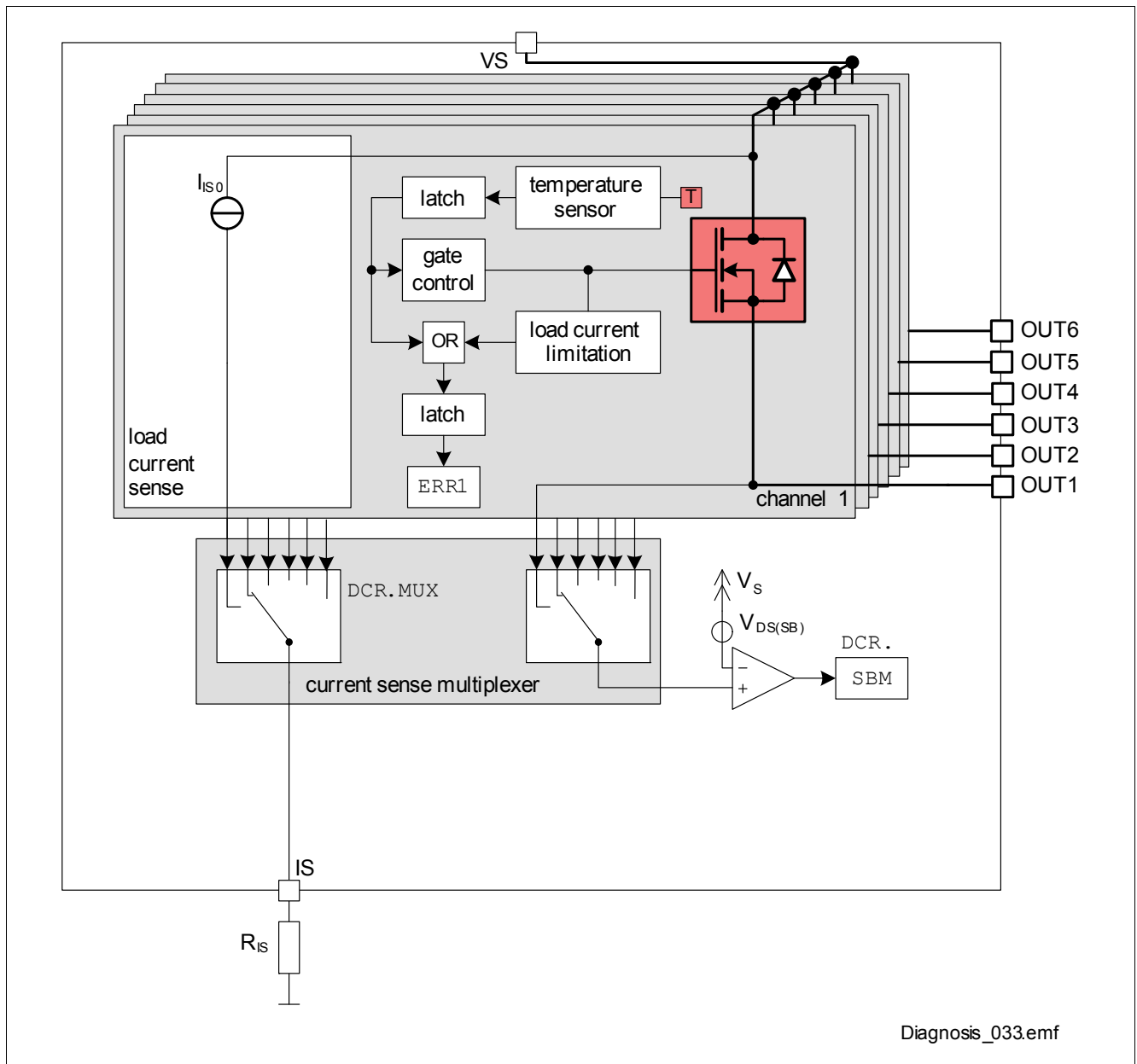
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Drain source diode voltage during reverse polarity Channel 1, 5, 6	$V_{DS(REV)}$	400	650	800	mV	$I_L = I_{L(nom)} =$ P_6.6.18 $T_j = 150\text{ °C}$	P_7.7.21
<b>Over Voltage</b>							
Overvoltage protection	$V_{S(AZ)}$	42	47	54	V	$I_S = 4\text{ mA}$	P_7.7.22

1) Not subject to production test, specified by design.

## 8 Diagnosis

For diagnosis purpose, the SPOC+ BTS56033-LBA provides a current sense signal at pin IS and a diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

Please refer to [Figure 8-1](#) for details.



**Figure 8-1 Block Diagram: Diagnosis**

For diagnosis feedback at different operation modes, please see [Table 8-1](#).

Table 8-1 Operation Modes <sup>1)</sup>

Operation Mode	Input Level <b>OUT.OUT<sub>n</sub></b>	Output Level $V_{OUT}$	Current Sense $I_{IS}$	Error Flag <b>ERR_COUNTEN<sub>n</sub></b> <sup>2)</sup>	<b>DCR.SB</b> M bit
Normal Operation ( <b>Channel OFF</b> )	L / 0 (OFF-state)	GND	Z	0	1
Short Circuit to GND		GND	Z	0	1
Thermal shut down		Z	Z	0 <sup>2)</sup>	X
Short Circuit to $V_S$		$V_S$	Z	0	0
Open Load		Z	Z	0	X
Normal Operation ( <b>Channel ON</b> )	H / 1 (ON-state)	$\sim V_S$	$I_L / k_{ILIS}$	0	0
Current Limitation		$< V_S$	Z	0	X
Dynamic or Absolute Thermal Limitation → Channel switched OFF		Z	Z	0	X
Dynamic or Absolute Thermal Limitation $n_{retry}$ reached → Channel latched OFF		Z	Z	1 <sup>2)</sup>	X
Short Circuit to GND		$\sim$ GND	Z	0	1
Short Circuit to $V_S$		$V_S$	$< I_L / k_{ILIS}$	0	0
Open Load		$V_S$	Z	0	0

1) L = "low" level, H = "high" level, Z = high impedance, potential depends on leakage currents and external circuit.  
X = undefined.

2) The over temperature flag is set latched and can be cleared by setting **HWCR.CTC** bit to 1.

## 8.1 Diagnosis Word at SPI

Diagnostic information about the status of each channel are provided through SPI. In the Standard Diagnosis the **ERR\_MUX** bit reports if there is a channel which had already enough restarts to reach the maximum allowed number of retries  $n_{retry}$  (P\_7.7.17). If 2 or more channels are latched OFF due to that, **ERR\_MUX** bits aren't enough to identify which channels are OFF. In such cases, it is possible to get an overview channel by channel using **ERR\_COUNTER** bits in Errors Diagnosis (see [Chapter 9.6.2](#))

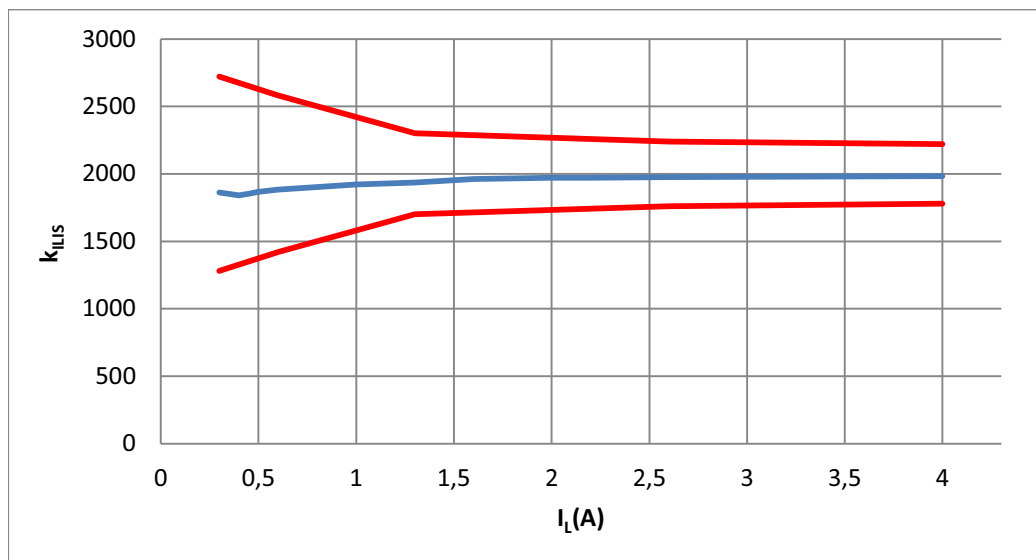
## 8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

### 8.2.1 Current Sense Signal

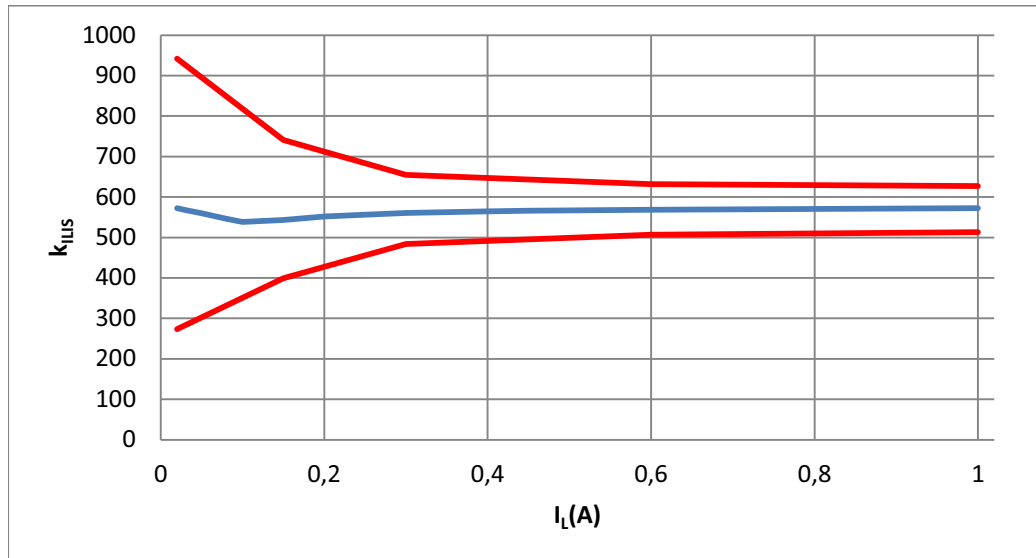
The current sense signal (ratio  $k_{ILIS} = I_L / I_S$ ) is provided during ON-state as long as no failure mode occurs. The ratio  $k_{ILIS}$  can be adjusted to the load type (LED or bulb) via SPI register LGCR. The accuracy of the ratio  $k_{ILIS}$  depends on the load current and temperature. Usually a resistor  $R_{IS}$  is connected to the current sense pin. It is recommended to use resistors  $1.5 \text{ k}\Omega < R_{IS} < 5 \text{ k}\Omega$ . A typical value is  $2.7 \text{ k}\Omega$ .

The current sense signal of a channel is not active when the channel is OFF or when the protection functions (current limitation, over temperature or dynamic temperature sensors) are active. If the maximum number of automatic reactivations  $n_{\text{retry}}$  is reached ( $n = n_{\text{retry}}$ ), the current sense signal of the affected channel is deactivated until the reset the counters by setting **HWCR.CTC** bit to 1.



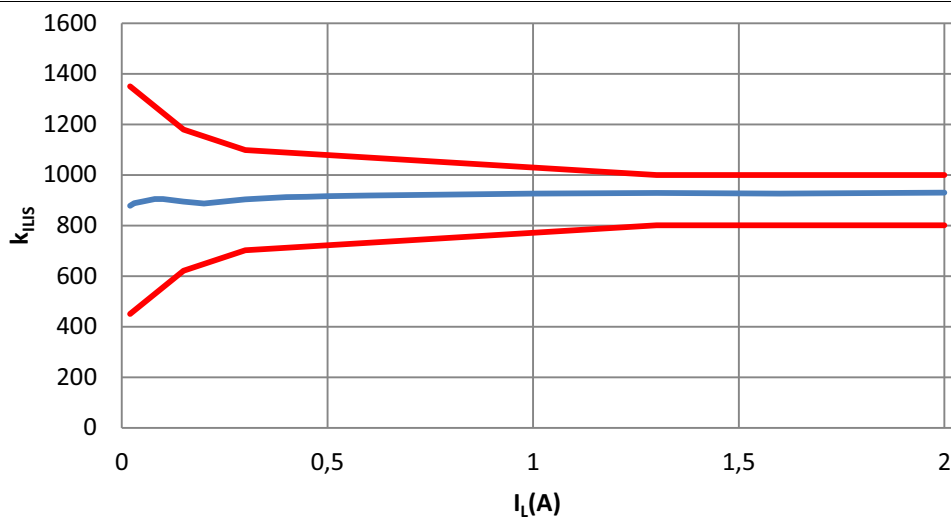
**Figure 8-2 Current Sense Ratio  $k_{ILIS}$  Channel 2, 3, 4 (Bulb mode)**

*Note: The curves show the behavior based on characterization data.*



**Figure 8-3 Current Sense Ratio  $k_{ILIS}$  Channel 2, 3, 4 (LED mode)**

*Note: The curves show the behavior based on characterization data.*



**Figure 8-4 Current Sense Ratio  $k_{ILIS}$  Channel 1, 5, 6**

*Note: The curves show the behavior based on characterization data.*

Details about timings between the current sense signal  $I_{IS}$  and the output voltage  $V_{OUT}$  and the load current  $I_L$  can be found in [Figure 8-5](#).

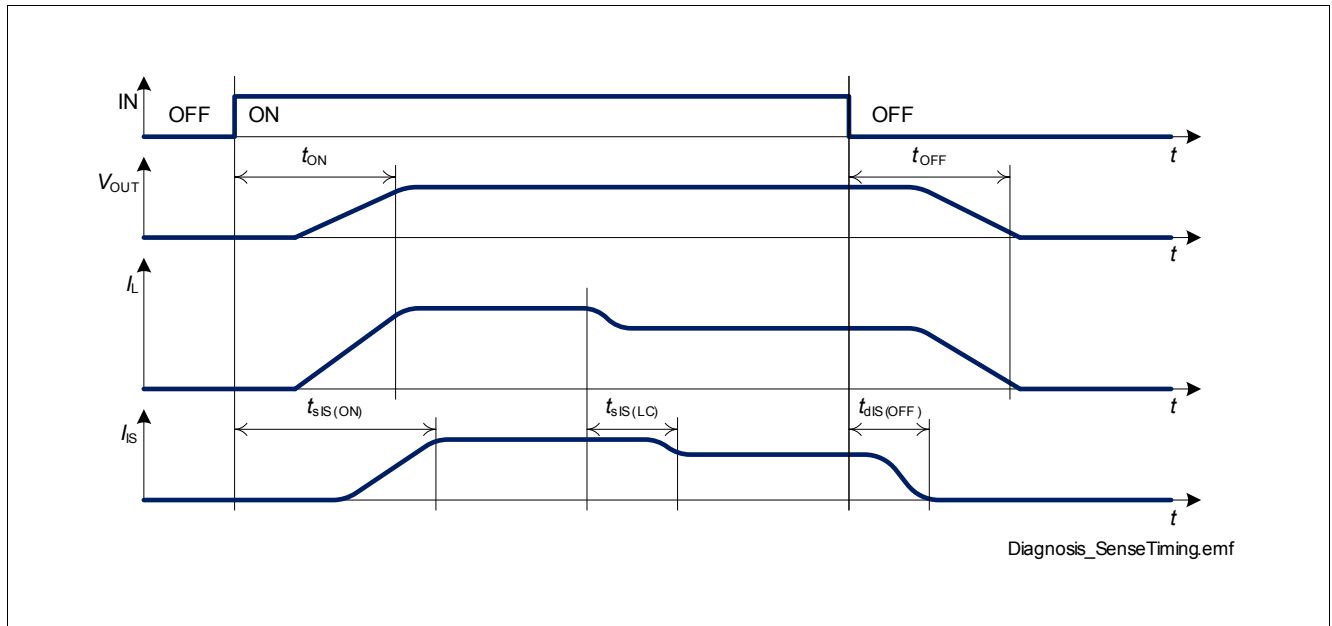


Figure 8-5 Current Sense Signal Timings

## 8.2.2 Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC+ BTS56033-LBA that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register **DCR.MUX**. The sense current also can be disabled by SPI register **DCR.MUX**. For details on timing of the current sense multiplexer, please refer to [Figure 8-6](#).

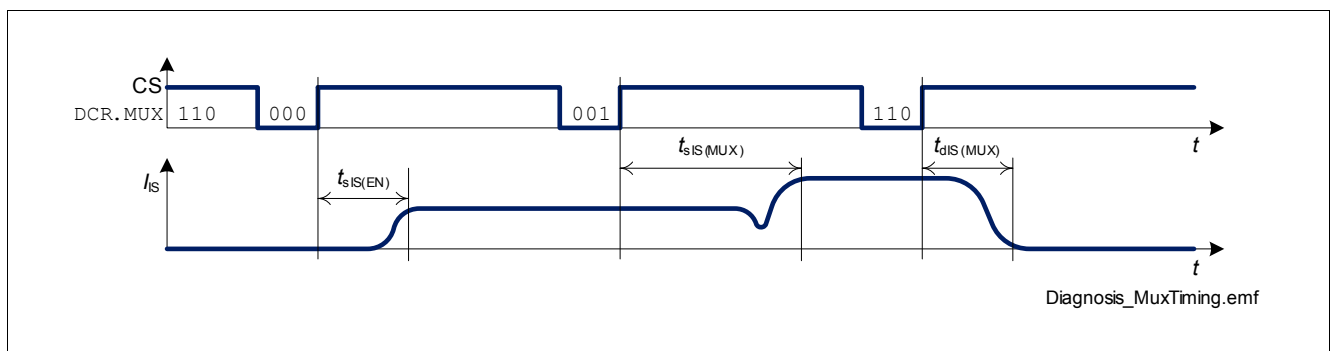


Figure 8-6 Current Sense Multiplexer Timings

## 8.3 Switch Bypass Monitor Diagnosis

To detect short circuit to  $V_S$ , there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and  $V_S$  in ON-state, the current flows through the power transistor as well as through the short circuit (bypass) with undefined share between the two. As a result, the current sense signal shows lower values than expected by the load current. In OFF-state, the output voltage remains close to  $V_S$  potential which leads to a small  $V_{DS}$ .

The switch bypass monitor compares the threshold  $V_{DS(SB)}$  with the voltage  $V_{DS}$  across the power transistor of that channel which is selected by the current sense multiplexer (**DCR.MUX**). The result of the comparison can be read in SPI register **DCR.SBM**.



## 8.4 Gate Back Regulation

To increase the current sense accuracy, the Gate Back Regulation (GBR) function is implemented. This function is active by default. According to output current, GBR function can be left active or disabled. [Table 8-2](#) indicates for which output currents this is necessary in order to fulfill the desired current accuracy.

The circuitry that controls GBR function can be deactivated with the following SPI command sequence:

- **SWCR.SWR** = 1 (11001100<sub>B</sub>)
- **LGCR.GBR**<sub>n</sub> = 0 (1101aaaa<sub>B</sub> where "aaaa"<sub>B</sub> is the new value for **LGCR.GBR** bits
- (optional but recommended: **SWCR.SWR** = 0 (11000100<sub>B</sub>))

GBR cannot be deactivated for the channels 1, 5 and 6.

Refer to [Chapter 9.7](#) for more details.

## 8.5 Electrical Characteristics

Unless otherwise specified:  $V_S = 7\text{ V to }18\text{ V}$ ,  $V_{DD} = 3.8\text{ V to }5.5\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $V_{DD} = 4.3\text{ V}$ ,  $T_j = 25\text{ °C}$

Typical resistive loads connected to the outputs (unless otherwise specified):

Channel 2, 3, 4:  $R_L = 6.8\text{ }\Omega$  ( $33\text{ }\Omega$  when **LGCR.LEDn** = 1)

Channel 1, 5, 6:  $R_L = 18\text{ }\Omega$

Measurement setup used for  $k_{ILIS}$  (unless otherwise specified):

Channel 2, 3, 4: when  $I_L \leq 1.3\text{ A}$  the channels are ON at the same time with equal  $I_L$ , channels 1, 5, 6 have  $I_L = 0$

Channel 1, 5, 6: when  $I_L \leq 1.3\text{ A}$  the channels are ON at the same time with equal  $I_L$ , channels 2, 3, 4 have  $I_L = 0$

When  $I_L \geq 2.0\text{ A}$  only the measured channel is ON, all other channels have  $I_L = 0$

**Table 8-2 Electrical Characteristics Diagnosis**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			

### Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition

#### Channel 2, 3, 4

**LGCR.LEDn** = 0

Current sense ratio $I_{L03} = 300\text{ mA}$	$k_{ILIS03}$	-36	2000	+36	%	—	P_8.5.49
Current sense ratio $I_{L05} = 600\text{ mA}$	$k_{ILIS05}$	-29	2000	+29	%	—	P_8.5.51
Current sense ratio $I_{L07} = 1.3\text{ A}$	$k_{ILIS07}$	-15	2000	+15	%	—	P_8.5.53
Current sense ratio $I_{L09} = 2.6\text{ A}$	$k_{ILIS09}$	-12	2000	+12	%	—	P_8.5.55
Current sense ratio $I_{L10} = 4\text{ A}$	$k_{ILIS10}$	-11	2000	+11	%	—	P_8.5.56

### Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition

#### Channel 2, 3, 4

**LGCR.LEDn** = 1

Current sense ratio $I_{L00} = 20\text{ mA}$	$k_{ILIS00}$	-52	620	+52	%	—	P_8.5.57
Current sense ratio $I_{L02} = 150\text{ mA}$	$k_{ILIS02}$	-30	570	+30	%	—	P_8.5.59
Current sense ratio $I_{L03} = 300\text{ mA}$	$k_{ILIS03}$	-15	570	+15	%	—	P_8.5.60
Current sense ratio $I_{L05} = 600\text{ mA}$	$k_{ILIS05}$	-11	570	+11	%	—	P_8.5.62
Current sense ratio $I_{L06} = 1\text{ A}$	$k_{ILIS06}$	-10	570	+10	%	—	P_8.5.63

### Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition

#### Channel 1, 5, 6

Table 8-2 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense ratio $I_{L00} = 20 \text{ mA}$	$k_{ILIS00}$	-50	900	+50	%	—	P_8.5.66
Current sense ratio $I_{L02} = 150 \text{ mA}$	$k_{ILIS02}$	-31	900	+31	%	—	P_8.5.68
Current sense ratio $I_{L03} = 300 \text{ mA}$	$k_{ILIS03}$	-22	900	+22	%	—	P_8.5.69
Current sense ratio $I_{L07} = 1.3 \text{ A}$	$k_{ILIS07}$	-11	900	+11	%	—	P_8.5.73
Current sense ratio $I_{L08} = 2 \text{ A}$	$k_{ILIS08}$	-11	900	+11	%	—	P_8.5.74
Sense pin maximum voltage	$V_{IS(AZ)}$	42	47	54	V	$I_{IS} = 5 \text{ mA}$	P_8.5.75

#### Current Sense Drift Over Current and Temperature per Device

Current sense drift over current and temperature per device Channel 2, 3, 4	$\Delta k_{ILIS(T)}$	-8	—	8	%	1) $k_{ILIS09}$ versus $k_{ILIS07}$ <b>LGCR.LED</b> <sub>n</sub> = 0	P_8.5.80
Current sense drift over current and temperature per device Channel 2, 3, 4	$\Delta k_{ILIS(T)}$	-9.5	—	9.5	%	1) $k_{ILIS05}$ versus $k_{ILIS03}$ <b>LGCR.LED</b> <sub>n</sub> = 1	P_8.5.81
Current sense drift over current and temperature per device Channel 1, 5, 6	$\Delta k_{ILIS(T)}$	-8	—	8	%	1) $k_{ILIS07}$ versus $k_{ILIS03}$	P_8.5.82

#### Current Sense Drift of Unaffected Channel during Inverse Current of other Channels

One channel with  $I_{L(IC)} = -I_{Ln}$ , all other channels with  $I_{Ln}$

DCR.MUX ≠ <111, 110> and set to sense any of the channels not in Inverse current condition

Current sense drift of unaffected channels during inverse current of one channel	$\Delta k_{ILIS(IC)}$	-20	—	20	%	1) $I_{L1} = 1.3 \text{ A}$ $I_{L2} = 2.6 \text{ A}$ $I_{L3} = 2.6 \text{ A}$ $I_{L4} = 2.6 \text{ A}$ $I_{L5} = 1.3 \text{ A}$ $I_{L6} = 1.3 \text{ A}$	P_8.5.85
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#### Sense Pin - Currents

Maximum steady state current sense output current Channel 2, 3, 4	$I_{IS(MAX)}$	3.8	—	15	mA	$V_{IS} = 0 \text{ V}$ $V_S \geq 8 \text{ V}$	P_8.5.88
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Table 8-2 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Maximum steady state current sense output current Channel 1, 5, 6	$I_{IS(MAX)}$	3.8	–	15	mA	$V_S = 0\text{ V}$ $V_S \geq 8\text{ V}$	P_8.5.89
Current sense leakage / offset current	$I_{IS(en)}$	–	–	3.2	$\mu\text{A}$	$I_L = 0\text{ mA}$ $LGCR\_GBR = \text{ON}$ $DCR\_MUX \neq <111,110>_B$	P_8.5.90
Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	0.01	1	$\mu\text{A}$	$I_{L2} = 2.6\text{ A}$ $DCR\_MUX = 110_B$	P_8.5.98

#### Sense Pin - Timings

Current sense settling time after channel activation Channel 2, 3, 4	$t_{sIS(ON)}$	–	–	250	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$ $LGCR\_LEDn = 0$	P_8.5.103
Current sense settling time after channel activation Channel 2, 3, 4	$t_{sIS(ON)}$	–	–	100	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$ $LGCR\_LEDn = 1$	P_8.5.104
Current sense settling time after channel activation Channel 1, 5, 6	$t_{sIS(ON)}$	–	–	250	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$	P_8.5.105
Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$	–	–	25	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$	P_8.5.106
Current sense settling time after change of load current Channel 2, 3, 4	$t_{sIS(LC)}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $I_L = 2.6\text{ A to }1.3\text{ A}$ $V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$ $LGCR\_LEDn = 0$	P_8.5.111
Current sense settling time after change of load current Channel 2, 3, 4	$t_{sIS(LC)}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $I_L = 1.0\text{ A to }0.6\text{ A}$ $V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$ $LGCR\_LEDn = 1$	P_8.5.112
Current sense settling time after change of load current Channel 1, 5, 6	$t_{sIS(LC)}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $I_L = 2.6\text{ A to }1.3\text{ A}$ $V_S = 13.5\text{ V}$ $R_{IS} = 2.7\text{ k}\Omega$	P_8.5.113

**Table 8-2 Electrical Characteristics Diagnosis (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense settling time after current sense activation	$t_{\text{slS(EN)}}$	—	—	25	$\mu\text{s}$	$R_{\text{IS}} = 2.7 \text{ k}\Omega$ $I_{\text{L2}} = 2.6 \text{ A}$ <b>DCR.MUX</b> : 110 <sub>B</sub> → 001 <sub>B</sub>	P_8.5.114
Current sense settling time after multiplexer channel change	$t_{\text{slS(MUX)}}$	—	—	25	$\mu\text{s}$	$R_{\text{IS}} = 2.7 \text{ k}\Omega$ $I_{\text{L2}} = 2.6 \text{ A}$ $I_{\text{L3}} = 4 \text{ A}$ <b>DCR.MUX</b> : 001 <sub>B</sub> → 010 <sub>B</sub>	P_8.5.115
Current sense deactivation time	$t_{\text{dlS(MUX)}}$	—	—	25	$\mu\text{s}$	<sup>1)</sup> $R_{\text{IS}} = 2.7 \text{ k}\Omega$ <b>DCR.MUX</b> : 010 <sub>B</sub> → 110 <sub>B</sub>	P_8.5.116

**Switch Bypass Monitor**

Switch bypass monitor threshold	$V_{\text{DS(SB)}}$	1.5	3.3	4.5	V	OFF state	P_8.5.117
---------------------------------	---------------------	-----	-----	-----	---	-----------	-----------

1) Not subject to production test, specified by design.

## 9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CS. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CS indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CS. A modulo 8 counter ensures that data is taken only when a multiple of 8 bit has been transferred. The interface provides daisy chain capability with 8 bit SPI devices.

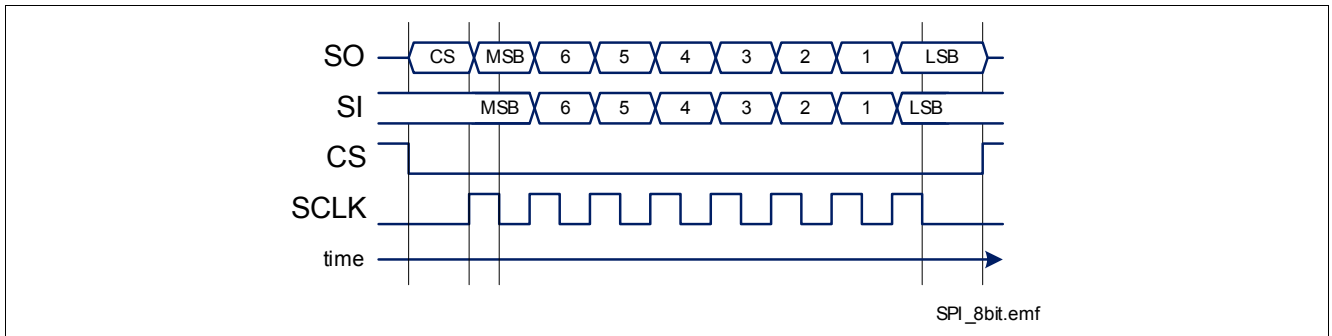


Figure 9-1 Serial Peripheral Interface

### 9.1 SPI Signal Description

#### CS - Chip Select

The system micro controller selects the SPOC+ BTS56033-LBA by means of the CS pin. Whenever the pin is in "low" state, data transfer can take place. When CS is in "high" state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

#### CS "high" to "low" Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to "high" or "low" state depending on the signal level at pin SI.

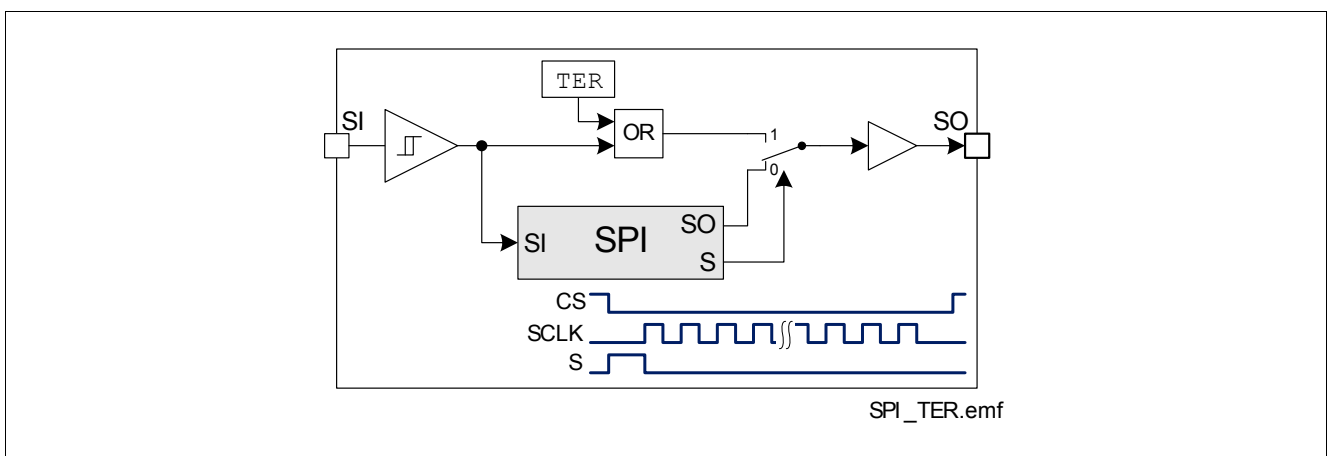


Figure 9-2 Combinatorial Logic for TER Flag

### CS "low" to "high" Transition

- Command decoding is only done, when after the falling edge of CS exactly a multiple (1, 2, 3, ...) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag ( $TER$ ) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

### SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in "low" state whenever chip select CS makes any transition, otherwise the command may be not accepted.

### SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to [Chapter 9.5](#) for further information.

### SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CS pin goes to "low" state. New data will appear at the SO pin following the rising edge of SCLK.

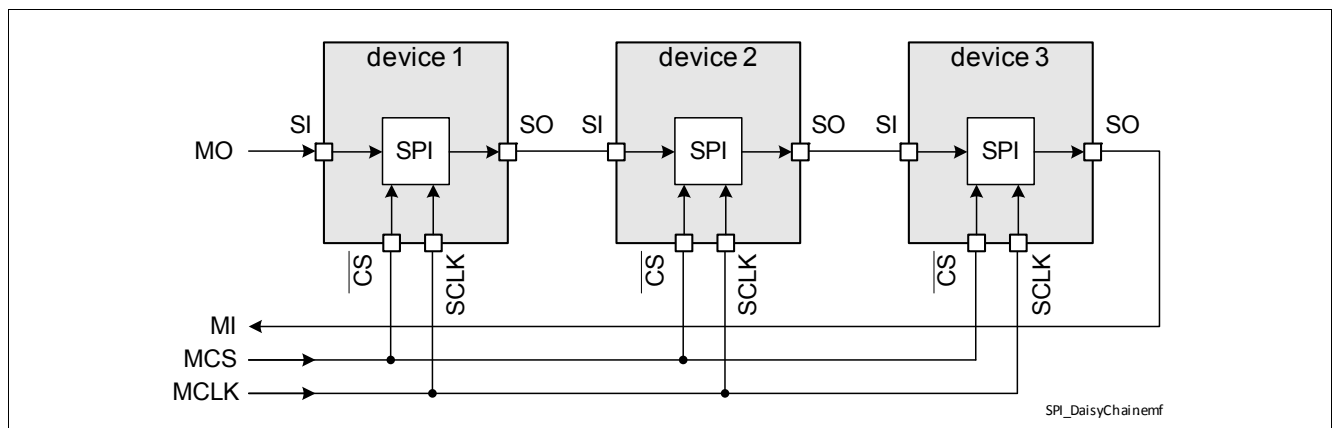
For the SPI Diagnosis readout operation the transmission error flag ( $TER$ ) appears in positions D8 and D6 on SO pin while for other readout operations it is only in position D8.

Please refer to [Chapter 9.5](#) for further information.

SO	TER	7	TER / 6	5	4	3	2	1	0
----	-----	---	---------	---	---	---	---	---	---

## 9.2 Daisy Chain Capability

The SPI of SPOC+ BTS56033-LBA provides daisy chain capability. In this configuration several devices are activated by the same CS signal MCS. The SI line of one device is connected with the SO line of another device (see [Figure 9-3](#)), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.



**Figure 9-3** Daisy Chain Configuration

## Serial Peripheral Interface (SPI)

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CS line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCS line must turn “high” (see [Figure 9-4](#)).

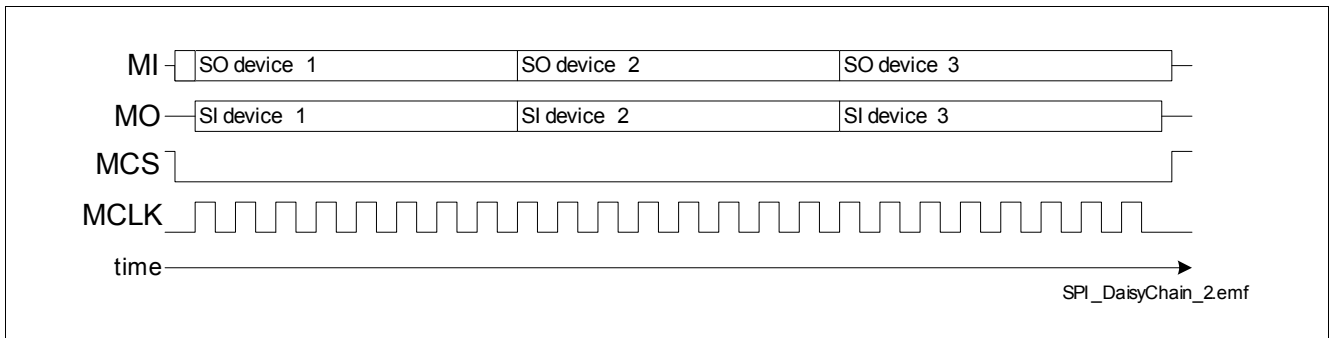


Figure 9-4 Data Transfer in Daisy Chain Configuration

### 9.3 Timing Diagrams

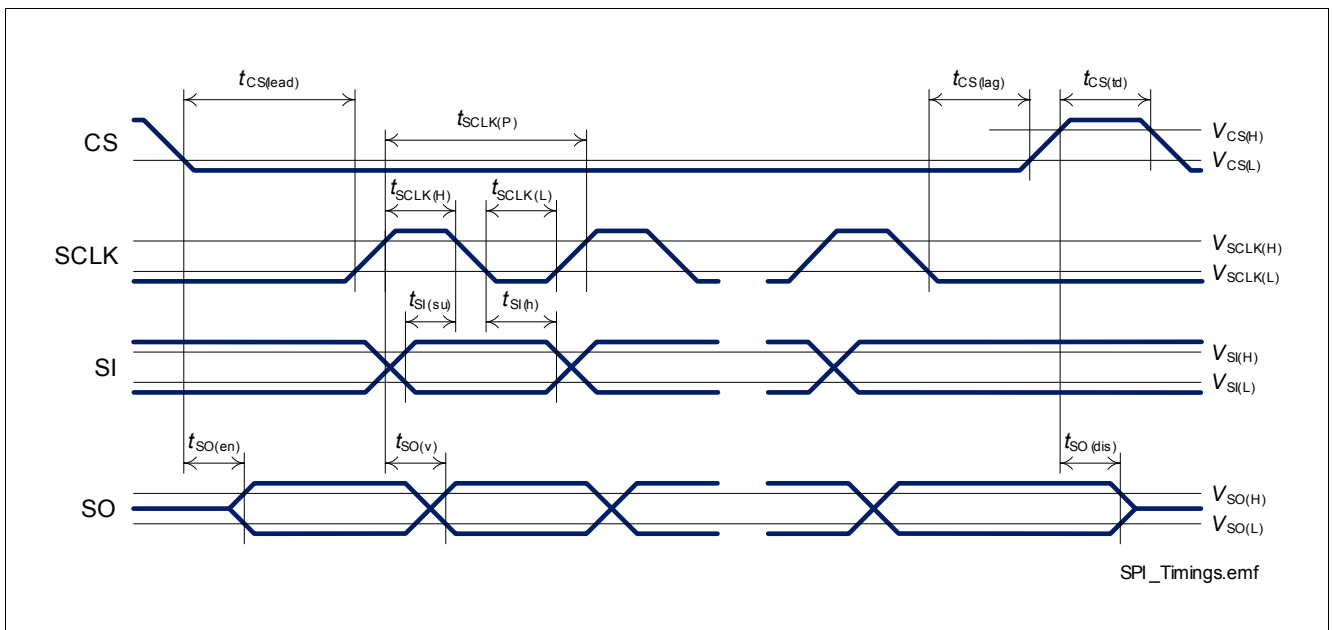


Figure 9-5 Timing Diagram SPI Access



## Serial Peripheral Interface (SPI)

## 9.4 Electrical Characteristics

Unless otherwise specified:  $V_S = 7\text{ V}$  to  $18\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.8\text{ V}$  to  $5.5\text{ V}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 4.3\text{ V}$

**Table 9-1 Electrical Characteristics Serial Peripheral Interface (SPI)**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CS, SCLK, SI) - L Level of pin							
CS	$V_{CS(L)}$	-0.3	—	1.0	V	$V_{DD} = 4.3\text{ V}$	P_9.4.1
SCLK	$V_{SCLK(L)}$	-0.3	—	1.0	V	$V_{DD} = 4.3\text{ V}$	P_9.4.2
SI	$V_{SI(L)}$	-0.3	—	1.0	V	$V_{DD} = 4.3\text{ V}$	P_9.4.3
Input Characteristics (CS, SCLK, SI) - H Level of pin							
CS	$V_{CS(H)}$	2.6	—	$V_{DD}$	V	$V_{DD} = 4.3\text{ V}$	P_9.4.4
SCLK	$V_{SCLK(H)}$	2.6	—	$V_{DD}$	V	$V_{DD} = 4.3\text{ V}$	P_9.4.5
SI	$V_{SI(H)}$	2.6	—	$V_{DD}$	V	$V_{DD} = 4.3\text{ V}$	P_9.4.6
L-input pull-up current at CS pin	$-I_{CS(L)}$	7	30	75	μA	$V_{DD} = 4.3\text{ V}$ $V_{CS} = 1.0\text{ V}$	P_9.4.7
H-input pull-up current at CS pin	$-I_{CS(H)}$	3	27	75	μA	$V_{DD} = 4.3\text{ V}$ $V_{CS} = 2.6\text{ V}$	P_9.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	3	27	75	μA	$V_{SCLK} = 1.0\text{ V}$ $V_{DD} = 4.3\text{ V}$	P_9.4.9
SI	$I_{SI(L)}$	3	27	75	μA	$V_{SI} = 1.0\text{ V}$ $V_{DD} = 4.3\text{ V}$	P_9.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	7	30	75	μA	$V_{SCLK} = 2.6\text{ V}$ $V_{DD} = 4.3\text{ V}$	P_9.4.11
SI	$I_{SI(H)}$	7	30	75	μA	$V_{SI} = 2.6\text{ V}$ $V_{DD} = 4.3\text{ V}$	P_9.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	—	0.5	V	$I_{SO} = -0.5\text{ mA}$	P_9.4.13
H level output voltage	$V_{SO(H)}$	$V_{DD} - 0.5\text{ V}$	—	$V_{DD}$	V	$I_{SO} = 0.5\text{ mA}$ $V_{DD} = 4.3\text{ V}$	P_9.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	—	1	μA	$V_{CS} = V_{DD}$ $V_{SO} = 0\text{ V}$ $V_{SO} = V_{DD}$	P_9.4.15
Timings							
Enable lead time (falling CS to rising SCLK)	$t_{CS(lead)}$	200	—	—	ns	— <sup>1)</sup>	P_9.4.16
Enable lag time (falling SCLK to rising CS)	$t_{CS(lag)}$	200	—	—	ns	— <sup>1)</sup>	P_9.4.17
Transfer delay time (rising CS to falling CS)	$t_{CS(td)}$	1	—	—	μs	— <sup>1)</sup>	P_9.4.18

## Serial Peripheral Interface (SPI)

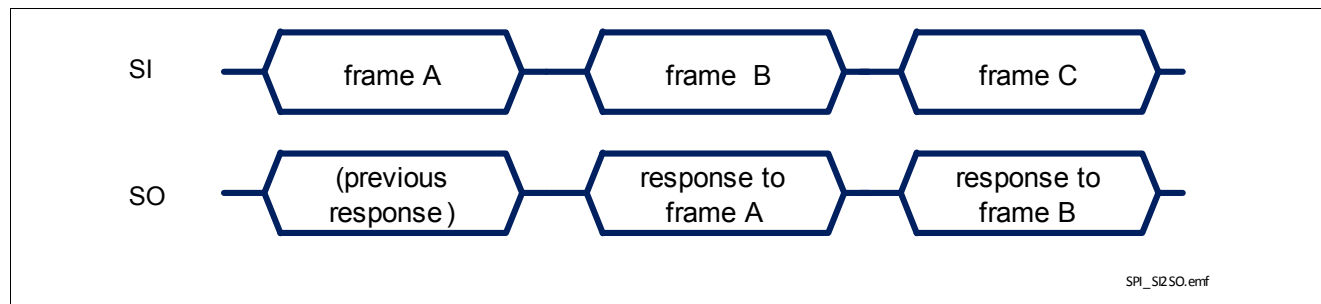
**Table 9-1 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output enable time (falling CS to SO valid)	$t_{SO(en)}$	–	–	1	$\mu s$	<sup>1)</sup> $C_L = 20 \text{ pF}$	P_9.4.19
Output disable time (rising CS to SO tristate)	$t_{SO(dis)}$	–	–	1	$\mu s$	<sup>1)</sup> $C_L = 20 \text{ pF}$	P_9.4.20
Serial clock frequency	$f_{SCLK}$	0	–	2.5	MHz	– <sup>1)</sup>	P_9.4.22
Serial clock period	$t_{SCLK(P)}$	400	–	–	ns	– <sup>1)</sup>	P_9.4.24
Serial clock “high” time	$t_{SCLK(H)}$	200	–	–	ns	– <sup>1)</sup>	P_9.4.26
Serial clock “low” time	$t_{SCLK(L)}$	200	–	–	ns	– <sup>1)</sup>	P_9.4.28
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	80	–	–	ns	– <sup>1)</sup>	P_9.4.30
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	80	–	–	ns	– <sup>1)</sup>	P_9.4.32
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	200	ns	<sup>1)</sup> $C_L = 20 \text{ pF}$	P_9.4.34

1) Not subject to production test, specified by design

## 9.5 SPI Protocol

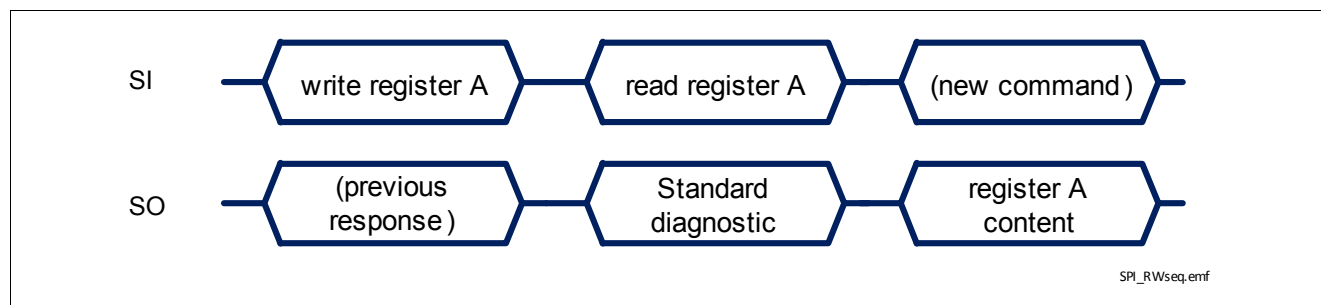
The relationship between SI and SO content during SPI communication is shown in [Figure 9-6](#). SI line represents the frame sent from the  $\mu\text{C}$  and SO line is the answer provided by SPOC+ BTS56033-LBA. The “(previous response)” means that the frame sent back depends on the command frame sent from the  $\mu\text{C}$  before.



**Figure 9-6 Relationship between SI and SO during SPI communication**

The SPI protocol will provide the answer to a command frame only with the next transmission triggered by the  $\mu\text{C}$ . Although the biggest majority of commands and frames implemented in SPOC+ BTS56033-LBA can be decoded without the knowledge of what happened before, it is advisable to consider what the  $\mu\text{C}$  sent in the previous transmission to decode SPOC+ BTS56033-LBA response frame completely.

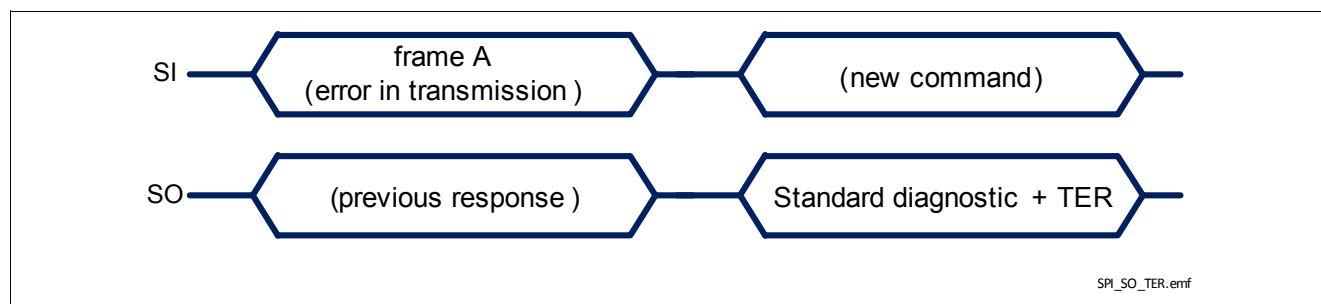
More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:



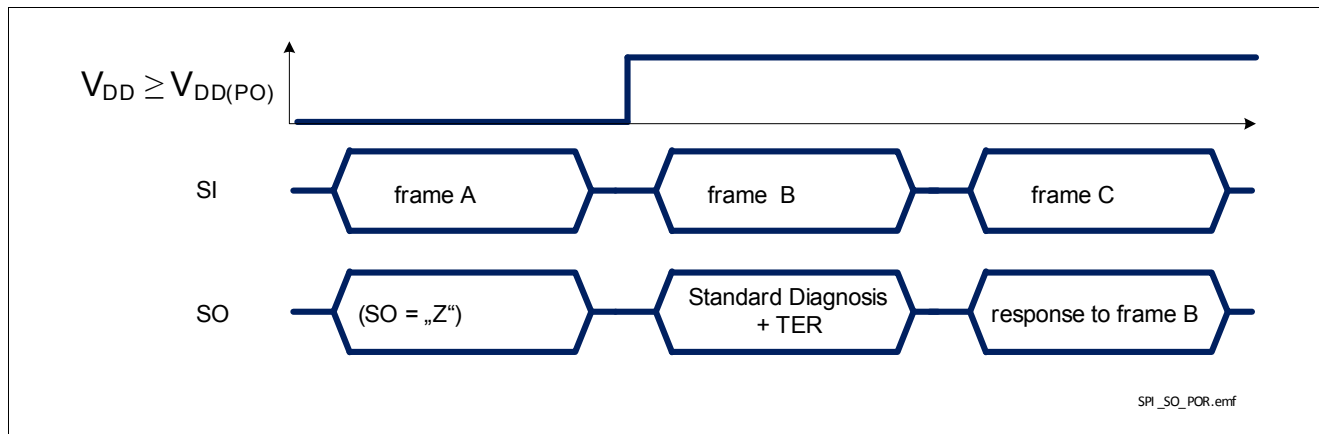
**Figure 9-7 Register content sent back to  $\mu\text{C}$**

There are 2 special situations where the frame sent back to the  $\mu\text{C}$  doesn't depend on the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8), shown in [Figure 9-8](#)
- when BTS56033-LBA logic supply comes out of Power-On reset condition, as shown in [Figure 9-9](#)



**Figure 9-8 BTS56033-LBA response after a error in transmission**



**Figure 9-9** BTS56033-LBA response after coming out of Power-On reset at  $V_{DD}$

A summary of all possible SPI commands is presented in [Table 9-2](#), including the answer that SPOC+ BTS56033-LBA will send back at the next transmission.

**Table 9-2** SPI Command summary

Requested Operation	Frame sent to SPOC+ (SI pin)	Frame received from SPOC+ (SO pin) with the next command
Write OUT register	10aaaaaa <sub>B</sub> where: “aaaaaa <sub>B</sub> ” = new OUT register content	0aaaaaaa <sub>B</sub> (Standard Diagnosis)
Read OUT register	00xx0000 <sub>B</sub> (“xx <sub>B</sub> ” = don’t care)	10aaaaaa <sub>B</sub> (“aaaaaa <sub>B</sub> ” = OUT register content)
Write Configuration register	11aabbbb <sub>B</sub> where: “aa <sub>B</sub> ” = register address “bbbb <sub>B</sub> ” = new register content	0aaaaaaa <sub>B</sub> (Standard Diagnosis)
Read Configuration register	01aa0000 <sub>B</sub> where: “aa <sub>B</sub> ” = register address	11aabbbb <sub>B</sub> where: “aa <sub>B</sub> ” = register address “bbbb <sub>B</sub> ” = register content
Read Standard Diagnosis	0xxx0001 <sub>B</sub> (“xxx <sub>B</sub> ” = don’t care)	0aaaaaaa <sub>B</sub> (Standard Diagnosis)
Read Error Diagnosis	0xxx0011 <sub>B</sub> (“xxx <sub>B</sub> ” = don’t care)	00aaaaaa <sub>B</sub> (Errors Diagnosis)

## 9.6 SPI Diagnosis Registers

### 9.6.1 Standard Diagnosis

SO	7	6	5	4	3	2	1	0	Default
----	---	---	---	---	---	---	---	---	---------

0	TER	LHI	STB	VSMON	ERR_MUX				50 <sub>H</sub>
---	-----	-----	-----	-------	---------	--	--	--	-----------------

Field	Bits	Type	Description
TER	6	r	<b>Transmission Error</b> 0 <sub>B</sub> (default) Previous transmission was successful (modulo 8 clocks received) 1 <sub>B</sub> Previous transmission failed or first transmission after reset
LHI	5	r	<b>Limp Home monitor</b> 0 <sub>B</sub> (default) Normal mode operation 1 <sub>B</sub> Limp Home Mode
STB	4	r	<b>Standby mode monitor</b> 0 <sub>B</sub> (default) Normal mode operation 1 <sub>B</sub> Standby mode
VSMON	3	r	<b><math>V_S</math> monitor</b> 0 <sub>B</sub> (default) $V_S$ always > $V_{SMON}$ since last Standard Diagnosis readout 1 <sub>B</sub> $V_S < V_{SMON}$ at least once
ERR_MUX	X	r	<b>Diagnosis of Channel n in error</b> 000 <sub>B</sub> (default) No latch off 001 <sub>B</sub> Channel one latch off 010 <sub>B</sub> Channel two latch off 011 <sub>B</sub> Channel three latch off 100 <sub>B</sub> Channel four latch off 101 <sub>B</sub> Channel five latch off 110 <sub>B</sub> Channel six latch off 111 <sub>B</sub> More than one channel latch off

#### Notes:

- $V_S$  monitoring is disabled in Stand-by mode (MUX = „111“) to allow SPI configuration without  $V_S$  voltage applied.
- As long as  $V_S < V_{SMON}$  the SPI command is not taken over by the SPI. TER and VSMON bits are set.

## 9.6.2 Errors Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	0	ERR_CO UNTER6		ERR_CO UNTER4	ERR_CO UNTER3	ERR_CO UNTER2	ERR_CO UNTER1	00 <sub>H</sub>

Field	Bits	Type	Description
ERR_COUNTERn n = 6 to 1	X	r	<b>Diagnosis of Channel n</b> 0 <sub>B</sub> (default) No failure 1 <sub>B</sub> Over temperature counter reached to $n_{\text{retry}}$

## 9.7 SPI Configuration Registers

### 9.7.1 Output Configuration Register

**SWCR.SWR = 0**

Bit	7	6	5	4	3	2	1	0	
Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	5	4	3	2	1	0	Default
OUT	W/R	0	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	80 <sub>H</sub>

**SWCR.SWR = 1**

Bit	7	6	5	4	3	2	1	0	
Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	5	4	3	2	1	0	Default
OUT	R	0	LHI	1	INST4	INST3	INST2	INST1	90 <sub>H</sub>

### 9.7.2 Swap Configuration Register

Bit	7	6	5	4	3	2	1	0	Default
Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	ADDR		3	2	1	0	
SWCR	W/R	1	0	0	SWR	1	0	0	C4 <sub>H</sub>

### 9.7.3 LED Mode Configuration Register

**SWCR.SWR = 0**

Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	ADDR		3	2	1	0	Default
LGCR	W/R	1	0	1	LED4	LED3	LED2	0	D0 <sub>H</sub>

### 9.7.4 Gate Back Regulation Register

**SWCR.SWR = 1**

Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	ADDR		3	2	1	0	Default
LGCR	W/R	1	0	1	GBR4	GBR3	GBR2	0	DE <sub>H</sub>

### 9.7.5 Hardware Configuration Register

Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	ADDR		3	2	1	0	Default
HWCR	R	1	1	0	RCR	COL	STB	0	E2 <sub>H</sub>
	W	1	1	0	RCR	COL	RST	CTC	-



## 9.7.6 Diagnosis Control Register

Name	$\overline{W} = 1$ $\overline{R} = 0$	RB	ADDR		3	2	1	0	Default
DCR	R	1	1	1	SBM	MUX			F7 <sub>H</sub>
	W	1	1	1	0	MUX			-

Field	Bits	Type	Description
RB	6	rw	<b>Register Bank</b> 0 <sub>B</sub> (default) Read / write to the OUTn channel 1 <sub>B</sub> Read / write to the other register
OUT.OUTn n = 6 to 1	n-1	rw	<b>Output Control Register of Channel n<sup>1)</sup></b> 0 <sub>B</sub> (default) OFF 1 <sub>B</sub> ON
OUT.INSTn n = 4 to 1	n-1	r	<b>Input Status Monitor Channel n</b> 0 <sub>B</sub> (default) Input signal "low" 1 <sub>B</sub> Input signal "high"
LGCR.LEDn n = 4 to 2	n-1	rw	<b>Set LED Mode for Channel n<sup>2)</sup></b> 0 <sub>B</sub> (default) Channel n is in bulb mode 1 <sub>B</sub> Channel n is in LED mode
LGCR.GBRn n = 4 to 2	n-1	rw	<b>Gate Back Regulation for Channel n</b> 0 <sub>B</sub> Gate back regulation for Channel n is forced OFF 1 <sub>B</sub> (default) Gate back regulation for Channel n is active
HWCR.CTC	0	w	<b>Clear Thermal Counter</b> 0 <sub>B</sub> (default) Thermal and over current latches are untouched 1 <sub>B</sub> Command: Clear all thermal and over current latches
HWCR.RST	1	w	<b>Reset Command</b> 0 <sub>B</sub> (default) Normal operation 1 <sub>B</sub> Execute reset command
HWCR.STB	1	r	<b>Standby Mode</b> 0 <sub>B</sub> Device is awake 1 <sub>B</sub> (default) Device is in Standby mode
HWCR.COL	2	rw	<b>Input Combinatorial Logic Configuration</b> 0 <sub>B</sub> (default) Input signal OR-combined with according OUT register bit <sup>3)</sup> 1 <sub>B</sub> Input signal AND-combined with according OUT register bit
HWCR.RCR	3	w	<b>Retry Counter Reset</b> 0 <sub>B</sub> (default) Retry Counter is reset only for <b>HWCR.CTC</b> =1 (and $V_{DD}$ reset) 1 <sub>B</sub> Retry Counter is reset for every IN-pin or OUT-bit "high" to "low" transition for nretry < 8 and also for <b>HWCR.CTC</b> =1 (and $V_{DD}$ reset)
SWCR.SWR	1	rw	<b>Switch Register</b> 0 <sub>B</sub> (default) LED and OUT transmitted 1 <sub>B</sub> GBR and INST transmitted

## Serial Peripheral Interface (SPI)

Field	Bits	Type	Description
DCR.SBM	3	r	<b>Switch Bypass Monitor<sup>3)</sup></b> $0_B \quad V_{DS} < V_{DS(SB)}$ $1_B \quad V_{DS} > V_{DS(SB)}$
DCR.MUX	2:0	rw	<b>Set Current Sense Multiplexer Configuration in OFF-state</b> $000_B$ IS pin is high impedance $001_B$ IS pin is high impedance $010_B$ IS pin is high impedance $011_B$ IS pin is high impedance $100_B$ IS pin is high impedance $101_B$ IS pin is high impedance $110_B$ IS pin is high impedance $111_B$ Stand-by mode (IS pin is high impedance)  <b>Set Multiplexer Configuration in ON-state</b> $000_B$ Current sense of channel 1 is routed to IS pin $001_B$ Current sense of channel 2 is routed to IS pin $010_B$ Current sense of channel 3 is routed to IS pin $011_B$ Current sense of channel 4 is routed to IS pin $100_B$ Current sense of channel 5 is routed to IS pin $101_B$ Current sense of channel 6 is routed to IS pin $110_B$ IS pin is high impedance $111_B$ Stand-by mode (IS pin is high impedance))

- 1) If **SWCR.SWR** = 1 every readout of the register shows the state of the channels' input pins (**OUT.INST** bits).
- 2) if **SWCR.SWR** = 1 every read or write operation done on the register will affect **LGCR.GBR** bits instead of **LGCR.LED** bits
- 3) In Limp Home Mode (LHI = 1) the combinatorial logic is switched to OR-mode.

## 9.8 SPI Registers Overview

Address	Name	Description
00	SWCR	<b>Swap Configuration Register</b>
01	LGCR	<b>LED Mode configuration Register</b> if <b>SWCR.SWR</b> = 0
		<b>Gate Back Regulation Register</b> if <b>SWCR.SWR</b> = 1
10	HWCR	<b>Hardware Configuration Register</b>
11	DCR	<b>Diagnosis Control Register</b>

Bit	7	6	5	4	3	2	1	0		
Name	$\overline{W} = 1$ $\overline{R} = 0$								SWR	Default

SWCR	W/R	1	0	0	SWR	1	0	0	-	C4 <sub>H</sub>
------	-----	---	---	---	-----	---	---	---	---	-----------------

OUT	W/R	0	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	0	80 <sub>H</sub>
-----	-----	---	------	------	------	------	------	------	---	-----------------

OUT	R	0	LHI	1	INST4	INST3	INST2	INST1	1	90 <sub>H</sub>
-----	---	---	-----	---	-------	-------	-------	-------	---	-----------------

LGCR	W/R	1	0	1	LED4	LED3	LED2	0	0	D0 <sub>H</sub>
------	-----	---	---	---	------	------	------	---	---	-----------------

LGCR	W/R	1	0	1	GBR4	GBR3	GBR2	0	1	DE <sub>H</sub>
------	-----	---	---	---	------	------	------	---	---	-----------------

HWCR	R	1	1	0	RCR	COL	STB	0	-	E2 <sub>H</sub>
	W	1	1	0	RCR	COL	RST	CTC	-	-

DCR	R	1	1	1	SBM	MUX			-	F7 <sub>H</sub>
	W	1	1	1	0	MUX			-	-

STD_DIAG	0	TER	LHI	STB	VSMON	ERR_MUX			-	50 <sub>H</sub>
----------	---	-----	-----	-----	-------	---------	--	--	---	-----------------

DIAG_ERR_COUNTER	0	0	ERR_C OUNTE R6	ERR_C OUNTE R5	ERR_C OUNTE R4	ERR_C OUNTE R3	ERR_C OUNTE R2	ERR_C OUNTE R1	-	00 <sub>H</sub>
------------------	---	---	----------------------	----------------------	----------------------	----------------------	----------------------	----------------------	---	-----------------

## 10 Application Description

The following Figure describes a typical operating circuit. It shall not be considered as a warranty of a certain functionality, condition or quality of the device. The [Table 10-1](#) shows suggested component values and purposes.

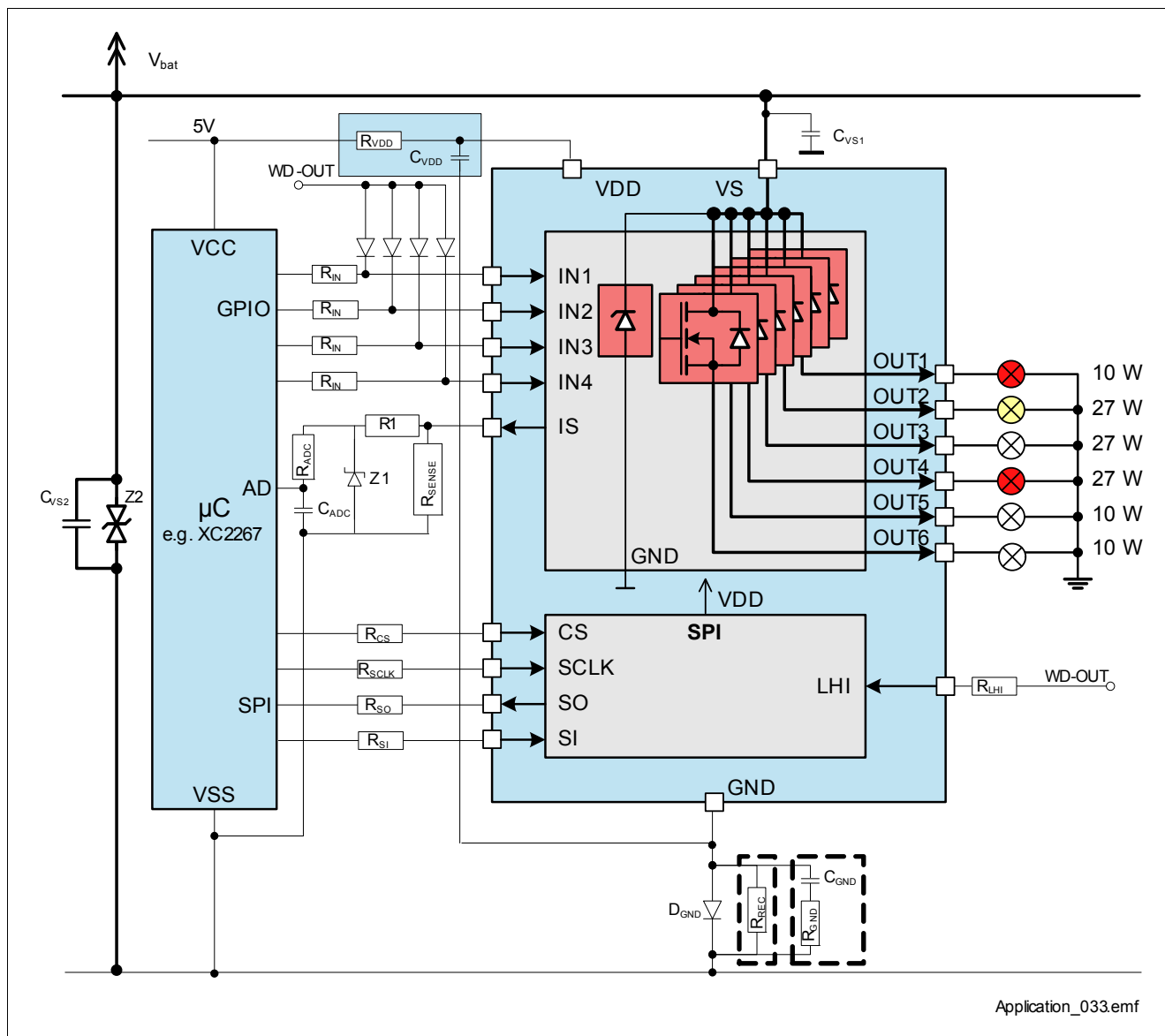
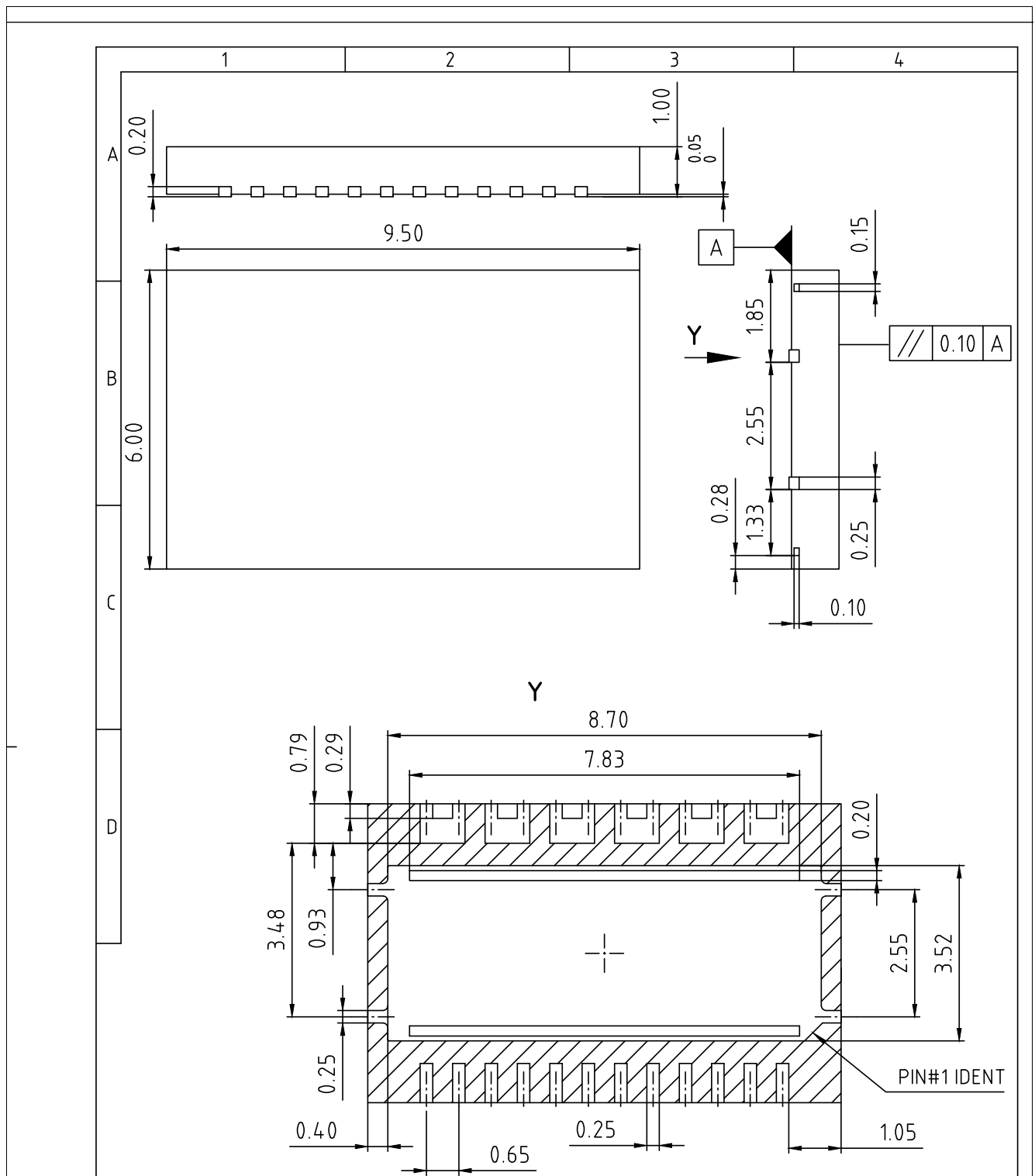


Figure 10-1 Application Circuit Example

**Table 10-1 Suggested Component values**

Reference	Value	Purpose
$R_{VDD}$	500 $\Omega$	Device logic protection
$R_{IN}$	8 k $\Omega$	Protection of the $\mu C$ during overvoltage, reverse polarity and loss of ground
$R_1$	4.7 k $\Omega$	Protection resistor for overvoltage, reverse polarity and loss of ground. Value to be tuned with $\mu C$ specification
$R_{IS}$	2.7 k $\Omega$	Sense resistor
$R_{ADC}$	1 k $\Omega$	$\mu C$ -ADC voltage spikes filtering
$R_{CS}$	3.9 k $\Omega$	Protection of the $\mu C$ during overvoltage and reverse polarity
$R_{SCLK}$	3.9 k $\Omega$	Protection of the $\mu C$ during overvoltage and reverse polarity
$R_{SO}$	3.9 k $\Omega$	Protection of the $\mu C$ during overvoltage and reverse polarity
$R_{SI}$	3.9 k $\Omega$	Protection of the $\mu C$ during overvoltage and reverse polarity
$R_{LHI}$	8 k $\Omega$	Protection of the $\mu C$ during overvoltage and reverse polarity
$C_{ADC}$	1 nF	$\mu C$ -ADC voltage spikes filtering
$C_{VDD}$	100 nF	Logic supply voltage spikes filtering
$C_{VS1}$	68 nF	Battery voltage spikes filtering
$C_{VS2}$	100 nF	Battery voltage spikes filtering
$C_{GND}$	8.2 nF	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
$R_{GND}$	100 $\Omega$	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
$R_{REC}$	1 k $\Omega$	Ground voltage recycling path (optional for providing a recycle path in case of loss of Battery)
$Z_1$	7 V	Protection of $\mu C$ during overvoltage. Zener diode
$Z_2$	P6SMB30	Protection of device during overvoltage. Zener diode
D	BAS70	Protection of device during reverse polarity. Schottky diode

## 11 Package Outlines SPOC+ BTS56033-LBA



**Figure 11-1 TSON-24-3 Package drawing**

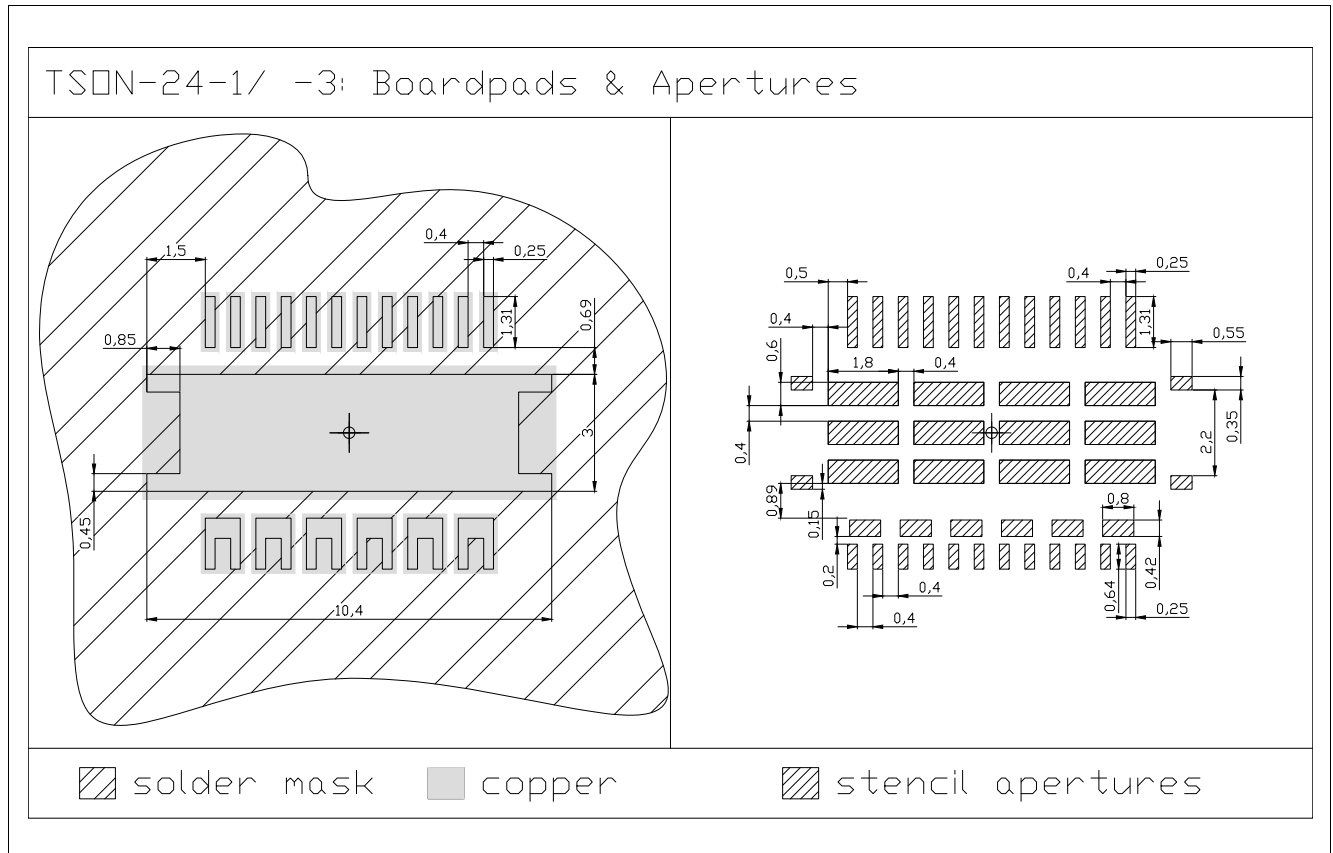


Figure 11-2 TSON-24-3 Package pads and stencil

### Green Product (RoHS Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

*Note: You can find all of our packages, sorts of packing and others in our Infineon Internet Page*

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