Dual D-type flip-flop with set and reset; positive-edge trigger

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

GENERAL DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	11 14 14	ns
f_{max}	maximum clock frequency		76	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74LV74N	14	DIL	plastic	SOT27
74LV74D	14	SO	plastic	SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

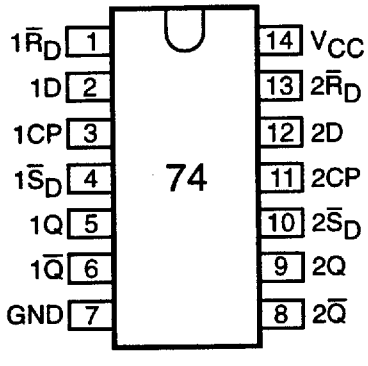

Fig.1 Pin configuration.

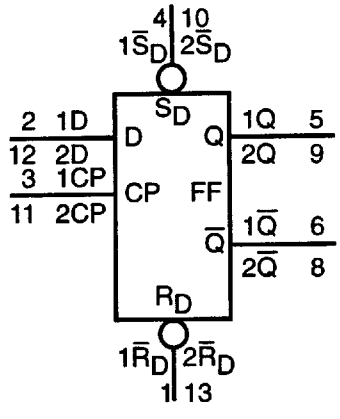

Fig.2 Logic symbol.

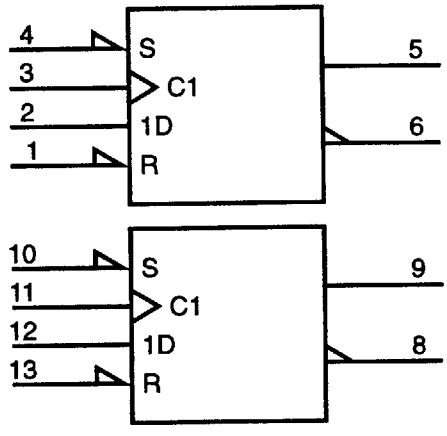

Fig.3 IEC Logic symbol.

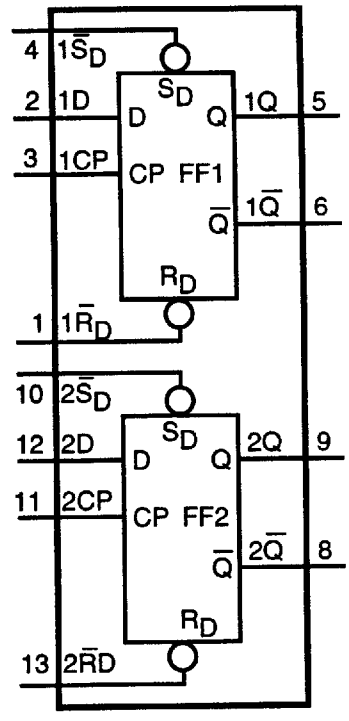

Fig.4 Functional diagram.

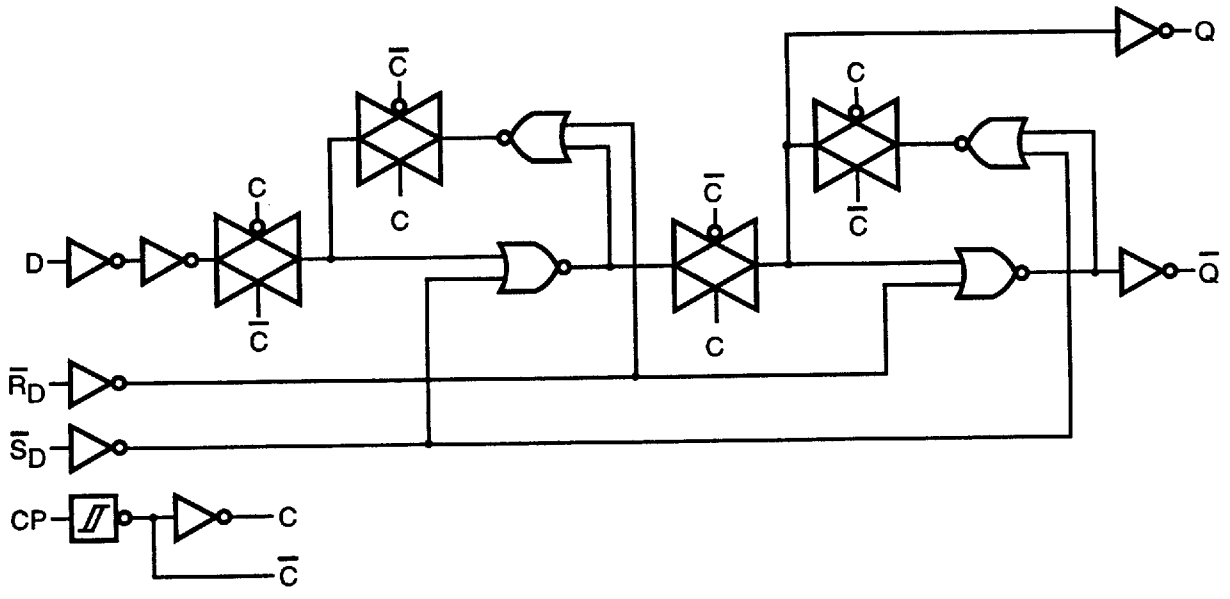

Fig.5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74LV74

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LV74

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	–	70	–	–	–	ns	1.2	Fig. 6
		–	24	48	–	54		2.0	
		–	18	35	–	40		2.7	
		–	13*	28	–	32		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	–	90	–	–	–	ns	1.2	Fig. 7
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	–	90	–	–	–	ns	1.2	Fig. 7
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig. 6
		25	8	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_W	set or reset pulse width LOW	34	10	–	41	–	ns	2.0	Fig. 7
		25	8	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_{rem}	removal time set or reset	–	5	–	–	–	ns	1.2	Fig. 7
		14	2	–	15	–		2.0	
		10	1	–	11	–		2.7	
		8	1*	–	9	–		3.0 to 3.6	
t_{su}	set-up time nD to nCP	–	10	–	–	–	ns	1.2	Fig. 6
		22	4	–	26	–		2.0	
		16	3	–	19	–		2.7	
		13	2*	–	15	–		3.0 to 3.6	
t_h	hold time nD to nCP	–	−10	–	–	–	ns	1.2	Fig. 6
		3	−2	–	3	–		2.0	
		3	−2	–	3	–		2.7	
		3	−2*	–	3	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig. 6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

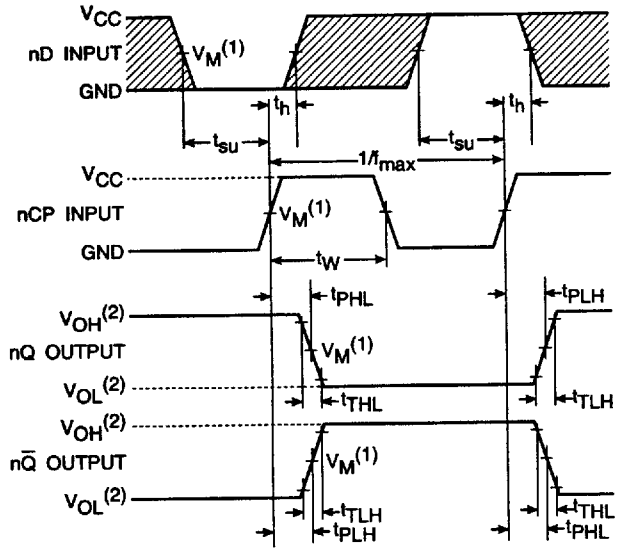

Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up times, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

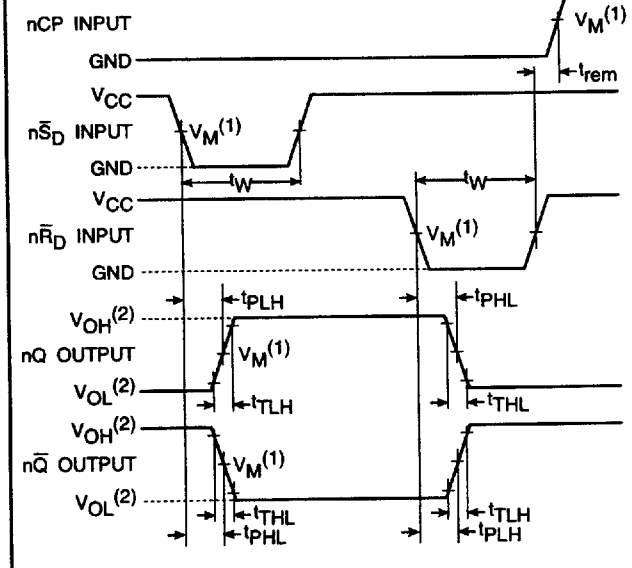

Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$ to nCP removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.