



# IP4770/71/72CZ16

VGA/video interface with integrated buffers, ESD protection and integrated termination resistors

Rev. 2 — 19 May 2011

Product data sheet

## 1. General description

The IP4770CZ16, IP4771CZ16, IP4772CZ16 is connected between the VGA/DVI interface and the video graphics controller and includes level shifting for the DDC signals, buffering for the SYNC lines as well as high-level ESD protection diodes for the RGB signal lines.

The level shifting functions are required when the DDC controller operates at a lower supply voltage than the monitor. To use this level shifting function the gates of the two N-channel MOSFETs have to be connected to the supply rail of the DDC transceivers.

Buffering for the SYNC signals is provided by two non-inverting buffers, which accept TTL input levels and convert these to CMOS compliant output levels between pins  $V_{CC(SYNC)}$  and GND.

The IP4770CZ16 and IP4771CZ16 contain the formerly external termination resistors, which are typically required for the HSYNC and VSYNC lines of the video interface:

- IP4770CZ16:  $R_{sync} = 55 \Omega$
- IP4771CZ16:  $R_{sync} = 65 \Omega$
- IP4772CZ16:  $R_{sync} = 10 \Omega$  to allow termination of the SYNC lines

All RGB I/Os are protected by a special diode configuration offering a low line capacitance of 4 pF (maximum) only to provide protection to downstream components for ESD voltages as high as  $\pm 8$  kV contact discharge according to IEC 61000-4-2, level 4 standard.

## 2. Features and benefits

- Integrated high-level ESD protection, buffering, SYNC signal impedance matching and level shifting
- Terminal connections with integrated rail-to-rail clamping diodes with downstream ESD protection of  $\pm 8$  kV according to IEC 61000-4-2, level 4 standard
- Backflow protection on DDC lines
- Drivers for HSYNC and VSYNC lines
- Bidirectional level shifting N-channel FETs available for DDC clock and DDC data channels
- Integrated impedance matching resistors on SYNC lines
- Line capacitance < 4 pF per channel
- Lead-free package and RoHS compliant



### 3. Applications

- To terminate and to buffer channels, to reduce EMI/RFI and to provide downstream ESD protection for:
  - ◆ VGA interfaces including DDC channels
  - ◆ Desktop and notebooks PCs
  - ◆ Graphics cards
  - ◆ Set-top boxes

### 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4770CZ16	SSOP16	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
IP4771CZ16			
IP4772CZ16			

### 5. Marking

Table 2. Marking codes

Type number	Marking code
IP4770CZ16	4770
IP4771CZ16	4771
IP4772CZ16	4772

6. Functional diagram

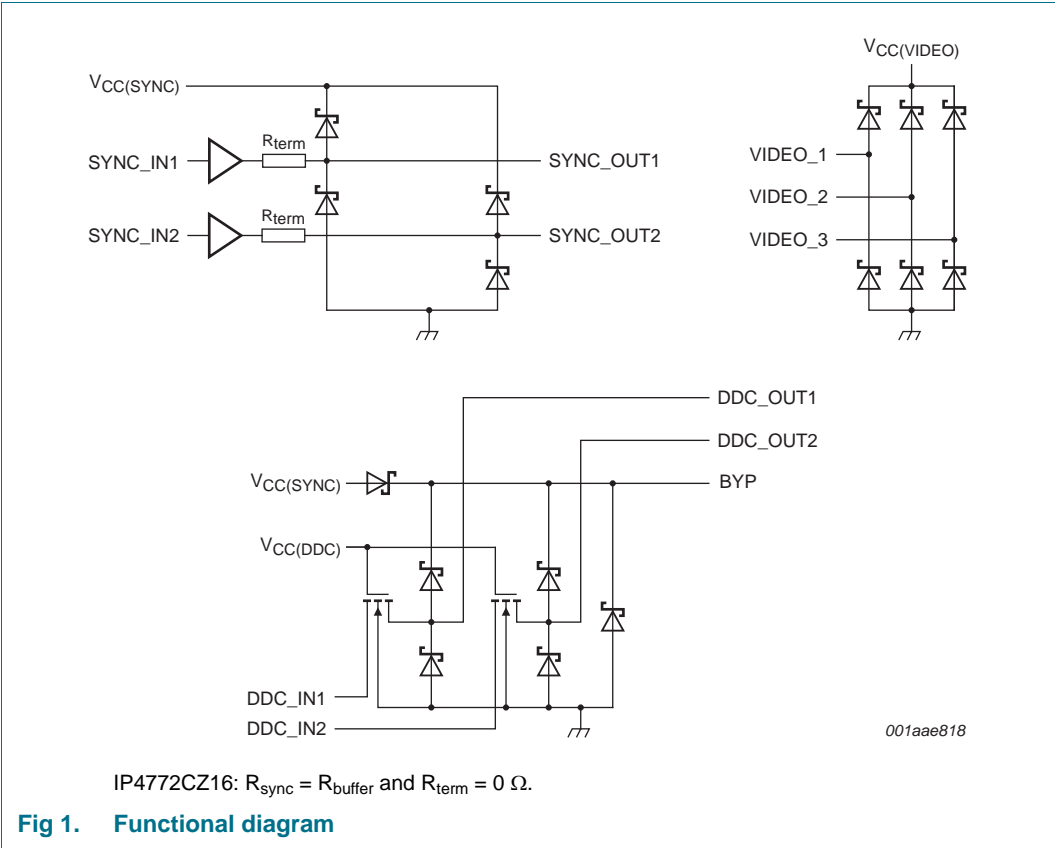


Fig 1. Functional diagram

## 7. Pinning information

### 7.1 Pinning

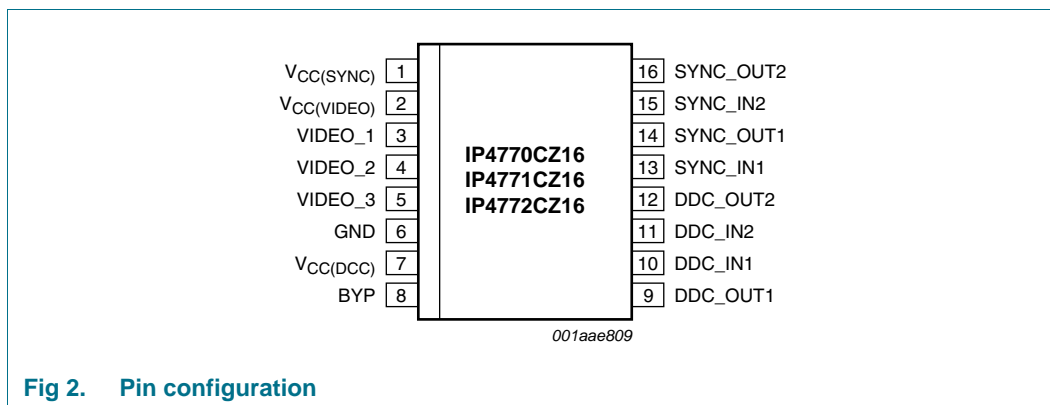


Fig 2. Pin configuration

### 7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V <sub>CC</sub> (SYNC)	1	supply voltage for SYNC_1 and SYNC_2 level shifter and their connected ESD protections
V <sub>CC</sub> (VIDEO)	2	supply voltage for VIDEO_1, VIDEO_2 and VIDEO_3 protection circuits
VIDEO_1	3	video signal ESD protection channel 1
VIDEO_2	4	video signal ESD protection channel 2
VIDEO_3	5	video signal ESD protection channel 3
GND	6	ground
V <sub>CC</sub> (DDC)	7	supply voltage for DDC_1 and DDC_2 level shifter N-FET gates
BYP	8	this input is used to connect an external 0.2 $\mu$ F bypass capacitor to increase ESD withstand voltage rating for the DDC outputs ( $\pm 8$ kV with capacitor or $\pm 4$ kV without capacitor)
DDC_OUT1	9	DDC signal output 1; connected to the video connector side of one of the SYNC lines
DDC_IN1	10	DDC signal input 1; connected to the VGA controller side of one of the SYNC lines
DDC_IN2	11	DDC signal input 2; connected to the VGA controller side of one of the SYNC lines
DDC_OUT2	12	DDC signal output 2; connected to the video connector side of one of the SYNC lines
SYNC_IN1	13	SYNC signal input 1; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT1	14	SYNC signal output 1; connected to the video connector side of one of the SYNC lines
SYNC_IN2	15	SYNC signal input 2; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT2	16	SYNC signal output 2; connected to the video connector side of one of the SYNC lines

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground (GND).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2; pins VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1, DDC_OUT2			
		level 4; contact	−8	+8	kV
		level 4; air discharge	−15	+15	kV
		IEC 61000-4-2; all other pins			
		level 1; contact	−2	+2	kV
		level 1; air discharge	−2	+2	kV
V <sub>CC(VIDEO)</sub>	video supply voltage		−0.5	5.5	V
V <sub>CC(DDC)</sub>	data display channel supply voltage		−0.5	5.5	V
V <sub>CC(SYNC)</sub>	synchronization supply voltage		−0.5	5.5	V
V <sub>I(VIDEO_1)</sub>	input voltage on pin VIDEO_1		−0.5	V <sub>CC(VIDEO)</sub>	V
V <sub>I(VIDEO_2)</sub>	input voltage on pin VIDEO_2		−0.5	V <sub>CC(VIDEO)</sub>	V
V <sub>I(VIDEO_3)</sub>	input voltage on pin VIDEO_3		−0.5	V <sub>CC(VIDEO)</sub>	V
V <sub>I(DDC_IN1)</sub>	input voltage on pin DDC_IN1		−0.5	V <sub>CC(DDC)</sub>	V
V <sub>I(DDC_IN2)</sub>	input voltage on pin DDC_IN2		−0.5	V <sub>CC(DDC)</sub>	V
V <sub>I(SYNC_IN1)</sub>	input voltage on pin SYNC_IN1		−0.5	V <sub>CC(SYNC)</sub>	V
V <sub>I(SYNC_IN2)</sub>	input voltage on pin SYNC_IN2		−0.5	V <sub>CC(SYNC)</sub>	V
V <sub>O(DDC_OUT1)</sub>	output voltage on pin DDC_OUT1		−0.5	V <sub>CC(DDC)</sub>	V
V <sub>O(DDC_OUT2)</sub>	output voltage on pin DDC_OUT2		−0.5	V <sub>CC(DDC)</sub>	V
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	-	500	mW
T <sub>stg</sub>	storage temperature		−55	+125	°C

- [1] Pins BYP, V<sub>CC(VIDEO)</sub> and V<sub>CC(SYNC)</sub> must be bypassed to ground (pin GND) via a low-impedance ground plane with 0.22 µF, low inductance, chip ceramic capacitor at each supply pin.  
ESD pulse is applied between the pins VIDEO\_1, VIDEO\_2, VIDEO\_3, SYNC\_OUT1, SYNC\_OUT2, DDC\_OUT1, DDC\_OUT2 and GND.  
The bypass capacitor at pin BYP can be omitted. In this case the maximum ESD level for DDC\_OUT1 and DDC\_OUT2 pins is reduced to ±4 kV.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{oper}$	operating temperature		-40	-	+85	°C

## 10. Characteristics

**Table 6. Sync circuit characteristics**

$V_{CC(SYNC)} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply: pin $V_{CC(SYNC)}$						
$I_{CC(SYNC)}$	supply current on pin $V_{CC(SYNC)}$		[1]	-	-	50 $\mu$ A
		SYNC input at 3 V	[1]	-	-	2 mA
Input: pins SYNC_IN1 and SYNC_IN2						
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.6	V
Output: pins SYNC_OUT1 and SYNC_OUT2						
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 1$ mA	4.85	-	-	V
		IP4772CZ16; $I_{OH} = 24$ mA	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 1$ mA	-	-	0.15	V
		IP4772CZ16; $I_{OL} = 24$ mA	-	-	0.8	V
$R_{sync}$	synchronization resistance	IP4770CZ16	[2]	-	55	$\Omega$
		IP4771CZ16	[2]	-	65	$\Omega$
		IP4772CZ16	[3]	-	10	$\Omega$
Sync channel						
$t_{PLH}$	LOW to HIGH propagation delay	$C_L = 50$ pF; $t_r$ and $t_f \leq 5$ ns	[4]	-	-	12 ns
$t_{PHL}$	HIGH to LOW propagation delay	$C_L = 50$ pF; $t_r$ and $t_f \leq 5$ ns	[4]	-	-	12 ns
$t_{r(o)}$	output rise time	$C_L = 50$ pF; $t_r$ and $t_f \leq 5$ ns	-	4	-	ns
		$C_L = 7$ pF; $t_r$ and $t_f \leq 5$ ns	-	1.5	-	ns
$t_{f(o)}$	output fall time	$C_L = 50$ pF; $t_r$ and $t_f \leq 5$ ns	-	4	-	ns
		$C_L = 7$ pF; $t_r$ and $t_f \leq 5$ ns	-	1.5	-	ns
Protection diode						
$I_{L(r)}$	reverse leakage current	per channel; $V = 3.0$ V	-	-	1	$\mu$ A
$V_{BRzd}$	Zener diode breakdown voltage	$I = 1$ mA	6	-	9	V
$V_{Fd}$	diode forward voltage	$I_F = 1$ mA	-	0.7	-	V

[1] SYNC outputs unloaded.

[2]  $R_{sync} = R_{term} + R_{buffer}$ .

[3]  $R_{sync} = R_{buffer}$  because  $R_{term} = 0\text{ }\Omega$ .

[4] This parameter is guaranteed by design and characterization.

**Table 7. Video circuit characteristics** $V_{CC(VIDEO)} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply: pin <math>V_{CC(VIDEO)}</math></b>						
$I_{CC(VIDEO)}$	supply current on pin $V_{CC(VIDEO)}$	static input signals	-	-	10	$\mu\text{A}$
<b>Video channel: pins VIDEO_1, VIDEO_2 and VIDEO_3</b>						
$C_{ch(video)}$	video channel capacitance	$f_i = 1\text{ MHz}$ ; $V_i = 2.5\text{ V}$	[1]	-	4	pF
$I_{i(video)}$	video input current	$V_i = V_{CC(VIDEO)}$ or GND	-1	-	+1	$\mu\text{A}$
<b>Protection diode</b>						
$V_{Fd}$	diode forward voltage	$I_F = 1\text{ mA}$	-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

**Table 8. Level circuit characteristics** $V_{CC(DDC)} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply: pin <math>V_{CC(DDC)}</math></b>						
$I_{CC(DDC)}$	data display channel supply current		-	-	10	$\mu\text{A}$
<b>N-MOSFET</b>						
$I_{L(off)}$	off-state leakage current		[1]	-	10	$\mu\text{A}$
$\Delta V_{on}$	on-state voltage drop	$V_{CC(DDC)} = 2.5\text{ V}$ ; $V_S = \text{GND}$ ; $I_{DS} = 3\text{ mA}$	-	-	0.18	V
<b>Protection diode</b>						
$I_{L(r)}$	reverse leakage current	per channel; $V = 3.0\text{ V}$	-	-	1	$\mu\text{A}$
$V_{BRzd}$	Zener diode breakdown voltage	$I = 1\text{ mA}$	6	-	9	V
$V_{Fd}$	diode forward voltage	$I_F = 1\text{ mA}$	-	0.7	-	V

[1] Input  $V_{I(DDC\_INx)} \leq V_{CC(DDC)} - 0.4\text{ V}$  and output  $V_{O(DDC\_OUTx)} = V_{CC(DDC)}$  or  
input  $V_{I(DDC\_INx)} = V_{CC(DDC)}$  and output  $V_{O(DDC\_OUTx)} \leq V_{CC(DDC)} - 0.4\text{ V}$ .

## 11. Application information

The IP4770CZ16, IP4771CZ16, IP4772CZ16 should be placed as close as possible to the VGA/DVI interface connector.

The ESD protection channels VIDEO\_1, VIDEO\_2 and VIDEO\_3 can be connected in any order with RGB signals.

The 100 k $\Omega$  resistors between the DDC\_OUTx channels and VCC\_5V are optional. They may be used, if required, to pull-up the DDC\_OUTx lines to VCC\_5V when no monitor is connected to the VGA connector. Backflow current can flow between pins DDC\_OUTx and VCC\_5V via these resistors when VCC\_5V is powered down.

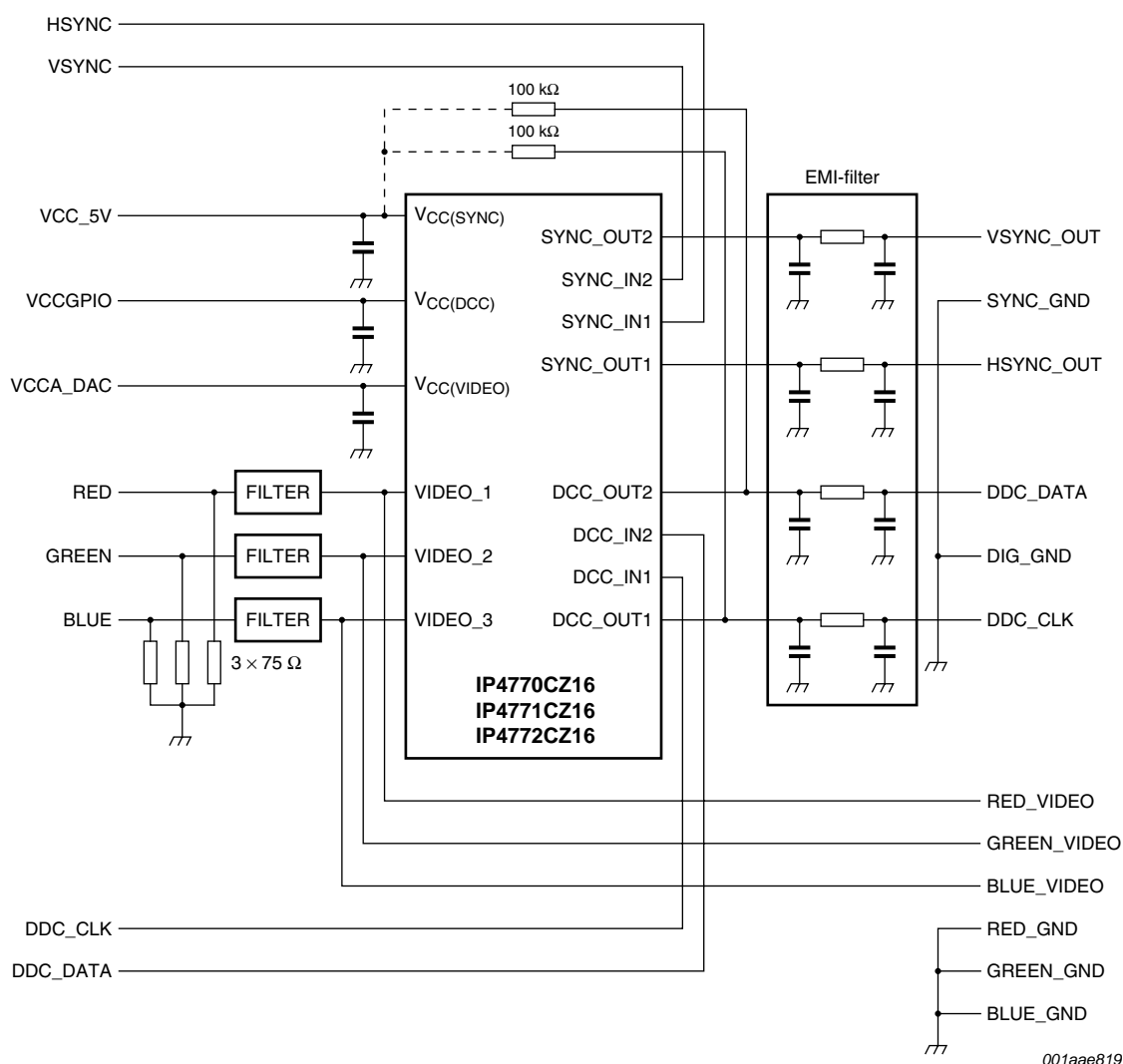


Fig 3. Application diagram



12. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

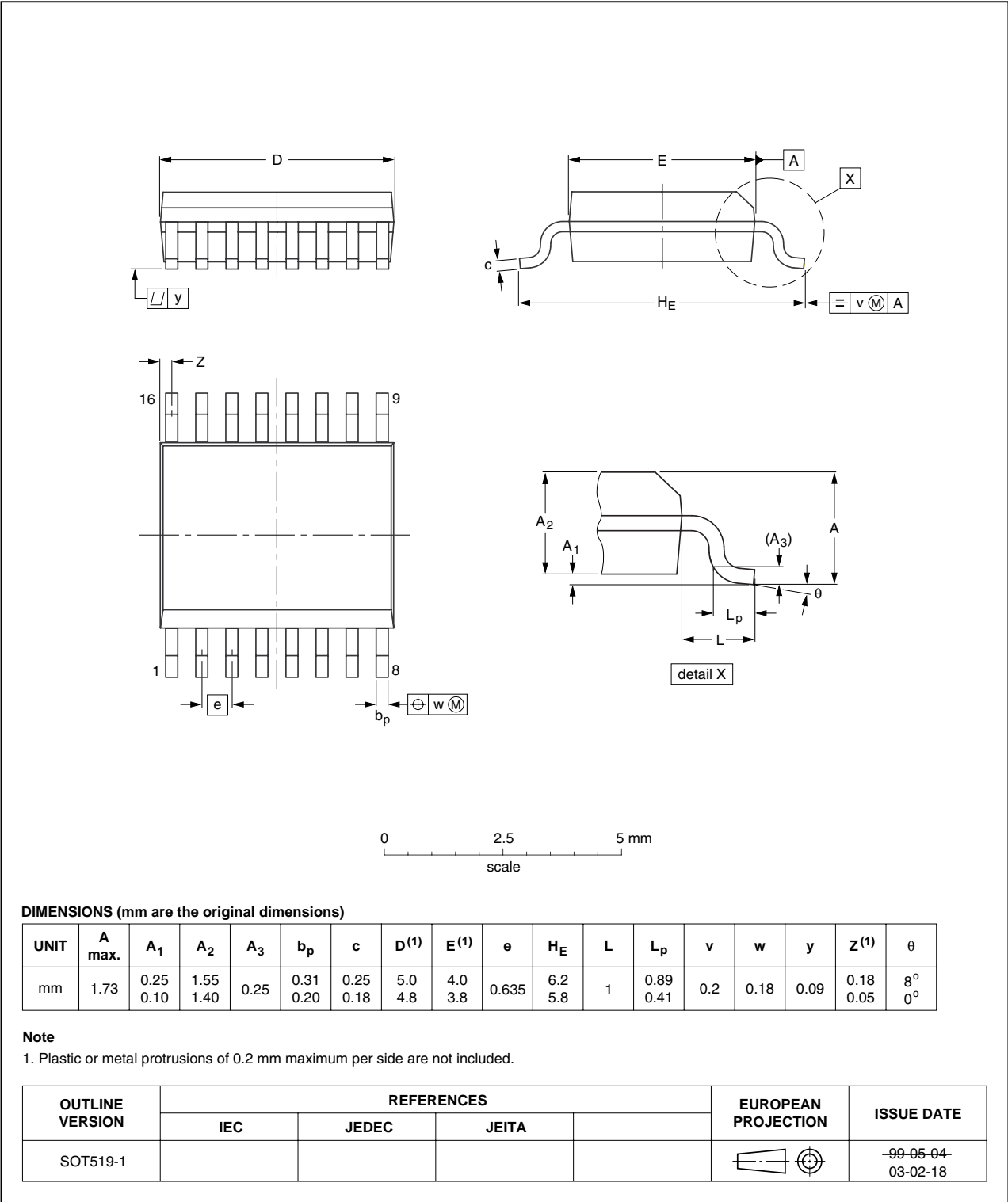


Fig 4. Package outline SOT519-1 (SSOP16)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DDC	Data Display Channel
DVI	Digital Video Interface
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HSYNC	Horizontal SYNChronization
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PC	Personal Computer
RFI	Radio Frequency Interference
RGB	Red Green Blue
RoHS	Restriction of Hazardous Substances
SYNC	SYNChronization
TTL	Transistor-Transistor Logic
VGA	Video Graphics Adapter
VSYNC	Vertical SYNChronization

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4770_71_72CZ16 v.2	20110519	Product data sheet	-	IP4770CZ16_4771_4772 v.1
Modifications:	<ul style="list-style-type: none"><li>• <a href="#">Section 5 “Marking”</a>: added.</li><li>• <a href="#">Figure 1</a>: corrected.</li><li>• <a href="#">Table 9</a>: updated.</li><li>• <a href="#">Section 15 “Legal information”</a>: updated.</li></ul>			
IP4770CZ16_4771_4772 v.1	20061025	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Marking</b> .....	<b>2</b>
<b>6</b>	<b>Functional diagram</b> .....	<b>3</b>
<b>7</b>	<b>Pinning information</b> .....	<b>4</b>
7.1	Pinning .....	4
7.2	Pin description .....	4
<b>8</b>	<b>Limiting values</b> .....	<b>5</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>10</b>	<b>Characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Application information</b> .....	<b>8</b>
<b>12</b>	<b>Package outline</b> .....	<b>9</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>10</b>
<b>14</b>	<b>Revision history</b> .....	<b>11</b>
<b>15</b>	<b>Legal information</b> .....	<b>12</b>
15.1	Data sheet status .....	12
15.2	Definitions .....	12
15.3	Disclaimers .....	12
15.4	Trademarks .....	13
<b>16</b>	<b>Contact information</b> .....	<b>13</b>
<b>17</b>	<b>Contents</b> .....	<b>14</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 19 May 2011

Document identifier: IP4770\_71\_72CZ16

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[IP4772CZ16,118](#)