

# 74HC4052; 74HCT4052

Dual 4-channel analog multiplexer/demultiplexer

Rev. 10 — 19 July 2012

Product data sheet

## 1. General description

The 74HC4052; 74HCT4052 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4052B. The device is specified in compliance with JEDEC standard no. 7A.

The 74HC4052; 74HCT4052 is a dual 4-channel analog multiplexer/demultiplexer with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin  $\bar{E}$ ). When pin  $\bar{E}$  = LOW, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin  $\bar{E}$  = HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs (pins S0, S1 and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are 2.0 V to 10.0 V for the 74HC4052 and 4.5 V to 5.5 V for the 74HCT4052. The analog inputs/outputs (pins nY0 to nY3 and nZ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

## 2. Features and benefits

- Wide analog input voltage range from -5 V to +5 V
- Low ON resistance:
  - ◆ 80  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 4.5$  V
  - ◆ 70  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 6.0$  V
  - ◆ 60  $\Omega$  (typical) at  $V_{CC} - V_{EE} = 9.0$  V
- Logic level translation: to enable 5 V logic to communicate with  $\pm 5$  V analog signals
- Typical 'break before make' built-in
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



### 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

### 4. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
<b>74HC4052</b>					
74HC4052N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	
74HC4052D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	
74HC4052DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1	
74HC4052PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1	
74HC4052BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1	
<b>74HCT4052</b>					
74HCT4052N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	
74HCT4052D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	
74HCT4052DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1	
74HCT4052PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1	
74HCT4052BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1	

## 5. Functional diagram

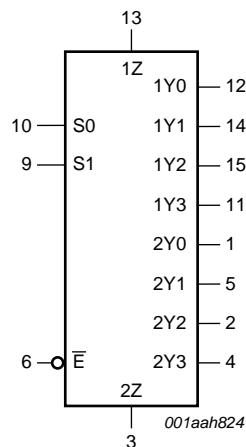


Fig 1. Logic symbol

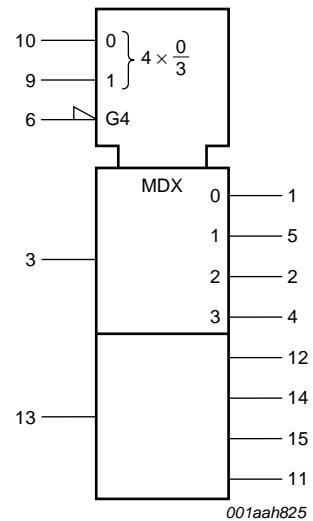


Fig 2. IEC logic symbol

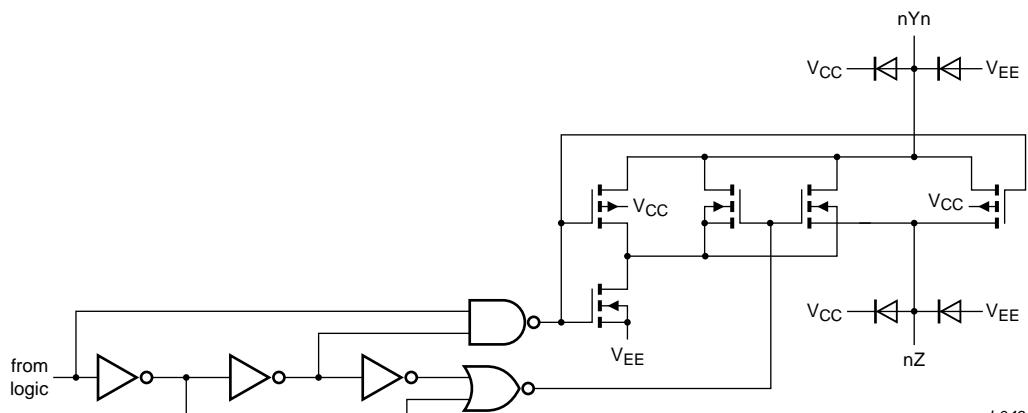


Fig 3. Schematic diagram (one switch)

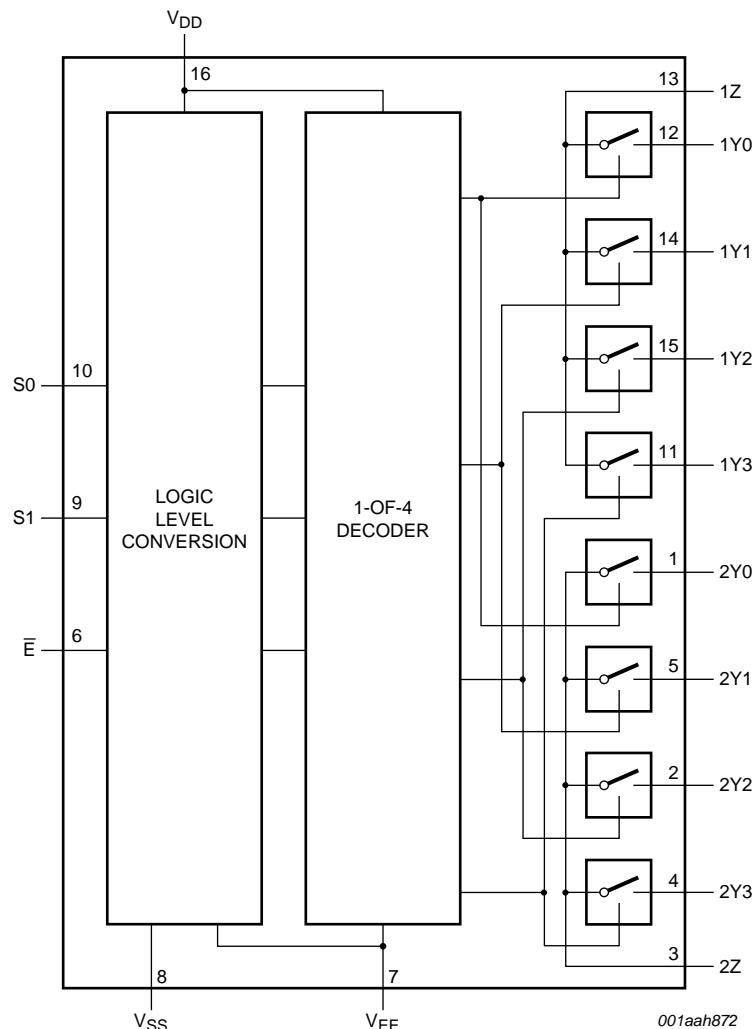


Fig 4. Functional diagram

## 6. Pinning information

### 6.1 Pinning

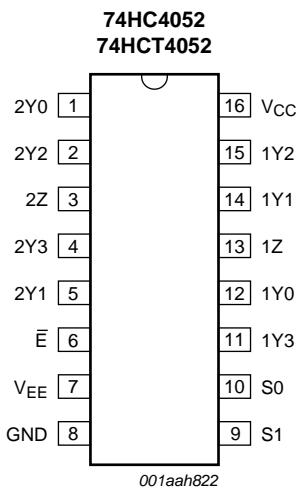


Fig 5. Pin configuration for DIP16, SO16 and (T)SSOP16

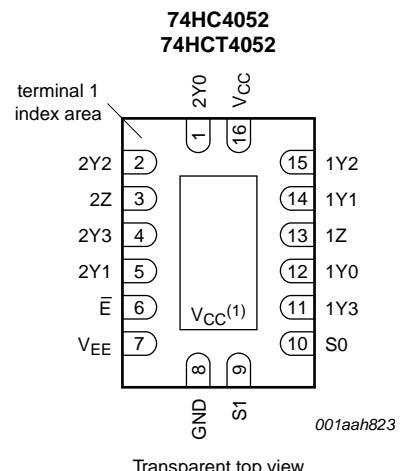


Fig 6. Pin configuration for DHVQFN16

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input or output 2Y0
2Y2	2	independent input or output 2Y2
2Z	3	common input or output 2
2Y3	4	independent input or output 2Y3
2Y1	5	independent input or output 2Y1
E	6	enable input (active LOW)
V <sub>EE</sub>	7	negative supply voltage
GND	8	ground (0 V)
S1	9	select logic input 1
S0	10	select logic input 0
1Y3	11	independent input or output 1Y3
1Y0	12	independent input or output 1Y0
1Z	13	common input or output 1
1Y1	14	independent input or output 1Y1
1Y2	15	independent input or output 1Y2
V <sub>CC</sub>	16	positive supply voltage

## 7. Functional description

### 7.1 Function table

Table 3. Function table<sup>[1]</sup>

Input			Channel on
<b>E</b>	<b>S1</b>	<b>S0</b>	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to  $V_{EE} = GND$  (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		[1] -0.5	+11.0	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5 \text{ V}$ or $V_{SW} > V_{CC} + 0.5 \text{ V}$	-	$\pm 20$	mA
$I_{SW}$	switch current	$-0.5 \text{ V} < V_{SW} < V_{CC} + 0.5 \text{ V}$	-	$\pm 25$	mA
$I_{EE}$	supply current		-	$\pm 20$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	DIP16 package	[2] -	750	mW
		SO16, (T)SSOP16, and DHVQFN16 package	[3] -	500	mW
P	power dissipation	per switch	-	100	mW

[1] To avoid drawing  $V_{CC}$  current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no  $V_{CC}$  current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

[2] For DIP16 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 12 mW/K.

[3] For SO16 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

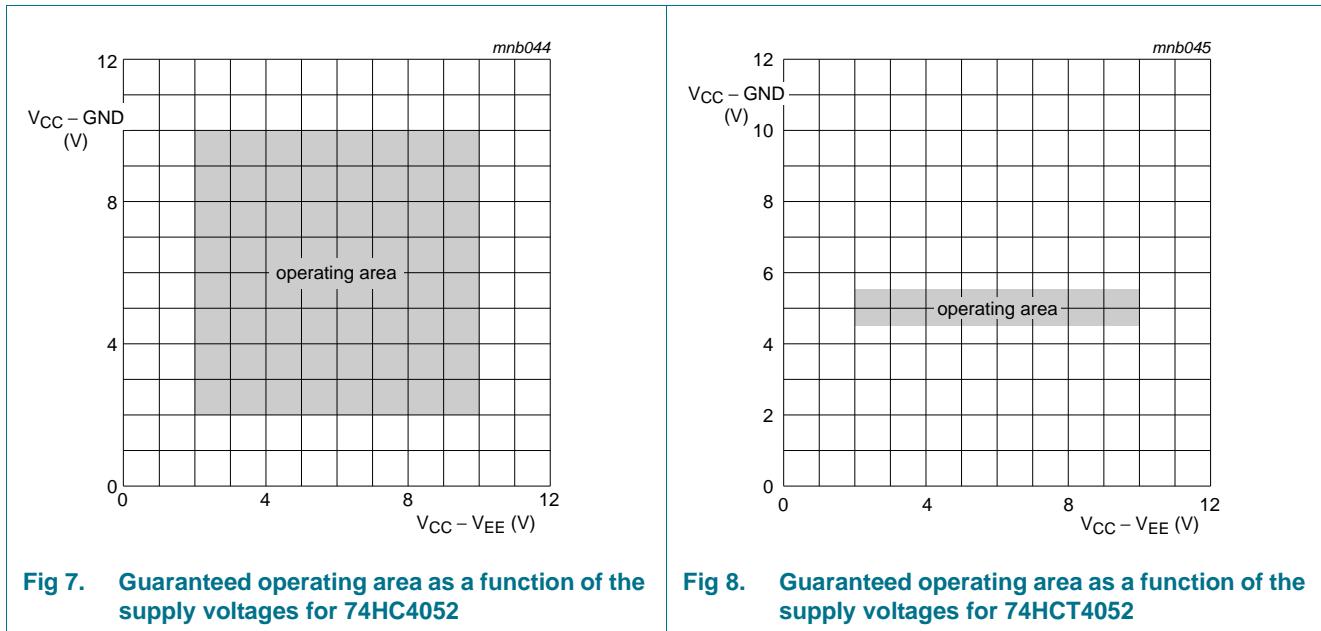
For SSOP16 and TSSOP16 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 4.5 mW/K.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	74HC4052			74HCT4052			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage	see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>							
		$V_{CC} - GND$	2.0	5.0	10.0	4.5	5.0	5.5	V
		$V_{CC} - V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V
$V_I$	input voltage		GND	-	$V_{CC}$	GND	-	$V_{CC}$	V
$V_{SW}$	switch voltage		$V_{EE}$	-	$V_{CC}$	$V_{EE}$	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V
		$V_{CC} = 10.0$ V	-	-	31	-	-	-	ns/V



## 10. Static characteristics

**Table 6.  $R_{ON}$  resistance per switch for 74HC4052 and 74HCT4052**

$V_I = V_{IH}$  or  $V_{IL}$ ; for test circuit see [Figure 9](#).

$V_{IS}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input.

$V_{OS}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.

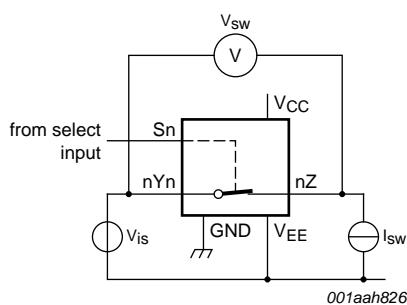
For 74HC4052:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0$  V, 4.5 V, 6.0 V and 9.0 V.

For 74HCT4052:  $V_{CC} - GND = 4.5$  V and 5.5 V,  $V_{CC} - V_{EE} = 2.0$  V, 4.5 V, 6.0 V and 9.0 V.

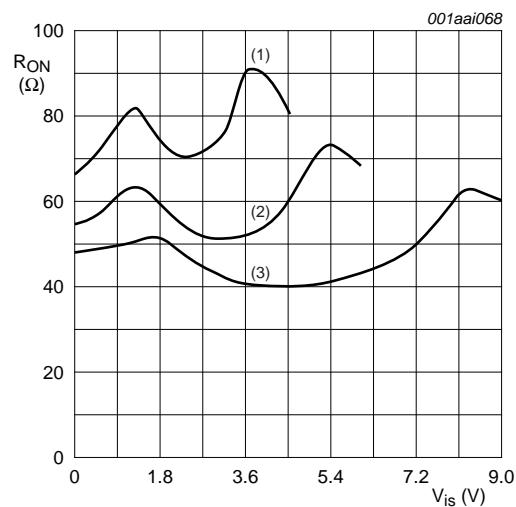
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40</math> °C to +85 °C</b> <a href="#">[1]</a>						
$R_{ON(peak)}$	ON resistance (peak)	$V_{IS} = V_{CC}$ to $V_{EE}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	100	225	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	90	200	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	70	165	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_{IS} = V_{EE}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	150	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	80	175	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	70	150	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	60	130	$\Omega$
		$V_{IS} = V_{CC}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	150	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	90	200	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	80	175	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	65	150	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_{IS} = V_{CC}$ to $V_{EE}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V	[2]	-	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	9	-	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V	-	8	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	6	-	$\Omega$
<b><math>T_{amb} = -40</math> °C to +125 °C</b>						
$R_{ON(peak)}$	ON resistance (peak)	$V_{IS} = V_{CC}$ to $V_{EE}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	270	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	240	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	-	195	$\Omega$

**Table 6.  $R_{ON}$  resistance per switch for 74HC4052 and 74HCT4052 ...continued** $V_I = V_{IH}$  or  $V_{IL}$ ; for test circuit see [Figure 9](#). $V_{is}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input. $V_{os}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.For 74HC4052:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0$  V, 4.5 V, 6.0 V and 9.0 V.For 74HCT4052:  $V_{CC} - GND = 4.5$  V and 5.5 V,  $V_{CC} - V_{EE} = 2.0$  V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	210	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	180	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	-	160	$\Omega$
		$V_{is} = V_{CC}$				
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V; $I_{SW} = 100$ $\mu$ A	[2]	-	-	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	240	$\Omega$
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V; $I_{SW} = 1000$ $\mu$ A	-	-	210	$\Omega$
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V; $I_{SW} = 1000$ $\mu$ A	-	-	180	$\Omega$

[1] All typical values are measured at  $T_{amb} = 25$  °C.[2] When supply voltages ( $V_{CC} - V_{EE}$ ) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals. $V_{is} = 0$  V to  $(V_{CC} - V_{EE})$ .

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

**Fig 9. Test circuit for measuring  $R_{ON}$**  $V_{is} = 0$  V to  $(V_{CC} - V_{EE})$ .(1)  $V_{CC} = 4.5$  V(2)  $V_{CC} = 6$  V(3)  $V_{CC} = 9$  V**Fig 10. Typical  $R_{ON}$  as a function of input voltage  $V_{is}$**

**Table 7. Static characteristics for 74HC4052**

Voltages are referenced to GND (ground = 0 V).

 $V_{IS}$  is the input voltage at pins  $nYn$  or  $nZ$ , whichever is assigned as an input. $V_{OS}$  is the output voltage at pins  $nZ$  or  $nYn$ , whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40^{\circ}\text{C}</math> to <math>+85^{\circ}\text{C}</math><sup>[1]</sup></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	4.7	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
		$V_{CC} = 9.0\text{ V}$	-	4.3	2.7	V
$I_I$	input leakage current	$V_{EE} = 0\text{ V}$ ; $V_I = V_{CC}$ or GND				
		$V_{CC} = 6.0\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}$ ; $V_{EE} = 0\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - V_{EE}$ ; see <a href="#">Figure 11</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - V_{EE}$ ; $V_{CC} = 10.0\text{ V}$ ; $V_{EE} = 0\text{ V}$ ; see <a href="#">Figure 12</a>	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{EE} = 0\text{ V}$ ; $V_I = V_{CC}$ or GND; $V_{IS} = V_{EE}$ or $V_{CC}$ ; $V_{OS} = V_{CC}$ or $V_{EE}$				
		$V_{CC} = 6.0\text{ V}$	-	-	80.0	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	160.0	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
$C_{sw}$	switch capacitance	independent pins $nYn$	-	5	-	pF
		common pins $nZ$	-	12	-	pF
<b><math>T_{amb} = -40^{\circ}\text{C}</math> to <math>+125^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
		$V_{CC} = 9.0\text{ V}$	-	-	2.7	V
$I_I$	input leakage current	$V_{EE} = 0\text{ V}$ ; $V_I = V_{CC}$ or GND				
		$V_{CC} = 6.0\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	$\pm 2.0$	$\mu\text{A}$

**Table 7. Static characteristics for 74HC4052 ...continued***Voltages are referenced to GND (ground = 0 V).* *$V_{is}$  is the input voltage at pins  $nY_n$  or  $nZ$ , whichever is assigned as an input.* *$V_{os}$  is the output voltage at pins  $nZ$  or  $nY_n$ , whichever is assigned as an output.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0 \text{ V}$ ; $V_{EE} = 0 \text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{sw}  = V_{CC} - V_{EE}$ ; see <a href="#">Figure 11</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_{sw}  = V_{CC} - V_{EE}$ ; $V_{CC} = 10.0 \text{ V}$ ; $V_{EE} = 0 \text{ V}$ ; see <a href="#">Figure 12</a>	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{EE} = 0 \text{ V}$ ; $V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $V_{EE}$				
		$V_{CC} = 6.0 \text{ V}$	-	-	160.0	$\mu\text{A}$
		$V_{CC} = 10.0 \text{ V}$	-	-	320.0	$\mu\text{A}$

[1] All typical values are measured at  $T_{amb} = 25 \text{ }^\circ\text{C}$ .**Table 8. Static characteristics for 74HCT4052***Voltages are referenced to GND (ground = 0 V).* *$V_{is}$  is the input voltage at pins  $nY_n$  or  $nZ$ , whichever is assigned as an input.* *$V_{os}$  is the output voltage at pins  $nZ$  or  $nY_n$ , whichever is assigned as an output.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}</math></b> <sup>[1]</sup>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0 \text{ V}$ ; $V_{EE} = 0 \text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{sw}  = V_{CC} - V_{EE}$ ; see <a href="#">Figure 11</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0 \text{ V}$ ; $V_{EE} = 0 \text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{sw}  = V_{CC} - V_{EE}$ ; see <a href="#">Figure 12</a>	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $V_{EE}$				
		$V_{CC} = 5.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	-	80.0	$\mu\text{A}$
		$V_{CC} = 5.0 \text{ V}$ ; $V_{EE} = -5.0 \text{ V}$	-	-	160.0	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	45	202.5	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
$C_{sw}$	switch capacitance	independent pins $nY_n$	-	5	-	pF
		common pins $nZ$	-	12	-	pF
<b><math>T_{amb} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	V

**Table 8. Static characteristics for 74HCT4052 ...continued**

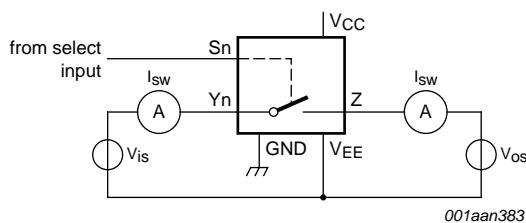
Voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at pins  $nY_n$  or  $nZ$ , whichever is assigned as an input.

$V_{os}$  is the output voltage at pins  $nZ$  or  $nY_n$ , whichever is assigned as an output.

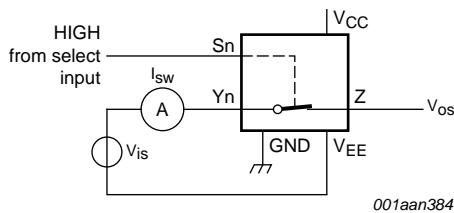
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	V
$I_I$	input leakage current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL};  V_{sw}  = V_{CC} - V_{EE}; \text{ see Figure 11}$				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL};  V_{sw}  = V_{CC} - V_{EE}; \text{ see Figure 12}$	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC} \text{ or GND}; V_{is} = V_{EE} \text{ or } V_{CC}; V_{os} = V_{CC} \text{ or } V_{EE}$				
		$V_{CC} = 5.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	160.0	$\mu\text{A}$
		$V_{CC} = 5.0 \text{ V}; V_{EE} = -5.0 \text{ V}$	-	-	320.0	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	220.5	$\mu\text{A}$

[1] All typical values are measured at  $T_{amb} = 25 \text{ }^\circ\text{C}$ .



$V_{is} = V_{CC}$  and  $V_{os} = V_{EE}$ .

$V_{is} = V_{EE}$  and  $V_{os} = V_{CC}$ .

**Fig 11. Test circuit for measuring OFF-state current**

$V_{is} = V_{CC}$  and  $V_{os} = \text{open-circuit}$ .

$V_{is} = V_{EE}$  and  $V_{os} = \text{open-circuit}$ .

**Fig 12. Test circuit for measuring ON-state current**

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics for 74HC4052**

$GND = 0 \text{ V}$ ;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; for test circuit see [Figure 15](#).

$V_{IS}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input.

$V_{OS}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b><math>T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}</math><sup>[1]</sup></b>							
$t_{pd}$	propagation delay	$V_{IS}$ to $V_{OS}$ ; $R_L = \infty \Omega$ ; see <a href="#">Figure 13</a>	[2]				
		$V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	14	75	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	5	15	ns	
		$V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	4	13	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$	-	4	10	ns	
$t_{on}$	turn-on time	$\bar{E}$ , $S_n$ to $V_{OS}$ ; $R_L = \infty \Omega$ ; see <a href="#">Figure 14</a>	[3]				
		$V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	105	405	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	38	81	ns	
		$V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$	-	28	-	ns	
		$V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	30	69	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$	-	26	58	ns	
$t_{off}$	turn-off time	$\bar{E}$ , $S_n$ to $V_{OS}$ ; $R_L = 1 \text{ k}\Omega$ ; see <a href="#">Figure 14</a>	[4]				
		$V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	74	315	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	27	63	ns	
		$V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$	-	21	-	ns	
		$V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	22	54	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$	-	22	48	ns	
$C_{PD}$	power dissipation capacitance	per switch; $V_I = GND$ to $V_{CC}$	[5]	-	57	-	pF
<b><math>T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}</math></b>							
$t_{pd}$	propagation delay	$V_{IS}$ to $V_{OS}$ ; $R_L = \infty \Omega$ ; see <a href="#">Figure 13</a>	[2]				
		$V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	90	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	18	ns	
		$V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	15	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$	-	-	12	ns	
$t_{on}$	turn-on time	$\bar{E}$ , $S_n$ to $V_{OS}$ ; $R_L = \infty \Omega$ ; see <a href="#">Figure 14</a>	[3]				
		$V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	490	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	98	ns	
		$V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$	-	-	83	ns	
		$V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$	-	-	69	ns	

**Table 9. Dynamic characteristics for 74HC4052 ...continued***GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; for test circuit see [Figure 15](#).* *$V_{is}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input.* *$V_{os}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{off}$	turn-off time	$\bar{E}$ , $S_n$ to $V_{os}$ ; $R_L = 1$ k $\Omega$ ; see <a href="#">Figure 14</a>	[4]			
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V	-	-	375	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	-	75	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V	-	-	64	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	-	57	ns

[1] All typical values are measured at  $T_{amb} = 25$  °C.[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .[3]  $t_{on}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .[4]  $t_{off}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum \{ (C_L + C_{sw}) \times V_{CC}^2 \times f_o \}$  where: $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz;

N = number of inputs switching;

 $\sum \{ (C_L + C_{sw}) \times V_{CC}^2 \times f_o \}$  = sum of outputs; $C_L$  = output load capacitance in pF; $C_{sw}$  = switch capacitance in pF; $V_{CC}$  = supply voltage in V.**Table 10. Dynamic characteristics for 74HCT4052***GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; for test circuit see [Figure 15](#).* *$V_{is}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input.* *$V_{os}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40</math> °C to +85 °C</b> [1]						
$t_{pd}$	propagation delay	$V_{is}$ to $V_{os}$ ; $R_L = \infty$ $\Omega$ ; see <a href="#">Figure 13</a>	[2]			
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	5	15	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	4	10	ns
$t_{on}$	turn-on time	$\bar{E}$ , $S_n$ to $V_{os}$ ; $R_L = 1$ k $\Omega$ ; see <a href="#">Figure 14</a>	[3]			
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	41	88	ns
		$V_{CC} = 5.0$ V; $V_{EE} = 0$ V; $C_L = 15$ pF	-	18	-	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	28	60	ns
$t_{off}$	turn-off time	$\bar{E}$ , $S_n$ to $V_{os}$ ; $R_L = 1$ k $\Omega$ ; see <a href="#">Figure 14</a>	[4]			
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	26	63	ns
		$V_{CC} = 5.0$ V; $V_{EE} = 0$ V; $C_L = 15$ pF	-	13	-	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	21	48	ns
$C_{PD}$	power dissipation capacitance	per switch; $V_I = \text{GND to } V_{CC} - 1.5$ V	[5]	-	57	-
						pF

**Table 10. Dynamic characteristics for 74HCT4052 ...continued**

$GND = 0 \text{ V}$ ;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; for test circuit see [Figure 15](#).

$V_{is}$  is the input voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a  $nYn$  or  $nZ$  terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40 \text{ }^{\circ}\text{C}</math> to <math>+125 \text{ }^{\circ}\text{C}</math></b>						
$t_{pd}$	propagation delay	$V_{is}$ to $V_{os}$ ; $R_L = \infty \Omega$ ; see <a href="#">Figure 13</a>	[2]			
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	-	18	ns
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = -4.5 \text{ V}$	-	-	12	ns
$t_{on}$	turn-on time	$\bar{E}$ , $S_n$ to $V_{os}$ ; $R_L = 1 \text{ k}\Omega$ ; see <a href="#">Figure 14</a>	[3]			
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	-	105	ns
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = -4.5 \text{ V}$	-	-	72	ns
$t_{off}$	turn-off time	$\bar{E}$ , $S_n$ to $V_{os}$ ; $R_L = 1 \text{ k}\Omega$ ; see <a href="#">Figure 14</a>	[4]			
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = 0 \text{ V}$	-	-	75	ns
		$V_{CC} = 4.5 \text{ V}$ ; $V_{EE} = -4.5 \text{ V}$	-	-	57	ns

[1] All typical values are measured at  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $t_{on}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[4]  $t_{off}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

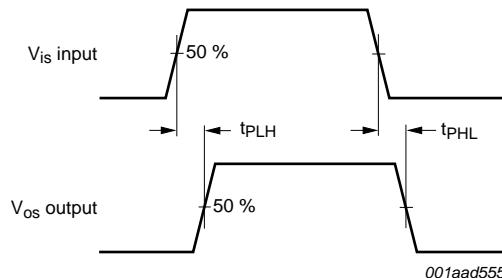
$N$  = number of inputs switching;

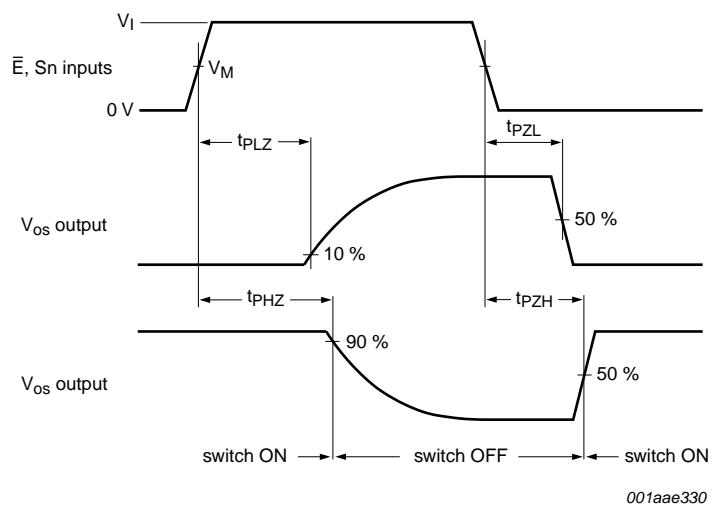
$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$C_{sw}$  = switch capacitance in pF;

$V_{CC}$  = supply voltage in V.

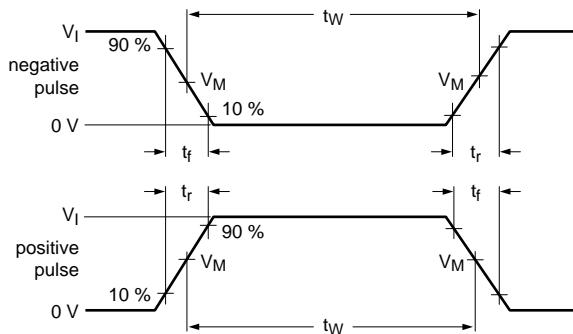
**Fig 13. Input ( $V_{is}$ ) to output ( $V_{os}$ ) propagation delays**



For 74HC4052:  $V_M = 0.5 \times V_{CC}$ .

For 74HCT4052:  $V_M = 1.3$  V.

**Fig 14. Turn-on and turn-off times**



Definitions for test circuit; see [Table 11](#):

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

$R_L$  = load resistance.

$S1$  = Test selection switch.

**Fig 15. Test circuit for measuring AC performance**

Table 11. Test data

Test	Input				Load		S1 position
	$V_I$	$V_{is}$	$t_r, t_f$	at $f_{max}$	other <sup>[1]</sup>	$C_L$	
$t_{PHL}, t_{PLH}$	[2]	pulse	< 2 ns	6 ns	50 pF	1 k $\Omega$	open
$t_{PZH}, t_{PHZ}$	[2]	$V_{CC}$	< 2 ns	6 ns	50 pF	1 k $\Omega$	$V_{EE}$
$t_{PZL}, t_{PLZ}$	[2]	$V_{EE}$	< 2 ns	6 ns	50 pF	1 k $\Omega$	$V_{CC}$

[1]  $t_r = t_f = 6$  ns; when measuring  $f_{max}$ , there is no constraint to  $t_r$  and  $t_f$  with 50 % duty factor.

[2]  $V_I$  values:

- a) For 74HC4052:  $V_I = V_{CC}$
- b) For 74HCT4052:  $V_I = 3$  V

## 12. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values;  $GND = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF.

$V_{is}$  is the input voltage at pins  $nYn$  or  $nZ$ , whichever is assigned as an input.

$V_{os}$  is the output voltage at pins  $nYn$  or  $nZ$ , whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$d_{sin}$	sine-wave distortion	$f_i = 1$ kHz; $R_L = 10$ k $\Omega$ ; see <a href="#">Figure 16</a>					
		$V_{is} = 4.0$ V (p-p); $V_{CC} = 2.25$ V; $V_{EE} = -2.25$ V	-	0.04	-	%	
		$V_{is} = 8.0$ V (p-p); $V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	0.02	-	%	
		$f_i = 10$ kHz; $R_L = 10$ k $\Omega$ ; see <a href="#">Figure 16</a>					
		$V_{is} = 4.0$ V (p-p); $V_{CC} = 2.25$ V; $V_{EE} = -2.25$ V	-	0.12	-	%	
		$V_{is} = 8.0$ V (p-p); $V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	0.06	-	%	
$\alpha_{iso}$	isolation (OFF-state)	$R_L = 600$ $\Omega$ ; $f_i = 1$ MHz; see <a href="#">Figure 17</a>					
		$V_{CC} = 2.25$ V; $V_{EE} = -2.25$ V	[1]	-	-50	-	dB
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	[1]	-	-50	-	dB
Xtalk	crosstalk	between two switches/multiplexers; $R_L = 600$ $\Omega$ ; $f_i = 1$ MHz; see <a href="#">Figure 18</a>					
		$V_{CC} = 2.25$ V; $V_{EE} = -2.25$ V	[1]	-	-60	-	dB
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	[1]	-	-60	-	dB
$V_{ct}$	crosstalk voltage	peak-to-peak value; between control and any switch; $R_L = 600$ $\Omega$ ; $f_i = 1$ MHz; E or Sn square wave between $V_{CC}$ and GND; $t_r = t_f = 6$ ns; see <a href="#">Figure 19</a>					
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	110	-	mV	
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	220	-	mV	
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50$ $\Omega$ ; see <a href="#">Figure 20</a>					
		$V_{CC} = 2.25$ V; $V_{EE} = -2.25$ V	[2]	-	170	-	MHz
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	[2]	-	180	-	MHz

[1] Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).

[2] Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for 1 MHz (0 dBm = 1 mW into 50  $\Omega$ ).

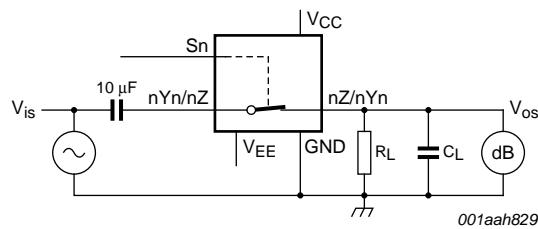
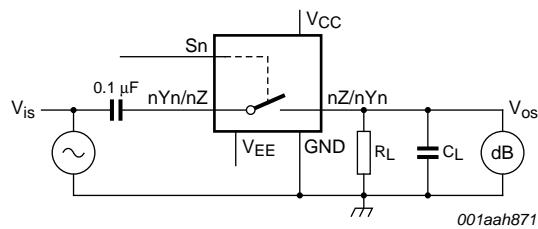
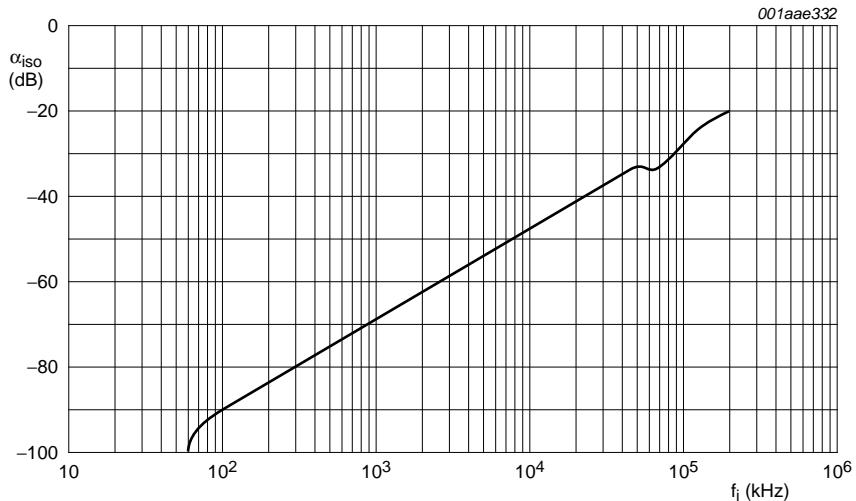


Fig 16. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5$  V; GND = 0 V;  $V_{EE} = -4.5$  V;  $R_L = 600 \Omega$ ;  $R_S = 1 \text{ k}\Omega$ .

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig 17. Test circuit for measuring isolation (OFF-state)

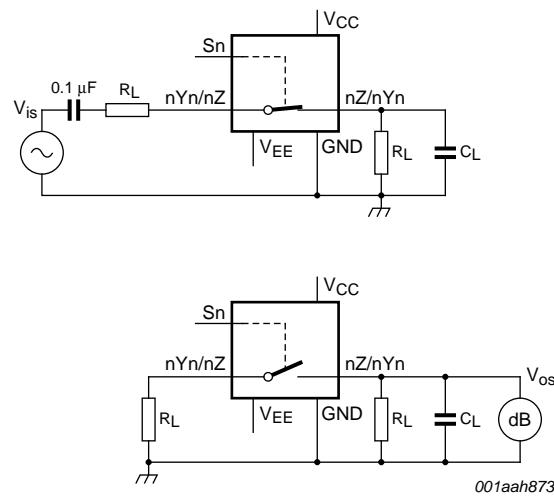


Fig 18. Test circuits for measuring crosstalk between any two switches/multiplexers

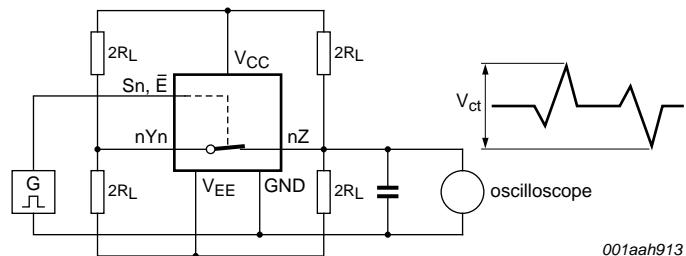
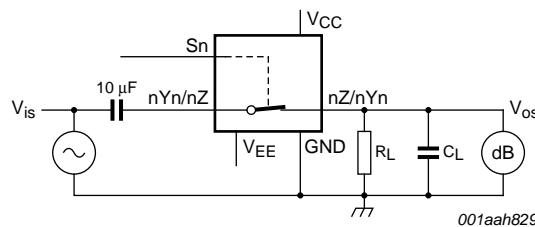
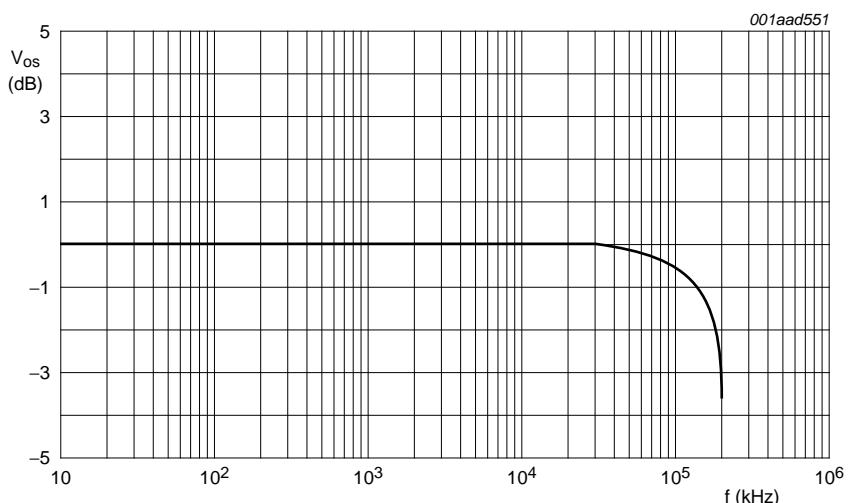


Fig 19. Test circuit for measuring crosstalk between control input and any switch



$V_{CC} = 4.5$  V; GND = 0 V;  $V_{EE} = -4.5$  V;  $R_L = 50 \Omega$ ;  $R_S = 1 \text{ k}\Omega$ .

a. Test circuit



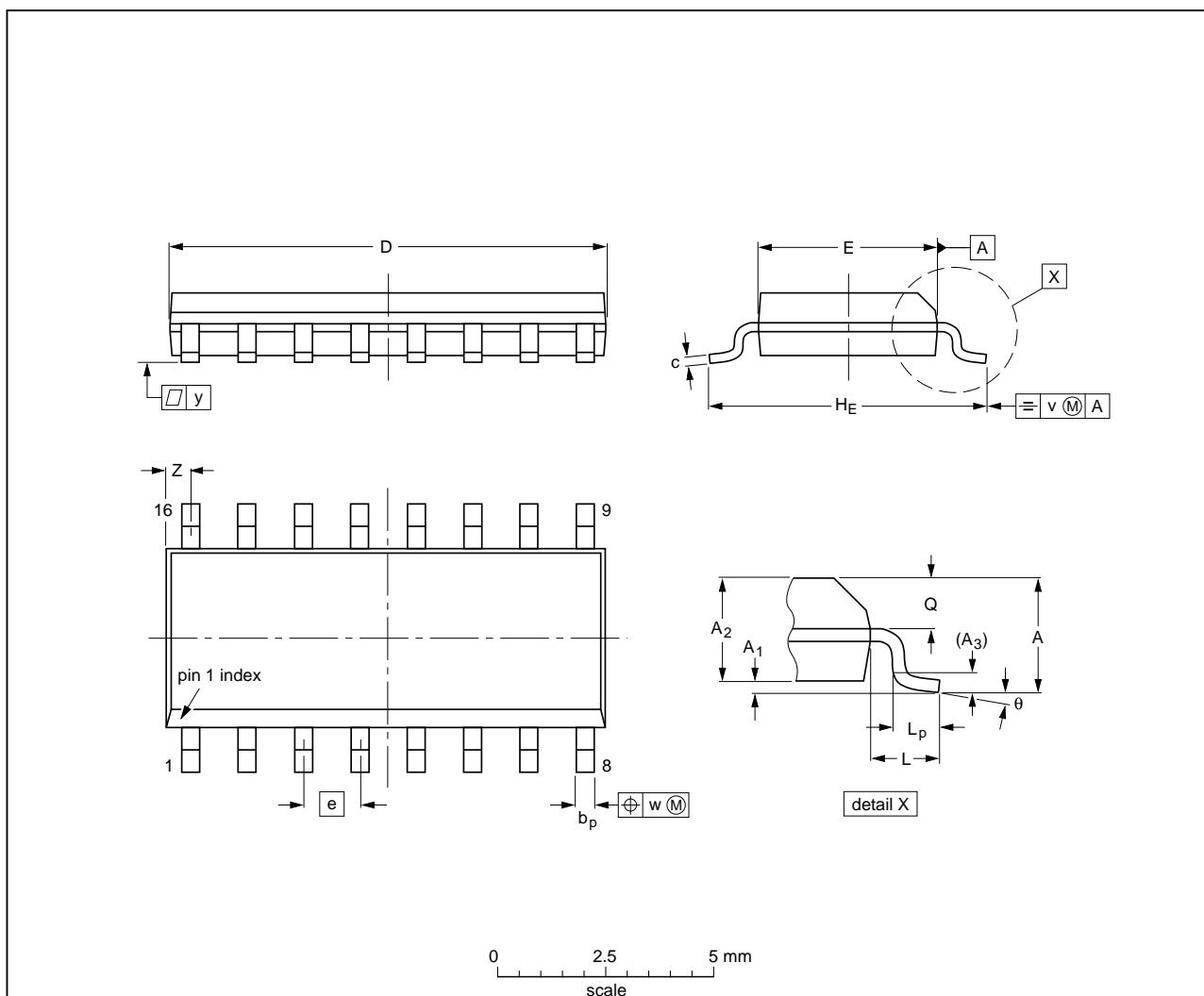
b. Typical frequency response

Fig 20. Test circuit for frequency response

## 13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig 21. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

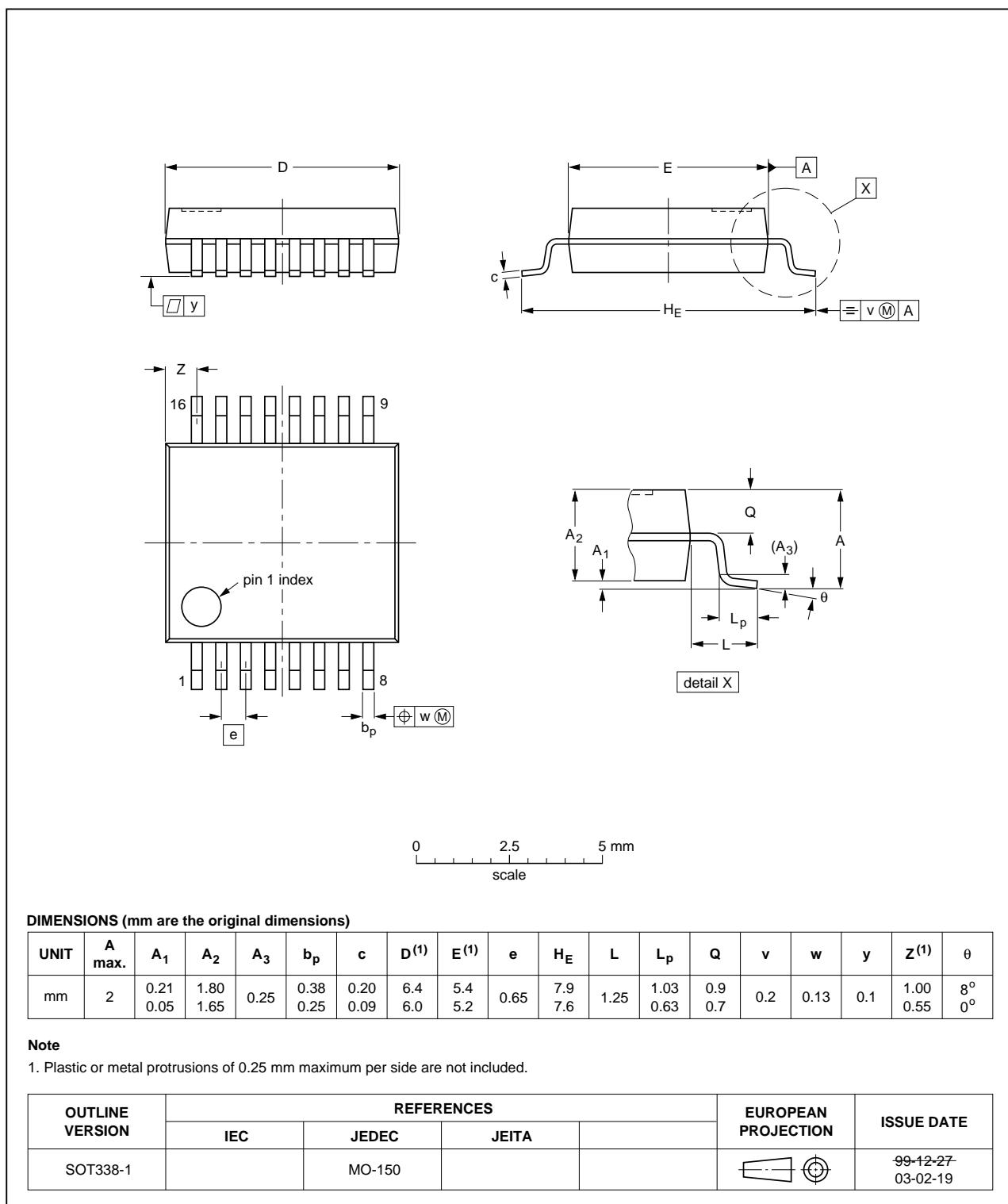
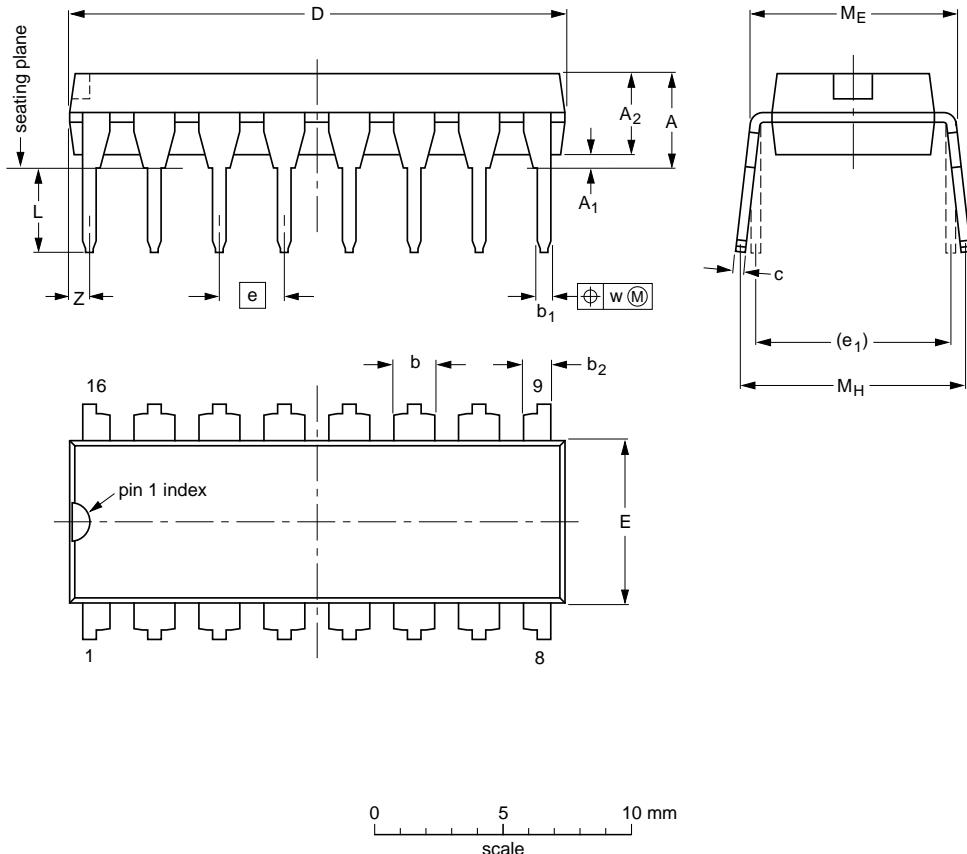


Fig 22. Package outline SOT338-1 (SSOP16)

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

## Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 23. Package outline SOT38-4 (DIP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

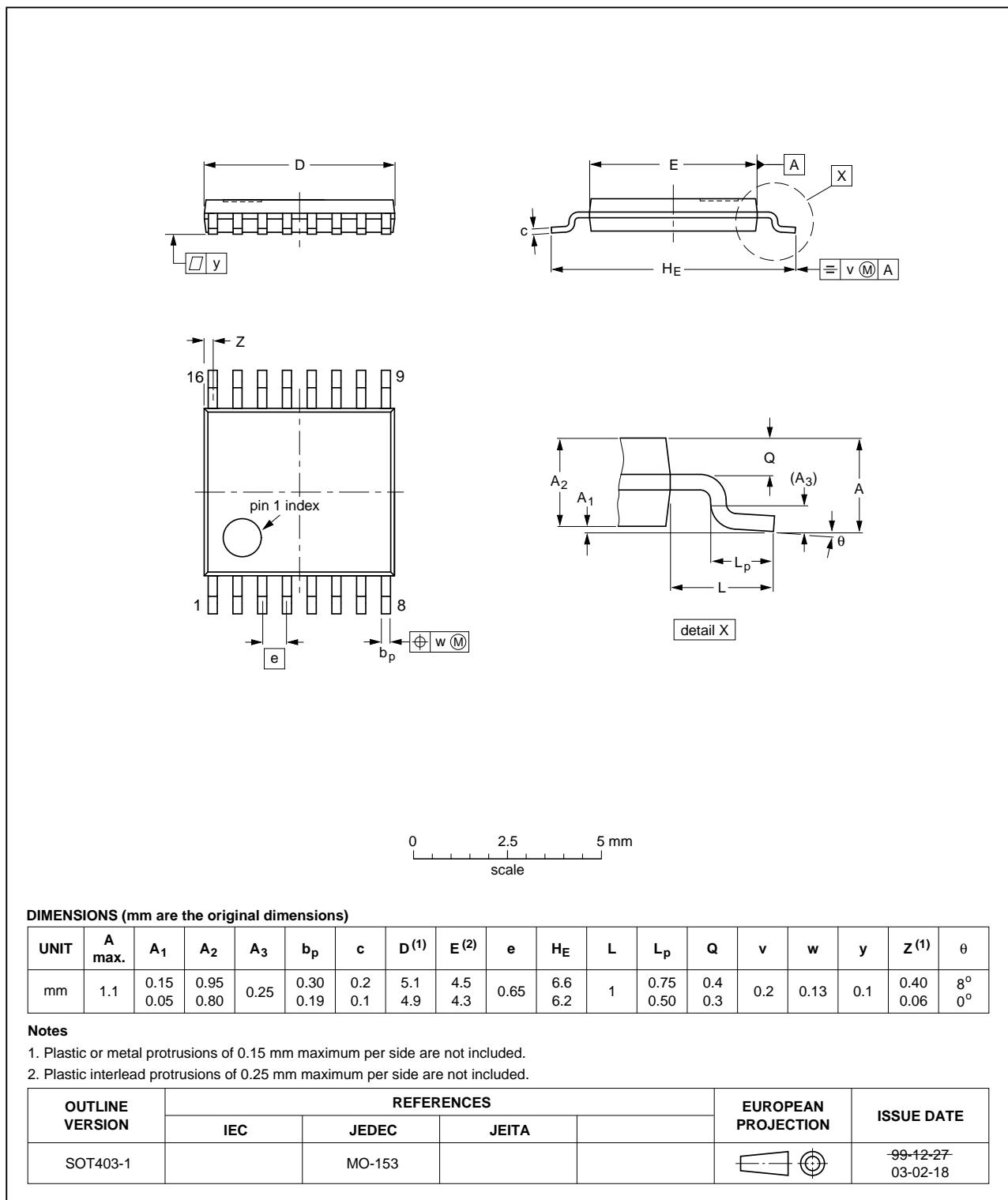


Fig 24. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

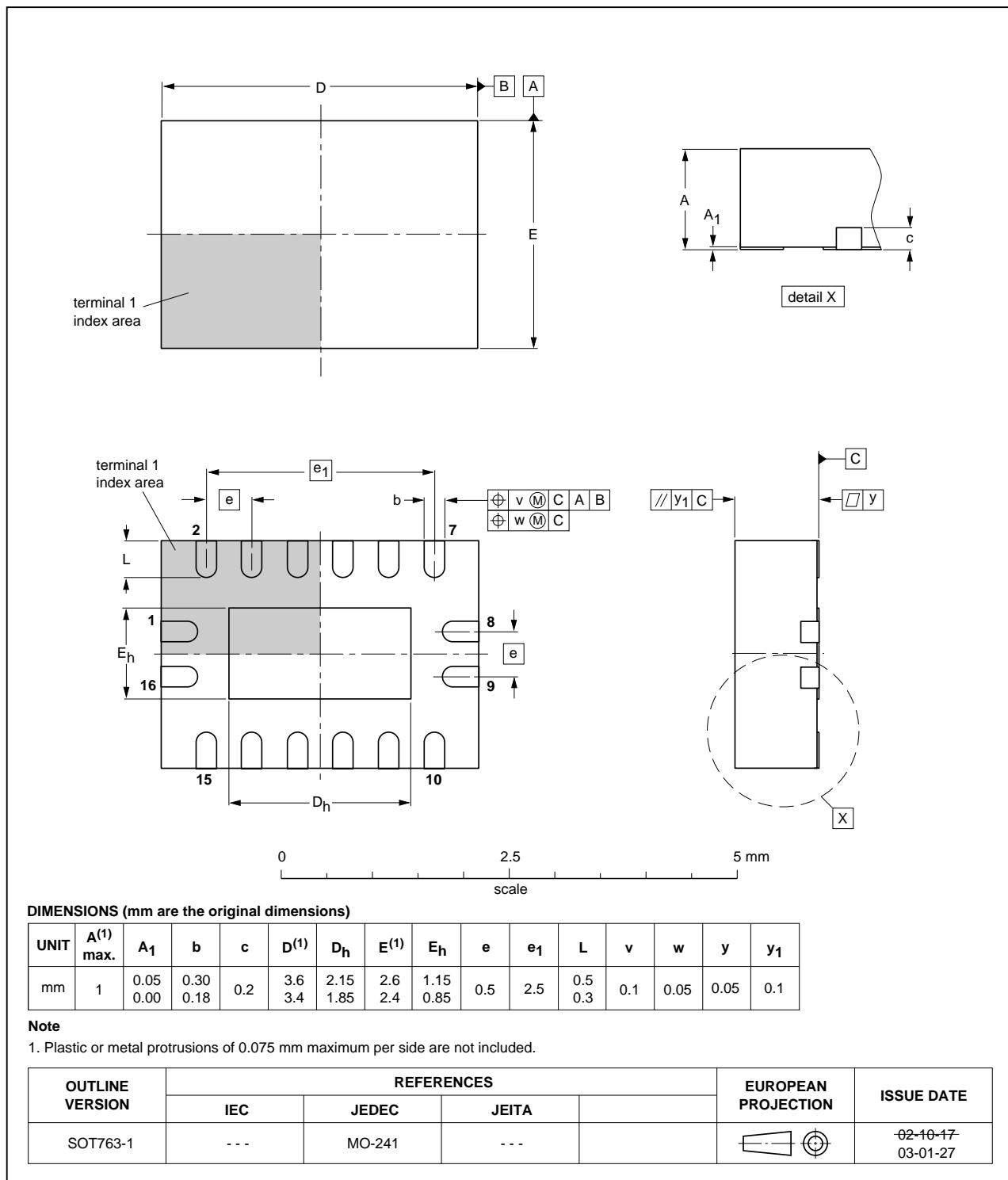


Fig 25. Package outline SOT763-1 (DHVQFN16)

## 14. Abbreviations

**Table 13. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

**Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4052 v.10	20120719	Product data sheet	-	74HC_HCT4052 v.9
Modifications:		• CDM added to features.		
74HC_HCT4052 v.9	20111213	Product data sheet	-	74HC_HCT4052 v.8
Modifications:		• Legal pages updated.		
74HC_HCT4052 v.8	20110511	Product data sheet	-	74HC_HCT4052 v.7
74HC_HCT4052 v.7	20110112	Product data sheet	-	74HC_HCT4052 v.6
74HC_HCT4052 v.6	20100111	Product data sheet	-	74HC_HCT4052 v.5
74HC_HCT4052 v.5	20080505	Product data sheet	-	74HC_HCT4052 v.4
74HC_HCT4052 v.4	20041111	Product specification	-	74HC_HCT4052 v.3
74HC_HCT4052 v.3	20030516	Product specification	-	74HC_HCT4052_CNV v.2
74HC_HCT4052_CNV v.2	19901201	-	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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