

Low Voltage / Low Power CMOS 16-bit Micro-controller

TMP93PW44DF

1. OUTLINE AND DEVICE CHARACTERISTICS

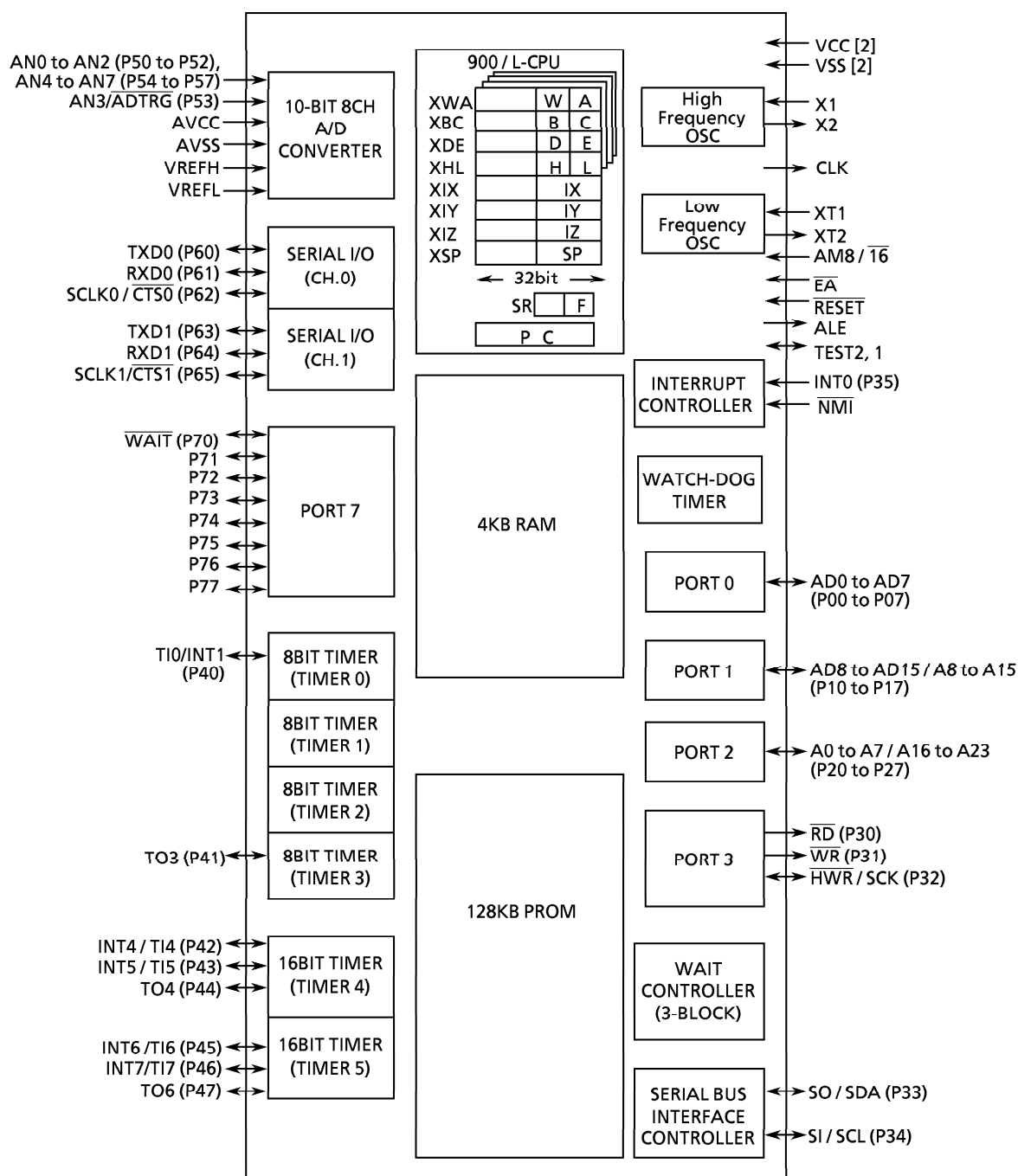
The TMP93PW44 is OTP type MCU which includes 128K byte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP93PW44. The TMP93PW44DF has the same pin-assignment as TMP93CW44 (Mask ROM type).

Writing the program to Built-in PROM, the TMP93PW44 operates as the same way as the TMP93CW44.

MCU	ROM	RAM	Package	Adapter Socket
TMP93PW44DF	OTP 128K-byte	4K-byte	QFP80-P-1420-0.80B	BM11152



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Note : The items in parentheses () are the initial setting after reset.

Figure 1 TMP93PW44 block diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for the TMP93PW44, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP93PW44DF.

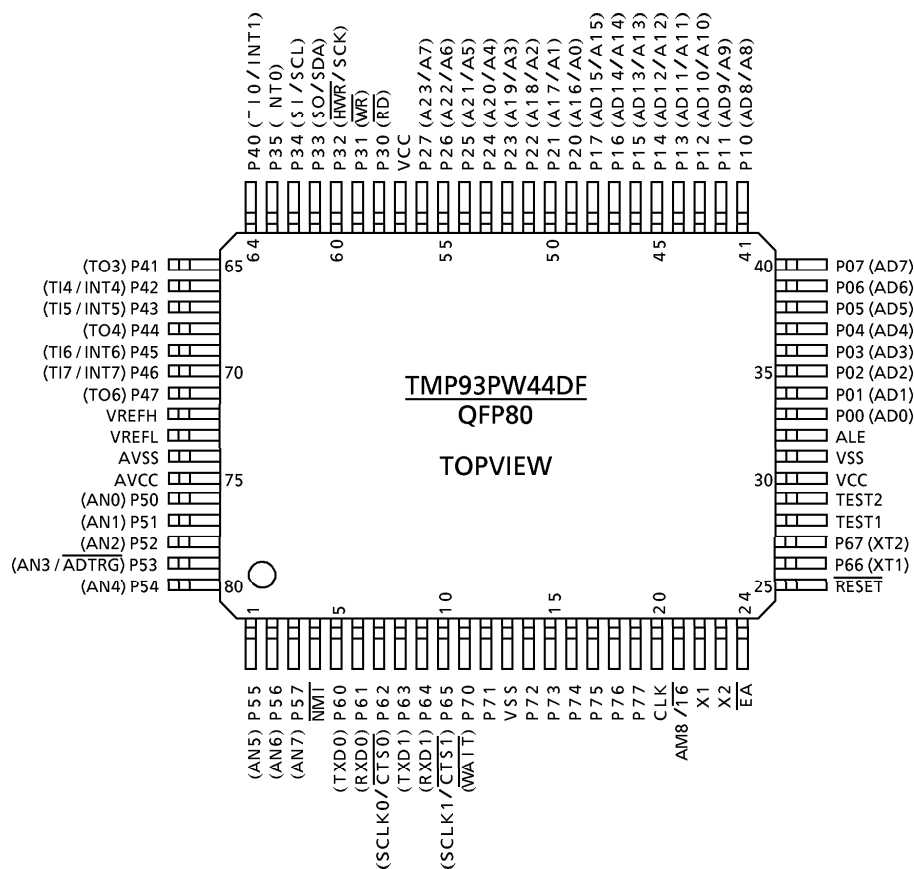


Figure 2.1 Pin Assignment (QFP80-P-1420-0.80B)

2.2 Pin Names and Functions

The TMP93PW44 has MCU mode and PROM mode.

- (1) Table 2.2 (1) shows pin function of TMP93PW44 in MCU mode.

Table 2.2 (1) Pin Names and Function (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 / AD0 to AD7	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
		3-state	Address/data (lower): Bits 0 to 7 for address/data bus
P10 to P17 / AD8 to AD15 / A8 to A15	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
		3-state	Address data (upper): Bits 8 to 15 for address/data bus
		Output	Address: Bits 8 to 15 for address bus
P20 to P27 / A0 to A7 / A16 to A23	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
		Output	Address: Bits 0 to 7 for address bus
		Output	Address: Bits 16 to 23 for address bus
P30 / $\overline{RD}$	1	Output	Port 30: Output port
		Output	Read: Strobe signal for reading external memory
P31 / $\overline{WR}$	1	Output	Port 31: Output port
		Output	Write: Strobe signal for writing data on pins AD0 to 7
P32 / $\overline{HWR}$ / SCK	1	I/O	Port 32: I/O port (with pull-up resistor)
		Output	High write: Strobe signal for writing data on pins AD8 to 15
		I/O	Mode clock SBI SIO mode clock
P33 / SO / SDA	1	I/O	Port 33: I/O port
		Output	Serial Send Data
		I/O	SBI I ² C bus mode channel data
P34 / SI / SCL	1	I/O	Port 34: I/O port
		Input	Serial Receive Data
		I/O	SBI I ² C bus mode clock
P35 / INT0	1	I/O	Port 35: I/O port
		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge 
P40 / TI0 / INT1	1	I/O	Port 40: I/O port
		Input	Timer input 0: Timer 0 input
		Input	Interrupt request pin 1: Interrupt request pin with rising edge 
P41 / TO3	1	I/O	Port 41: I/O port
		Output	PWM output 3: 8-bit PWM timer 3 output
P42 / TI4 / INT4	1	I/O	Port 42: I/O port
		Input	Timer input 4: Timer 4 count / capture trigger signal input
		Input	Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge 
P43 / TI5 / INT5	1	I/O	Port 43: I/O port
		Input	Timer input 5: Timer 4 count / capture trigger signal input
		Input	Interrupt request pin 5: Interrupt request pin with rising edge 
P44 / TO4	1	I/O	Port : I/O port
		Output	Timer output 4: Timer 4 output pin

Table 2.2 (1) Pin Names and Function (2/3)

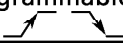
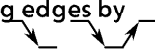
Pin name	Number of pins	I/O	Functions
P45 / TI6 / INT6	1	I/O	Port 45: I/O port
		Input	Timer input 6: Timer 5 count / capture trigger signal input
		Input	Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge 
P46 / TI7 / INT7	1	I/O	Port 46: I/O port
		Input	Timer input 7: Timer 5 count / capture trigger signal input
		Input	Interrupt request pin 7: Interrupt request pin with rising edge 
P47 / TO6	1	I/O	Port 47: I/O port
		Output	Timer output 6: Timer 5 output pin
P50 to P52, P54 to P57 / AN0 to AN2, AN4 to AN7	7	Input	Port 50 to Port 52, Port 54 to Port 57: Input port
		Input	Analog input: Analog signal input for A/D converter
P53 / AN3 / ADTRG	1	Input	Port53: Input Port
		Input	Analog input: Analog signal input for A/D converter
		Input	A/D converter external start trigger input
P60 / TXD0	1	I/O	Port 60: I/O port (with pull-up resistor)
		Output	Serial send data 0
P61 / RXD0	1	I/O	Port 61: I/O port (with pull-up resistor)
		Input	Serial receive data 0
P62 / CTS0 / SCLK0	1	I/O	Port 62: I/O port (with pull-up resistor)
		Input	Serial data send enable 0 (Clear to Send)
		I/O	Serial Clock I/O 0
P63 / TXD1	1	I/O	Port 63: I/O port (with pull-up resistor)
		Output	Serial send data 1
P64 / RXD1	1	I/O	Port 64: I/O port (with pull-up resistor)
		Input	Serial receive data 1
P65 / CTS1 / SCLK1	1	I/O	Port 65: I/O port (with pull-up resistor)
		Input	Serial data send enable 1 (Clear to Send)
		I/O	Serial clock I/O 1
P66 XT1	1	I/O	Port 66: I/O port (Open Drain Output)
		Input	Low Frequency Oscillator connecting pin
P67 XT2	1	I/O	Port 67: I/O port (Open Drain Output)
		Output	Low Frequency Oscillator connecting pin
P70 / WAIT	1	I/O	Port 70: I/O port (High current output available)
		Input	WAIT: Pin used to request CPU bus wait (It is active in 1 WAIT + N mode. Set by the Bus-width / wait control register.)
P71 to P77	7	I/O	Port 7: I/O port (High current output available)

Table 2.2 (1) Pin Names and Function (3/3)

Pin name	Number of pins	I/O	Functions
AVCC	1	Input	Power supply pin for A/D converter
AVSS	1	Input	GND pin for A/D converter (0 V)
VREFH	1	Input	Pin for high level reference voltage input to A/D converter
VREFL	1	Input	Pin for low level reference voltage input to A/D converter
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program. 
X1	1	Input	High Frequency Oscillator connecting pin
X2	1	Output	High Frequency Oscillator connecting pin
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93PW44. (With pull-up resistor)
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
CLK	1	Output	Clock output: Outputs " $f_{SYS} \div 2$ " Clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	External access: "1" should be inputted
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register.
VCC	2	Input	Power supply pin
VSS	2	Input	GND pin (All VSS pins are connected to the GND (0V).)
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.

Note : Built-in pull-up resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

(2) PROM mode

Table 2.2 (2) shows pin function of the TMP93PW44 in PROM mode.

Table 2.2 (2) Pin Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	$\overline{EA}$
VCC	3	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	3	Power supply	0 V	VSS, AVSS
Pin function	Number of pins	Input / Output	Disposal of pin	
P60	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Self oscillation with resonator	
X2	1	Output		
P66 to P61 AM8 / $\overline{16}$	7	Input	Fix to high level	
TEST1 / TEST2	2	Input / Output	Short	
P35, P34 P47 to P40 P57 to P50 P67 P77 to P70 VREFH VREFL $\overline{NMI}$	30	I/O	Open	

3. OPERATION

This section describes the functions and basic operational blocks of the TMP93PW44.

The TMP93PW44 has PROM in place of the mask ROM which is included in the TMP93CW44. The other configuration and functions are the same as the TMP93CW44. Regarding the function of the TMP93PW44 (not described), see the part of TMP93CW44.

The TMP93PW44 has two operational modes : MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CW44.

(2) Memory-map

The memory map of TMP93PW44 is same as that of TMP93CW44. Figure 3.1 (1) shows the memory map in MCU mode. Figure 3.1 (2) show that in PROM mode.

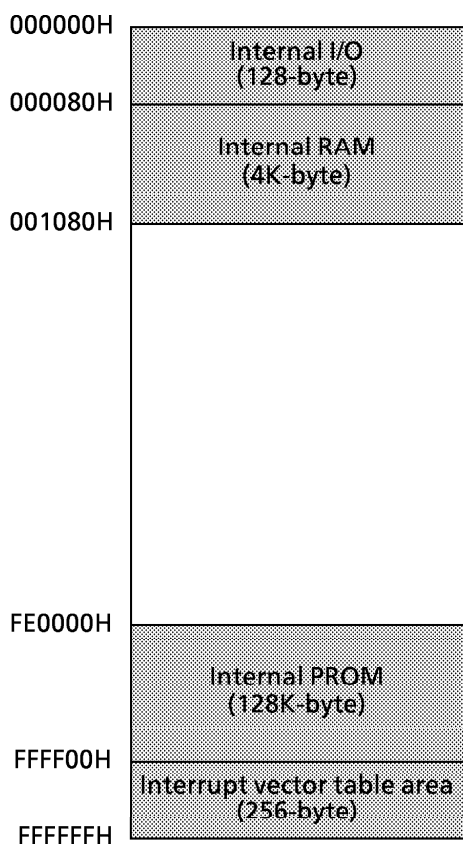


Figure 3.1 (1) Memory map in MCU mode

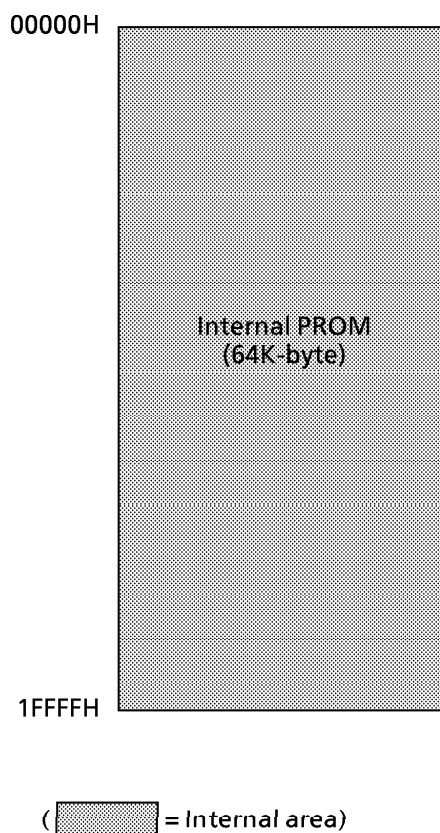


Figure 3.1 (2) Memory map in PROM mode

3.2 PROM Mode

(1) Mode setting and Function

PROM mode is set by setting the RESET and CLK pins to the “L” level. The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket.

① Preparation of OTP adaptor

BM11152 : for TMP93PW44DF

② Setting of OTP adaptor

The switch (SW1) is set to N side.

③ Setting of PROM writer

i) Set PROM type to TC 571000D.

Size : 1 Mbyte

VPP : 12.75 V

tpw : 100 μ s

Electric Signature mode : none

ii) Data transmission

In TMP93PW44, PROM is placed on addresses 00000 to 1FFFFFH in PROM mode, and addresses FE0000H to FFFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.)

iii) Setting of the program address

Start address : 00000H

End address : 1FFFFH

④ Programming

Program and verify according to operating process of PROM programmer.

Figure 3.2 (1) shows the setting of the pins in PROM mode.

Figure 3.2 (1) shows the setting of pins in PROM mode.

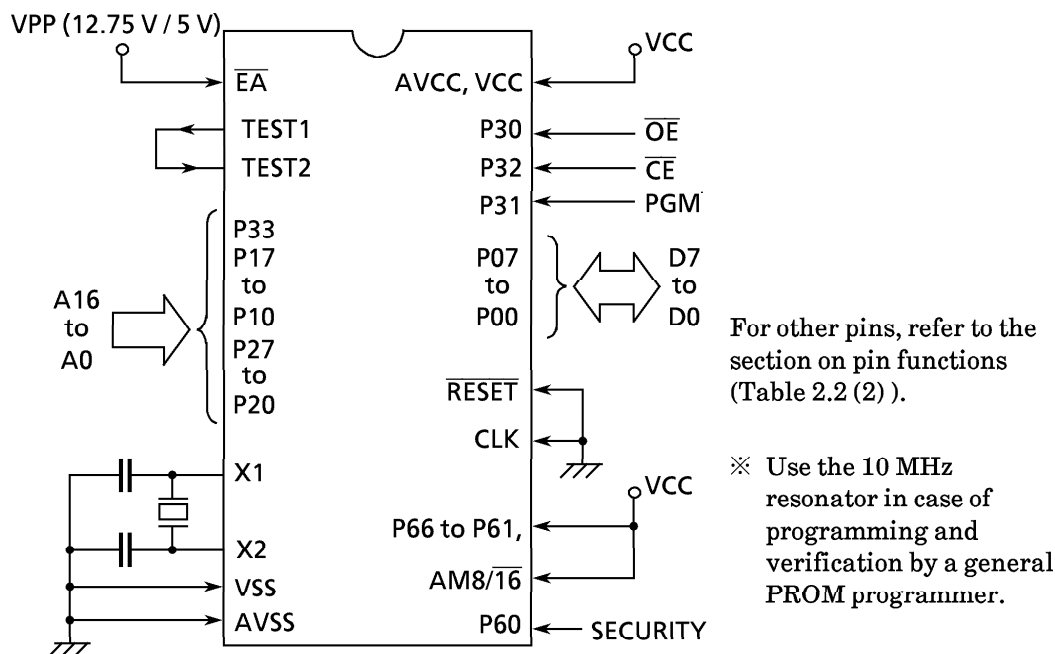


Figure 3.2 (1) PROM Mode Pin Setting

(2) Caution for Electric Signature

The TMP93PW44 does not support the electric signature mode (hereinafter referred to as “signature”). If PROM programmer used the signature, the device would be damaged because of applying voltage of $12 \pm 0.5V$ to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program Mode

All bits of the TMP93PW44 are “1” when delivered (the erase state). Data “0” is written in the necessary bit location during program operating.

Writing function can be operated at $V_{PP} = 12.5 V$, $\overline{OE} = V_{IH}$, $\overline{CE} = V_{IL}$. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adaptor Socket (BM11152 : for TMP93PW44DF)

BM11152 is the adapter sockets to write data into the TMP93PW44. The TMP93PW44 has built-in one time PROM using a general EPROM programmer.

(5) Program Storing Area of PROM Mode

The TMP93PW44 has the program space (FE0000H to FFFFFFFH) of 128 K bytes. The address 0000H to 1FFFFH of PROM mode equals to the address FE0000H to FFFFFFFH of MCU mode.

(6) Program Write Setting Method Using a general EPROM programmer

PROM to be prepared should equal to TC571000D functions.

1. Set the switch (SW1) of BM11152 (hereinafter referred to as “adapter”) to the program side (NOR). (Note1)
2. Connect MCU to the adapter. (Note2)
3. Connect the adapter to PROM programmer. (Note2)
4. Set the PROM type of PROM programmer to TC571000D.
5. Set the start address for writing PROM to 0000H, and the end address to 1FFFFH. (Note 3)
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

Note1: If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

Note2: Please set with the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or programmer would be damaged.

Note3: If data “0” is written to the address which is over 1FFFFH, the contents of the original program would be damaged because of writing “0” to the addresses 0000H to 1FFFFH.

(7) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows,

(VCC : 6.25 V, $\overline{\text{RESET}}$: “L” level, CLK : “L” level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to “L” level, 0.1 ms of “L” level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of $V_{pp} = V_{cc} = 5 \text{ V}$ after all data were written.

Figure 3.2 (2) shows the programming flow chart.

High Speed Program Writing.

Flow chart

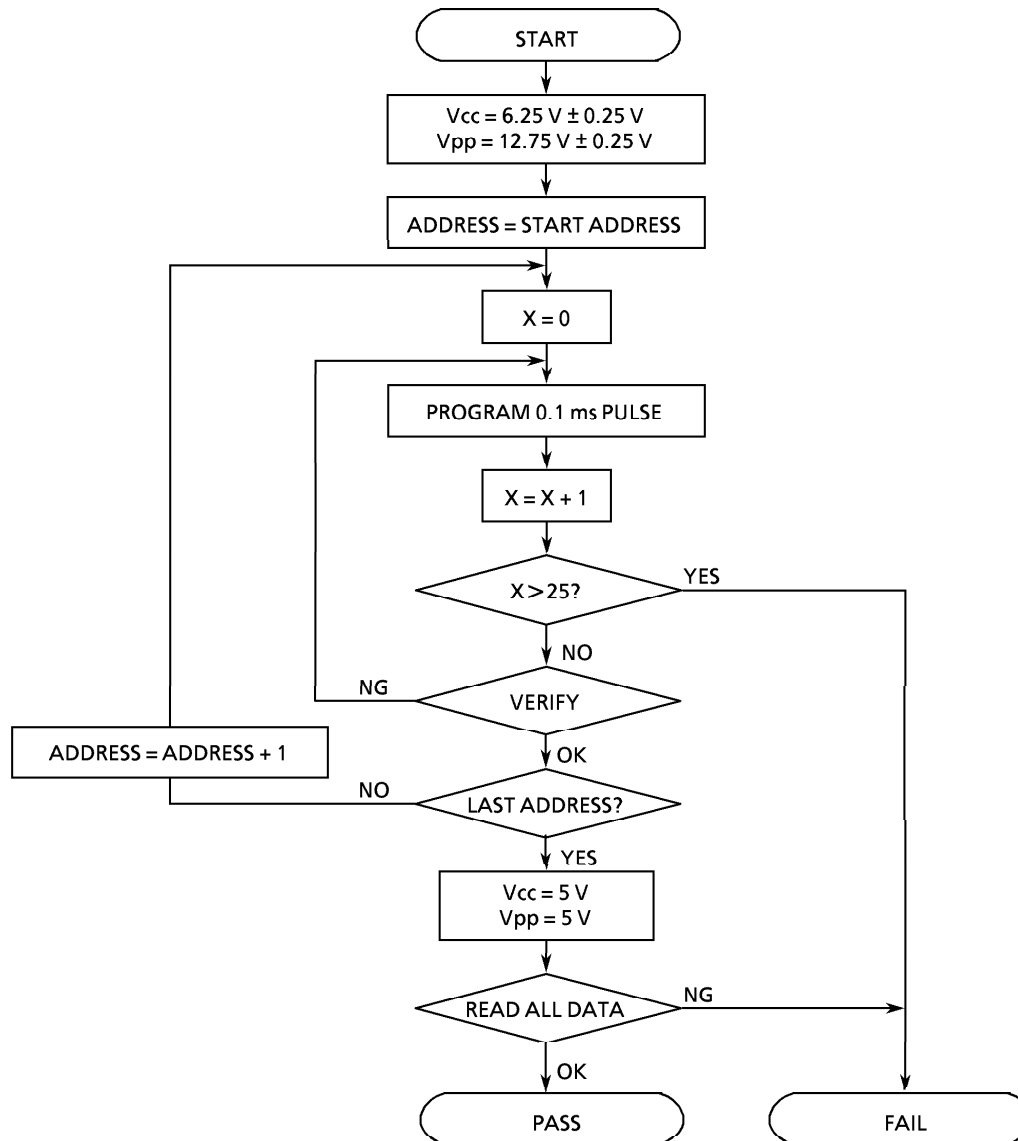


Figure 3.2 (2) Flow chart

(8) Security Bit

The TMP93PW44 has a Security Bit in PROM cell.

If the Security Bit is programmed to “0”, the content of the PROM is disable to be read (FFH data) in PROM mode.

(How to program the Security Bit.)

The difference from the programming procedures described in section 3.2 (1) are follows.

- ① Setting OTP adaptor
Set the switch (SW1) to S side.
- ② Setting PROM programmer
 - i) Transferring the data
 - ii) Setting of programming address

The security bit is in bit 0 of address 00000H.

Set the start address 00000H and the end address 00000H.

Set the data FEH at the address 00000H.

4. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

4.1 Absolute Maximum Ratings (TMP93PW44DF)

"X" used in an expression shows a cycle of clock from selected by SYSCR1 < SYSCK >. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at f_c , gear = 1/ f_c (SYSCR1 < SYSCK, GEAR 2 to 0 > = "0000").

Symbol	Parameter	Rating	Unit
V _{CC}	Power Supply Voltage	- 0.5 to 6.5	V
V _{IN}	Input Voltage	except $\overline{EA}$ pin - 0.5 to V _{CC} + 0.5 $\overline{EA}$ pin - 0.5 to 14.0	V
I _{OL1}	Output current (Per 1 pin) P7	20	mA
I _{OL2}	Output current (Per 1 pin) except P7	2	mA
Σ I _{OL1}	Output Current (P7 total)	80	mA
Σ I _{OL}	Output Current (total)	120	mA
Σ I _{OH}	Output Current (total)	- 80	mA
P _D	Power Dissipation (Ta = 85 °C)	350	mW
T _{SOLDER}	Soldering Temperature (10 s)	260	°C
T _{STG}	Storage Temperature	- 65 to 150	°C
T _{OPR}	Operating Temperature	- 40 to 85	°C

4.2 DC Characteristics (1/2)

Ta = - 40 to 85°C

Symbol	Parameter	Min.	Typ. (note1)	Max.	Unit	Condition
V _{CC}	Power Supply Voltage (AV _{CC} = V _{CC} AV _{SS} = V _{SS} = 0V)	4.5 2.7		5.5	V	f _c = 4 to 20 MHz f _s = 30 to 34 kHz
V _{IL}	Input Low Voltage	- 0.3		0.8	V	V _{CC} ≥ 4.5V
V _{IL1}				0.6		V _{CC} < 4.5V
V _{IL2}				0.3V _{CC}		V _{CC} = 2.7 to 5.5V
V _{IL3}				0.25V _{CC}		
V _{IL4}				0.3		
V _{IL4}	Input High Voltage	2.2 2.0 0.7V _{CC} 0.75V _{CC} V _{CC} - 0.3 0.8V _{CC}		V _{CC} + 0.3	V	V _{CC} ≥ 4.5V
V _{IH}						V _{CC} < 4.5V
V _{IH1}						V _{CC} = 2.7 to 5.5V
V _{IH2}						
V _{IH3}						
V _{IH4}						
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 1.6 mA (V _{CC} = 2.7 to 5.5V)
I _{OL7}	Output Low current (P7)	16 7			mA	V _{OL} = 1.0V (V _{CC} = 5V ± 10 %) (V _{CC} = 3V ± 10 %)
V _{OH1}	Output High Voltage	2.4			V	I _{OH} = - 400 μA (V _{CC} = 3V ± 10%)
V _{OH2}		4.2			V	I _{OH} = - 400 μA (V _{CC} = 5V ± 10%)

Note 1: Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min	Typ.(Note1)	Max	Unit	Condition
I_{DAR} (Note2)	Darlington Drive Current (8 Output Pins max.)	-1.0		-3.5	mA	$V_{EXT} = 1.5\text{ V}$ $R_{EXT} = 1.1\text{ k}\Omega$ ($V_{CC} = 5\text{ V} \pm 10\%$ only)
I_{LI}	Input Leakage Current		0.02	± 5	μA	$0.0 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		0.05	± 10		$0.2 \leq V_{IN} \leq V_{CC} - 0.2$
V_{STOP}	Power Down Voltage (at STOP, RAM Back up)	2.0		6.0	V	$V_{IL2} = 0.2 V_{CC}$, $V_{IH2} = 0.8 V_{CC}$
R_{PU}	Pull Up Resistance	45		130	$\text{k}\Omega$	$V_{CC} = 5.5\text{ V}$
		50		160		$V_{CC} = 4.5\text{ V}$
		70		280		$V_{CC} = 3.3\text{ V}$
		90		400		$V_{CC} = 2.7\text{ V}$
C_{IO}	Pin Capacitance			10	pF	$f_c = 1\text{ MHz}$
V_{TH}	Schmitt Width RESET, NMI, INTO	0.4	1.0		V	
I_{CC}	NORMAL (Note3)		27	33	mA	$V_{CC} = 5\text{ V} \pm 10\%$ $f_c = 20\text{ MHz}$
	RUN		22	27		
	IDLE2		16	19		
	IDLE1		4.2	7		
	NORMAL (Note3)		8.6	11	mA	$V_{CC} = 3\text{ V} \pm 10\%$ $f_c = 12.5\text{ MHz}$ (Typ. : $V_{CC} = 3.0\text{ V}$)
	RUN		7.7	10		
	IDLE2		6.3	7.2		
	IDLE1		1.2	1.8		
	SLOW (Note3)		27	41	μA	$V_{CC} = 3\text{ V} \pm 10\%$ $f_s = 32.768\text{ kHz}$ (Typ. : $V_{CC} = 3.0\text{ V}$)
	RUN		22	35		
	IDLE2		16	30		
	IDLE1		7	24		
	STOP		0.2	10	μA	$T_a \leq 50\text{ }^\circ\text{C}$
				20		$T_a \leq 70\text{ }^\circ\text{C}$
				50		$T_a \leq 85\text{ }^\circ\text{C}$
						$V_{CC} = 2.7\text{ V}$ to 5.5 V

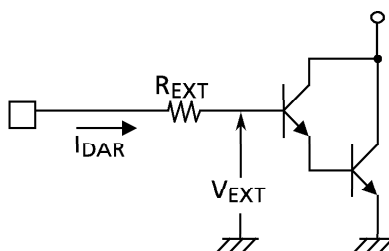
Note 1: Typical values are for $T_a = 25\text{ }^\circ\text{C}$ and $V_{CC} = 5\text{ V}$ unless otherwise noted.

Note 2: I_{DAR} is guaranteed for total of up to 8 ports.

Note 3: I_{CC} measurement conditions (NORMAL, SLOW):

Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of I_{DAR}



4.3 AC Electrical Characteristics

(1) $V_{CC} = 5\text{ V} \pm 10\%$

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	31250	62.5		50		ns
2	t_{CLK}	CLK width	$2x - 40$		85		60		ns
3	t_{AK}	A0 to 23 Valid → CLK Hold	$0.5x - 20$		11		5		ns
4	t_{KA}	CLK Valid → A0 to 23 Hold	$1.5x - 70$		24		5		ns
5	t_{AL}	A0 to 15 Valid → ALE fall	$0.5x - 15$		16		10		ns
6	t_{LA}	ALE fall → A0 to 15 Hold	$0.5x - 20$		11		5		ns
7	t_{LL}	ALE High width	$x - 40$		23		10		ns
8	t_{LC}	ALE fall → RD/WR fall	$0.5x - 25$		6		0		ns
9	t_{CL}	RD/WR rise → ALE rise	$0.5x - 20$		11		5		ns
10	t_{ACL}	A0 to 15 Valid → RD/WR fall	$x - 25$		38		25		ns
11	t_{ACH}	A0 to 23 Valid → RD/WR fall	$1.5x - 50$		44		25		ns
12	t_{CA}	RD/WR rise → A0 to 23 Hold	$0.5x - 25$		6		0		ns
13	t_{ADL}	A0 to 15 Valid → D0 to 15 input		$3.0x - 55$		133		95	ns
14	t_{ADH}	A0 to 23 Valid → D0 to 15 input		$3.5x - 65$		154		110	ns
15	t_{RD}	RD fall → D0 to 15 input		$2.0x - 60$		65		40	ns
16	t_{RR}	RD Low pulse width	$2.0x - 40$		85		60		ns
17	t_{HR}	RD rise → D0 to 15 Hold	0		0		0		ns
18	t_{RAE}	RD rise → A0 to 15 output	$x - 15$		48		35		ns
19	t_{WW}	WR Low pulse width	$2.0x - 40$		85		60		ns
20	t_{DW}	D0 to 15 Valid → WR rise	$2.0x - 55$		70		45		ns
21	t_{WD}	WR rise → D0 to 15 Hold	$0.5x - 15$		16		10		ns
22	t_{AWH}	A0 to 23 Valid → WAIT input ^(1 WAIT + n mode)		$3.5x - 90$		129		85	ns
23	t_{AWL}	A0 to 15 Valid → WAIT input ^(1 WAIT + n mode)		$3.0x - 80$		108		70	ns
24	t_{CW}	RD/WR fall → WAIT Hold ^(1 WAIT + n mode)	$2.0x + 0$		125		100		ns
25	t_{APH}	A0 to 23 Valid → PORT input		$2.5x - 120$		36		5	ns
26	t_{APH2}	A0 to 23 Valid → PORT Hold	$2.5x + 50$		206		175		ns
27	t_{CP}	WR rise → PORT Valid		200		200		200	ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
(However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, CLK)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
High 0.8 V_{CC} / Low 0.2 V_{CC} (Except for AD0 to AD15)

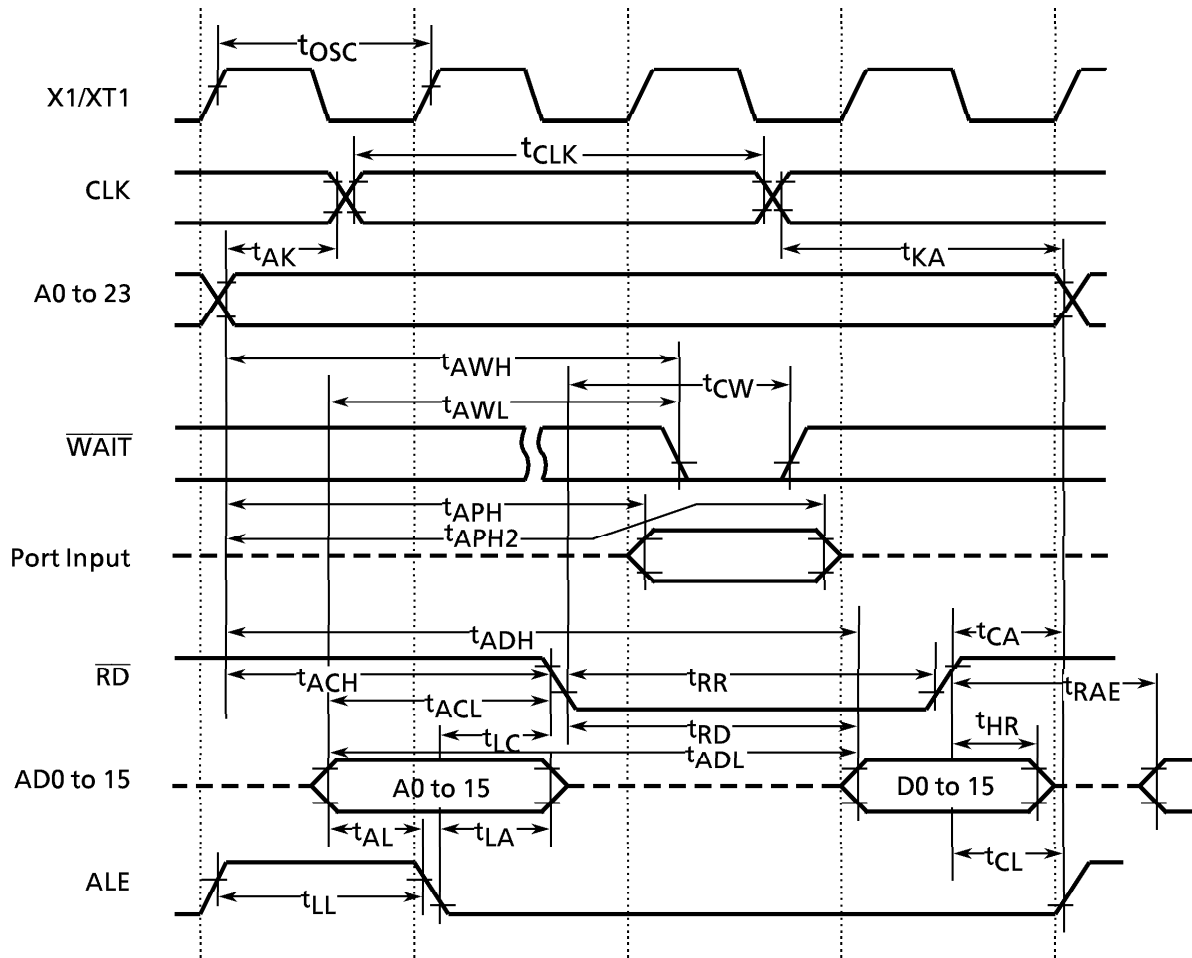
(2) $V_{CC} = 3\text{ V} \pm 10\%$

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	80	31250	80		ns
2	t_{CLK}	CLK width	$2x - 40$		120		ns
3	t_{AK}	A0 to 23 Valid → CLK Hold	$0.5x - 30$		10		ns
4	t_{KA}	CLK Valid → A0 to 23 Hold	$1.5x - 80$		40		ns
5	t_{AL}	A0 to 15 Valid → ALE fall	$0.5x - 35$		5		ns
6	t_{LA}	ALE fall → A0 to 15 Hold	$0.5x - 35$		5		ns
7	t_{LL}	ALE High width	$x - 60$		20		ns
8	t_{LC}	ALE fall → RD/WR fall	$0.5x - 35$		5		ns
9	t_{CL}	RD/WR rise → ALE rise	$0.5x - 40$		0		ns
10	t_{ACL}	A0 to 15 Valid → RD/WR fall	$x - 50$		30		ns
11	t_{ACH}	A0 to 23 Valid → RD/WR fall	$1.5x - 50$		70		ns
12	t_{CA}	RD/WR rise → A0 to 23 Hold	$0.5x - 40$		0		ns
13	t_{ADL}	A0 to 15 Valid → D0 to 15 input		$3.0x - 110$		130	ns
14	t_{ADH}	A0 to 23 Valid → D0 to 15 input		$3.5x - 125$		155	ns
15	t_{RD}	RD fall → D0 to 15 input		$2.0x - 115$		45	ns
16	t_{RR}	RD Low pulse width	$2.0x - 40$		120		ns
17	t_{HR}	RD rise → D0 to 15 Hold	0		0		ns
18	t_{RAE}	RD rise → A0 to 15 output	$x - 25$		55		ns
19	t_{WW}	WR Low pulse width	$2.0x - 40$		120		ns
20	t_{DW}	D0 to 15 Valid → WR rise	$2.0x - 120$		40		ns
21	t_{WD}	WR rise → D0 to 15 Hold	$0.5x - 40$		0		ns
22	t_{AWH}	A0 to 23 Valid → WAIT input ^(1 WAIT + n mode)		$3.5x - 130$		150	ns
23	t_{AWL}	A0 to 15 Valid → WAIT input ^(1 WAIT + n mode)		$3.0x - 100$		140	ns
24	t_{CW}	RD/WR fall → WAIT Hold ^(1 WAIT + n mode)	$2.0x + 0$		160		ns
25	t_{APH}	A0 to 23 Valid → PORT input		$2.5x - 120$		80	ns
26	t_{APH2}	A0 to 23 Valid → PORT Hold	$2.5x + 50$		250		ns
27	t_{CP}	WR rise → PORT Valid		200		200	ns

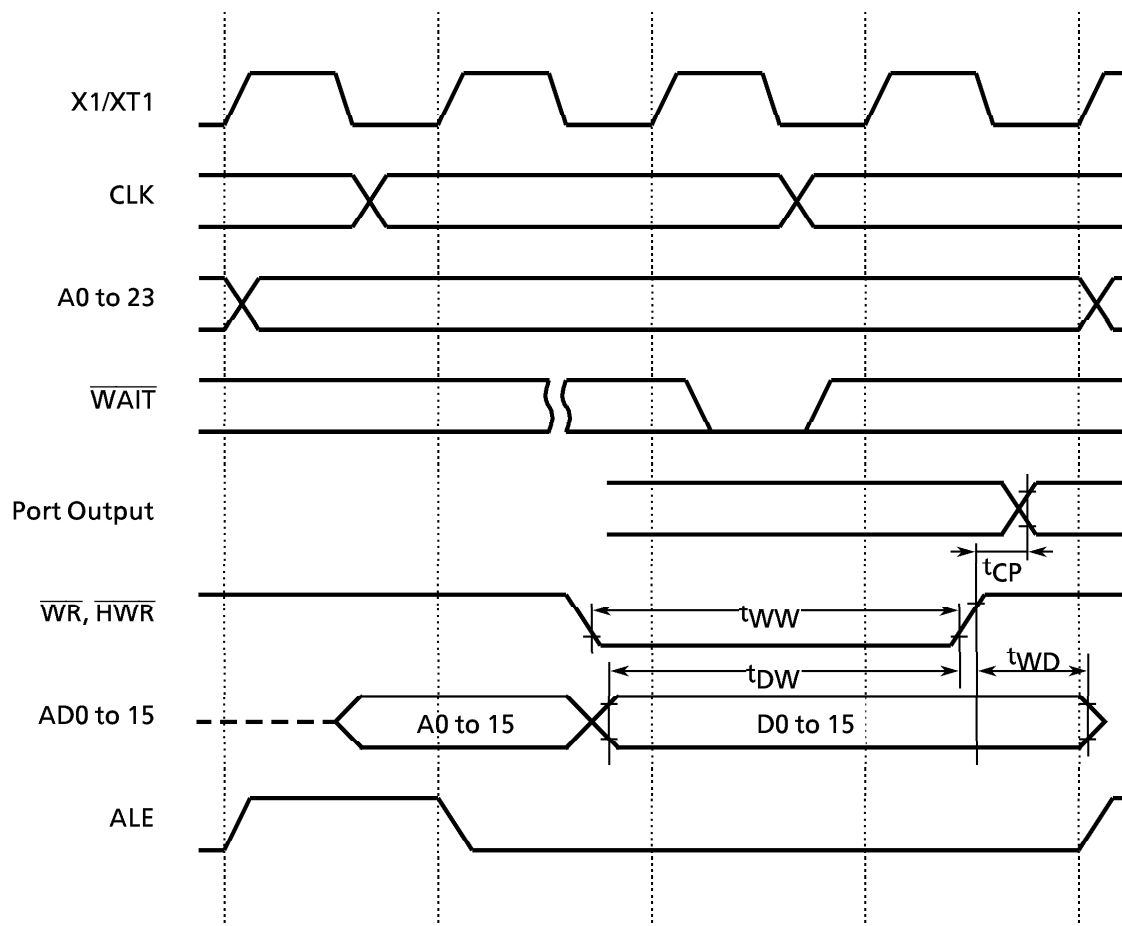
AC Measuring Conditions

- Output Level : High $0.7 \times V_{CC}$ / Low $0.3 \times V_{CC}$, CL = 50 pF
- Input Level : High $0.9 \times V_{CC}$ / Low $0.1 \times V_{CC}$

(1) Read Cycle



(2) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

Symbol	Parameter	Variable		(Note) 32.768 MHz		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16X		488 μs		1.28		0.8		μs
t_{OSS}	Output Data $\rightarrow$ falling edge of SCLK	$t_{SCY}/2 - 5X - 50$		91.5 μs		190		100		ns
t_{OHS}	SCLK rising / falling edge $\rightarrow$ Output Data hold	5X - 100		152 μs		300		150		ns
t_{HSR}	SCLK rising / falling edge $\rightarrow$ Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising / falling edge $\rightarrow$ effective data input		$t_{SCY} - 5X - 100$		336 μs		780		450	ns

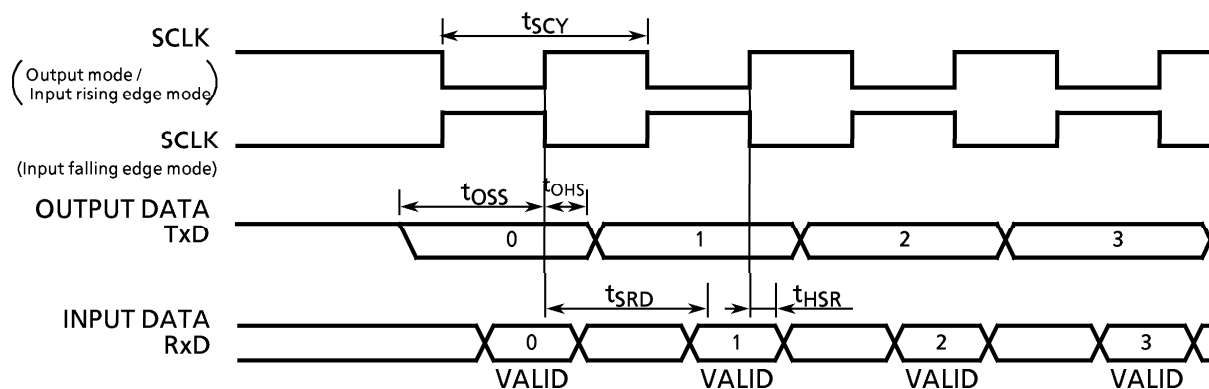
Note 1: When f_s is used as system clock or f_s divided by 4 is used as input clock to prescaler.

Note 2: SCLK rising/falling timing; SCLK rising in the rising mode of SCLK,
SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Symbol	Parameter	Variable		(Note) 32.768 MHz		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (Programmable)	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data $\rightarrow$ SCLK rising edge	$t_{SCY} - 2X - 150$		427 μs		970		550		ns
t_{OHS}	SCLK rising edge $\rightarrow$ Output Data hold	2X - 80		60 μs		80		20		ns
t_{HSR}	SCLK rising edge $\rightarrow$ Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising edge $\rightarrow$ effective Data input		$t_{SCY} - 2X - 150$		428 μs		970		550	ns

Note: When f_s is used as system clock or f_s divided by 4 is used as input clock to prescaler.



(2) UART Mode (SCLK0, 1 are external input)

Symbol	Parameter	Variable		32.768 kHz ^(Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{SCY}	SCLK cycle	4x + 20		122 μ s		340		220		ns
t _{SCYL}	SCLK Low level pulse width	2x + 5		6 μ s		165		105		ns
t _{SCYH}	SCLK High level pulse width	2x + 5		6 μ s		165		105		ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

4.5 A/D Conversion Characteristics

$$AV_{CC} = V_{CC}, AV_{SS} = V_{SS}$$

Symbol	Parameter	Power Supply	Min	Typ	Max	Unit
V _{REFH}	Analog reference voltage (+)	V _{CC} = 5V $\pm$ 10 %	V _{CC} - 0.2 V	V _{CC}	V _{CC}	V
		V _{CC} = 3V $\pm$ 10 %	V _{CC} - 0.2 V	V _{CC}	V _{CC}	
V _{REFL}	Analog reference voltage (-)	V _{CC} = 5V $\pm$ 10 %	V _{SS}	V _{SS}	V _{SS} + 0.2 V	
		V _{CC} = 3V $\pm$ 10 %	V _{SS}	V _{SS}	V _{SS} + 0.2 V	
V _{AIN}	Analog input voltage range		V _{REFL}		V _{REFH}	
I _{REF} (V _{REFL} = 0 V)	Analog current for analog reference voltage <VREFON> = 1	V _{CC} = 5V $\pm$ 10 %		0.5	1.5	mA
		V _{CC} = 3V $\pm$ 10 %		0.3	0.9	
	<VREFON> = 0	V _{CC} = 2.7 to 5.5V		0.02	5.0	μ A
-	Error (except quantization errors)	V _{CC} = 5V $\pm$ 10 %		$\pm$ 1.0	$\pm$ 3.0	LSB
		V _{CC} = 3V $\pm$ 10 %		$\pm$ 1.0	$\pm$ 5.0	

Note 1: 1LSB = (V_{REFH} - V_{REFL}) / 2¹⁰ [V]

Note 2: The operation above is guaranteed for f_{PPH} $\geq$ 4 MHz.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.6 Event Counter Input Clock (external input clock : TI0, TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t _{VCK}	Clock Cycle	8X + 100		740		500		ns
t _{VCKL}	Low level clock Pulse width	4X + 40		360		240		ns
t _{VCKH}	High level clock Pulse width	4X + 40		360		240		ns

4.7 Interrupt and Capture Operation

(1) $\overline{\text{NMI}}$, INT0 Interrupts

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t _{INTAL}	$\overline{\text{NMI}}$, INT0 Low level Pulse width	4X		320		200		ns
t _{INTAH}	$\overline{\text{NMI}}$, INT0 High level Pulse width	4X		320		200		ns

(2) INT1, 4 to 7 Interrupts and Capture

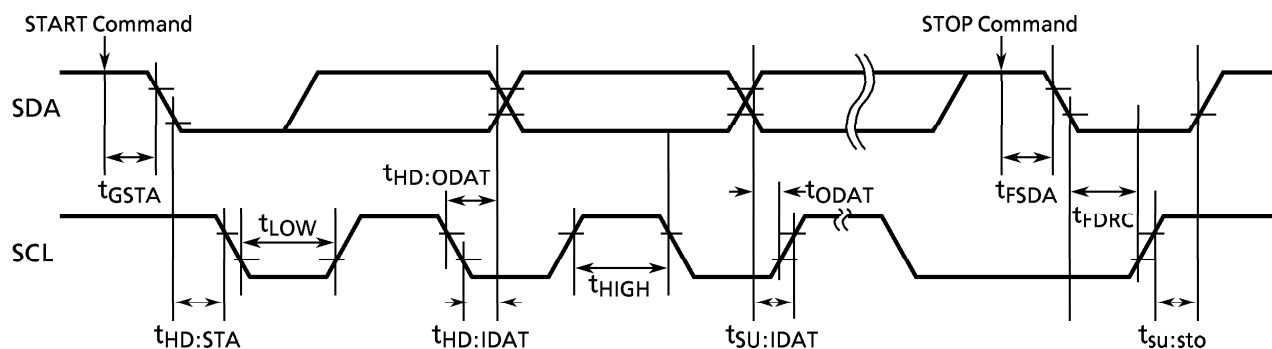
Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTBL}	INT1, INT4 to INT7 Low level Pulse width	$4X + 100$		420		300		ns
t_{INTBH}	INT1, INT4 to INT7 High level Pulse width	$4X + 100$		420		300		ns

4.8 Serial Bus Interface Timing

(1) I²C Bus Mode

Symbol	Parameter	Variable			Unit
		Min	Typ	Max	
t_{GSTA}	START command → SDA fall	3X			s
$t_{HD:STA}$	Hold time START condition	2^nX			s
t_{LOW}	SCL Low level pulse width	2^nX			s
t_{HIGH}	SCL High level pulse width	$2^nX + 12X$			s
$t_{HD:IDAT}$	Data hold time (input)	0			ns
$t_{SU:IDAT}$	Data set-up time (input)	250			ns
$t_{HD:ODAT}$	Data hold time (output)	7X		11X	s
t_{ODAT}	Data output → SCL Rising edge		$2^nX - t_{HD:ODAT}$		s
t_{FSDA}	STOP command → SDA fall	3X			s
t_{FDRC}	SDA Falling edge → SCL Rising edge	2^nX			s
$t_{SU:STO}$	Set-up time STOP condition	$2^nX + 16X$			s

Note : “n” value is set by SBICR1 <SCK2 to 0>



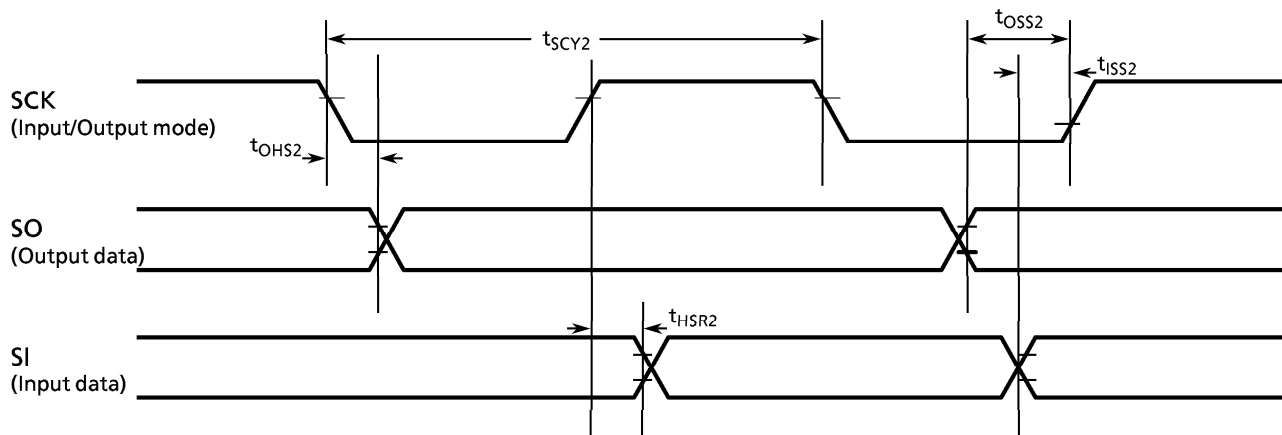
(2) Clocked-synchronous 8-bit SIO Mode

① SCK Input Mode

Symbol	Parameter	Variable		Unit
		Min	Max	
t_{SCY2}	SCK cycle	2^5X		s
t_{OHS2}	SCK falling edge → Output data hold	$6X$		s
t_{OSS2}	Output data → SCK rising edge	$t_{SCY2} - 6X$		s
t_{HSR2}	SCK rising edge → Input data hold	$6X$		ns
t_{ISS2}	Input data → SCK rising edge	0		ns

② SCK Output Mode

Symbol	Parameter	Variable		Unit
		Min	Max	
t_{SCY2}	SCK cycle	2^5X	$2^{11}X$	s
t_{OHS2}	SCK falling edge → Output data hold	$2X$		s
t_{OSS2}	Output data → SCK rising edge	$t_{SCY2} - 2X$		s
t_{HSR2}	SCK rising edge → Input data hold	$2X$		s
t_{ISS2}	Input data → SCK rising edge	0		ns



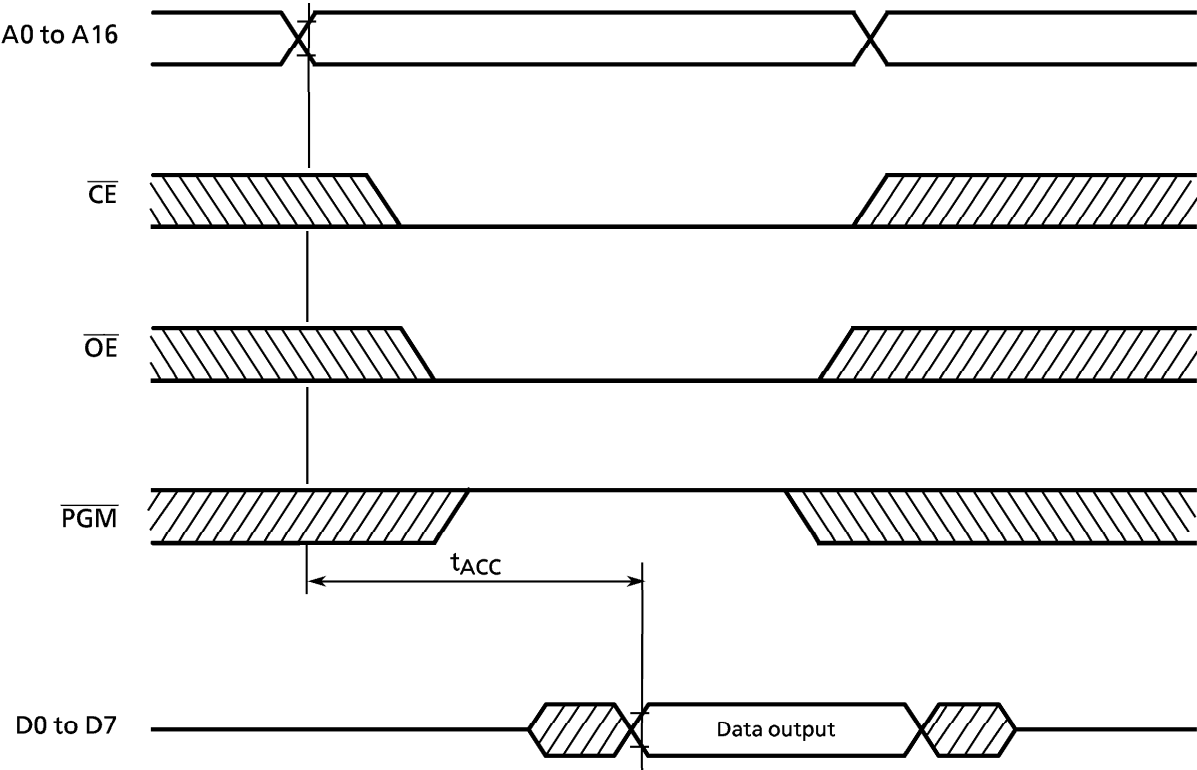
4.9 Read operation in PROM mode

DC / AC characteristics

$T_a = 25 \pm 5\text{ }^{\circ}\text{C}$ $V_{cc} = 5\text{ V} \pm 10\%$

Symbol	Parameter	Condition	Min	Max	Unit
V_{pp}	V_{pp} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.2	$V_{CC} + 0.3$	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3	0.8	V
t_{ACC}	Address to Output Delay	$C_L = 50\text{ pF}$	–	$2.25TCYC + \alpha$	ns

$TCYC = 400\text{ ns}$ (10 MHz Clock)
 $\alpha = 200\text{ ns}$

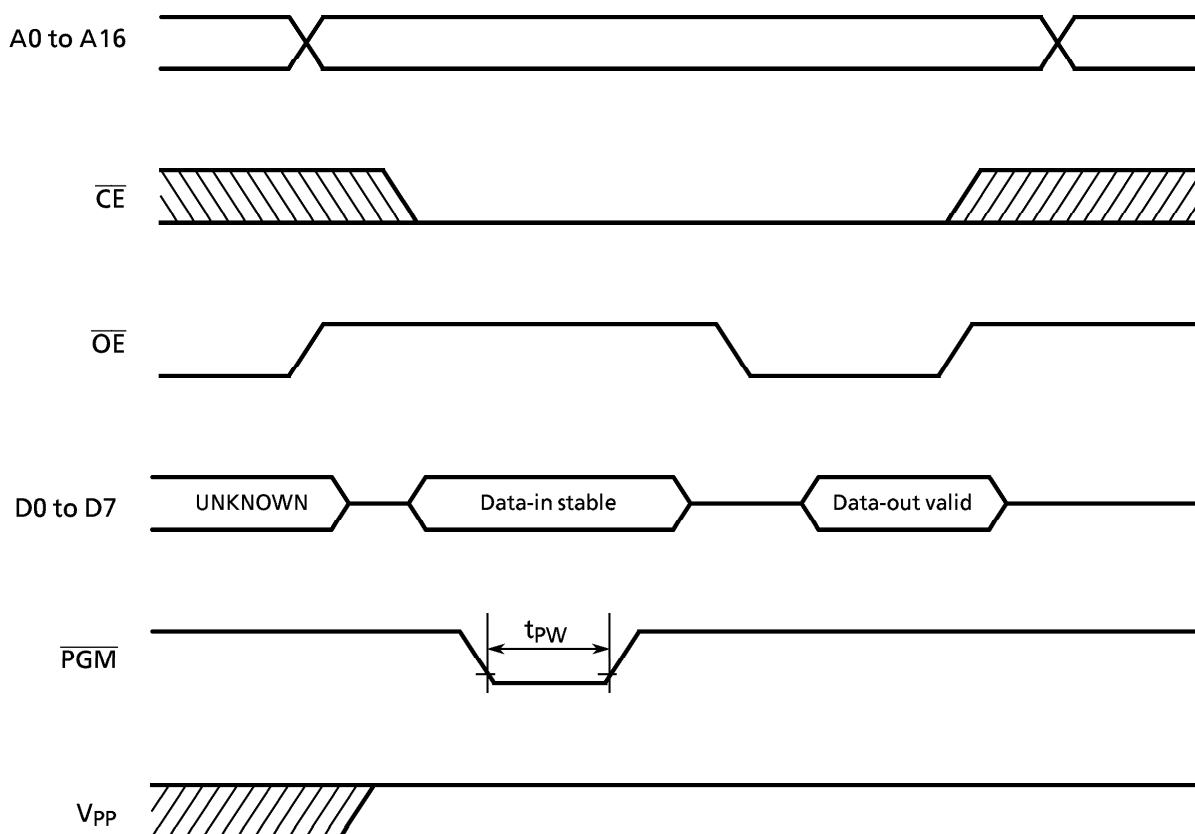


4.10 Program operation in PROM mode

DC / AC characteristics

 $T_a = 25 \pm 5^\circ\text{C}$ $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Supply Voltage	–	12.50	12.75	13.00	V
V_{IH}	Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, PGM)	–	2.6		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, PGM)	–	– 0.3		0.8	V
I_{CC}	V_{CC} Supply Current	$f_c = 10\text{ MHz}$	–		50	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = 13.00\text{ V}$	–		50	mA
t_{PW}	PGM Program Pulse Width	$C_L = 50\text{ pF}$	0.095	0.1	0.105	ms



NOTE

1. The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC} .
2. The pulling up/down device on condition of $V_{PP} = 12.75\text{ V}$ suffers a damage for the device.
3. The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.

