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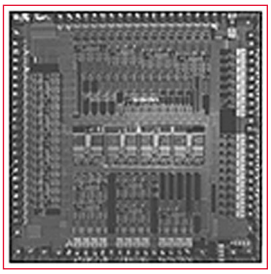
BCM8021 PRODUCT Brief



4-CHANNEL MULTIRATE 1.0–3.2-GBPS TRANSCEIVER WITH HIGH-SPEED REDUNDANCY

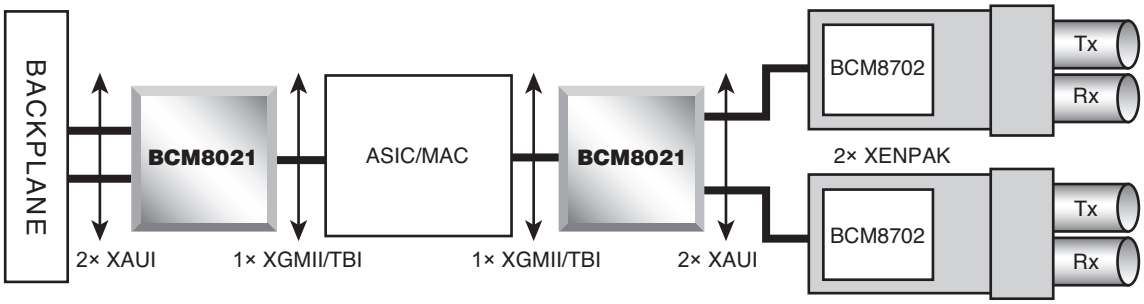
BCM8021 FEATURES

- **4 independent transceivers supporting multiple data rates from 1.0 Gbps to 3.2 Gbps including 1.06 Gbps, 1.25 Gbps, 2.12 Gbps, 2.488 Gbps, 2.667 Gbps, 3.125 Gbps, and 3.1875 Gbps**
- **Multiconfigurable to support various operating modes**
  - 4 Independent 1.0 to 3.2-Gbps SerDes transceivers
  - IEEE 802.3ae compliant XAUI to XGMII transceiver
  - XAUI-to-XAUI retiming
- **Low power dissipation**
  - Less than 300 mW per transceiver channel including I/O
- **SONET/SDH-quality jitter performance**
  - Less than 3 picoseconds rms jitter generation
  - Exceeds SONET jitter tolerance mask
- **High performance programmable Rx equalization and Tx pre-emphasis**
  - Tx pre-emphasis for interoperability with CML SerDes
  - Rx equalization for copper interconnects
- **Enhanced test capability**
  - Full loopback and on-chip PRBS generator/checker
  - IEEE 1149.1 JTAG
- **Compact 21-mm × 21-mm BGA package**
  - No requirement for heat sink or airflow

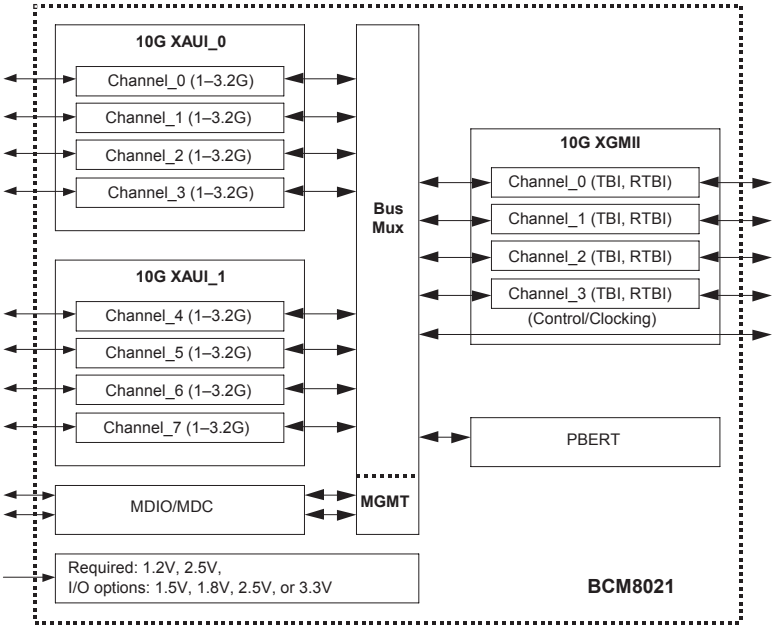
SUMMARY OF BENEFITS

- **One device supports a variety of applications including Gigabit Ethernet, 1× and 2× Fibre Channel, OC-48 SONET (with/without FEC), Infiniband, 10-Gigabit Ethernet, 10-Gigabit Fibre Channel, or others.**
- **Advanced 0.13-µ CMOS process technology provides unparalleled performance while achieving the lowest possible power consumption.**
- **IEEE 802.3ae 10-Gigabit Ethernet physical coding sublayer (PCS) has a selectable 8B/10B encoding/decoding block on-chip that can be configured to support the 10-Gbps Attachment Unit Interface (XAUI).**
- **Superior jitter characteristics enable the serializing/deserializing (SerDes) of data signals transmitted through front panel or backplane networking equipment supporting both primary and protection circuits.**
- **Drive PMD devices or backplane directly with no external clean-up circuit required.**
- **Simplifies manufacturability with itegrated Built-in self-test (BIST), high-speed and low-speed loopbacks, and programmable PRBS generator/checker.**
- **Decreases complexity and reduces board space on multichannel linecard designs.**

Independent Quad SerDes Application Diagram



BCM8021 Block Diagram



The **BCM8021** device integrates 4 independent serializer/deserializer (SerDes) channels leveraging Broadcom's high-performance mixed-signal design experience along with advanced 0.13-µ CMOS process technology. Combine this with a robust architecture offering the highest degree of flexibility and the result is a highly programmable, lowest power SerDes solution for network line-card and backplane applications.

An internal switch connects the parallel and serial ports to enable fully redundant operation. The switch enables an active serial link to be switched to the parallel interface, while a protection serial link can be continuously monitored to insure its condition. In the event of a failure on the active link the protection link can be instantly switched over through external control to the parallel interface.

On the parallel side of the device, transmitters and receivers interface with either 5-bit (RTBI) or 10-bit (TBI) wide data on each channel, or can be configured to interface to 32-bit wide data (XGMII) along with the clock and control signals. The low-speed I/O supports HSTL (1.5V or 1.8V) or SSTL_2 (2.5V) interfaces.

On the serial side of the device, transmitters and receivers support serial transmissions rates ranging from 1 Gbps to 3.2 Gbps. An on-chip phase lock loop (PLL) synthesizes the supplied reference clock to support the desired transmit rate, while vlock and data recovery (CDR) units recover the receive rate clock for timing. The interface can support single-channel (octal) or quad (XAUI) differential CML I/O.

For high-speed serial copper connections, the device incorporates both Tx pre-emphasis on the transmit channels and Rx equalization on the receive channels. Transmit pre-emphasis is programmable to improve the overall cable reach and compensate for electrical imperfections associated with traces and connectors. Rx equalization provides optimal performance over a variety of receive interfaces.

Highly programmable test capabilities exist within the device to support high-speed and low-speed loopback using generators/checkers that support PRBS 2^7 to 2^{31} patterns along with IEEE802.3ae defined test patterns.

A complete evaluation kit, including an evaluation board, related software, and documentation is available upon request.

Applications

- 1-Gigabit Ethernet and 10-Gigabit Ethernet LAN, MAN, WAN switches and routers
- 1×, 2×, or 10-Gbps Fibre Channel SONET network cards
- Advanced Test Equipment (ATE)

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