Low Skew, ÷1, ÷2 LVCMOS/LVTTL Clock Generator

ICS87946I-147

DATASHEET

General Description

The ICS87946I-147 is a low skew, ÷1, ÷2 LVCMOS/LVTTL Clock Generator. The ICS87946I-147 has two selectable single ended clock inputs. The single ended clock inputs accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

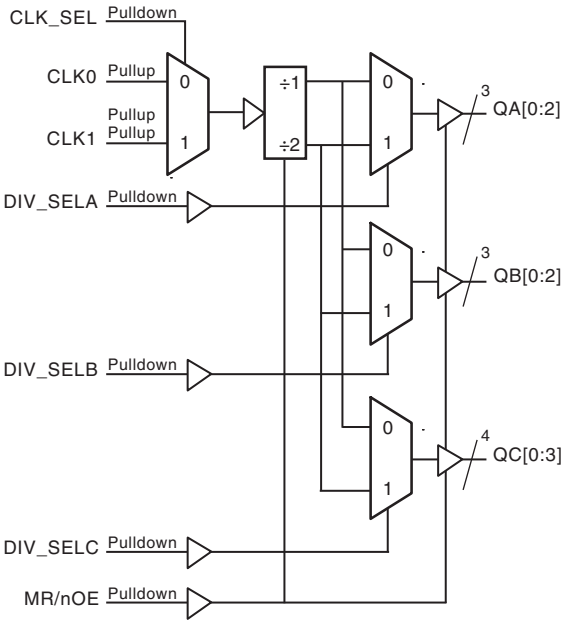
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87946I-147 is characterized at full 3.3V for input V_{DD}, and mixed 3.3V and 2.5V for output operating supply mode. Guaranteed bank, output and part-to-part skew characteristics make the ICS87946I-147 ideal for those clock distribution applications demanding well defined performance and repeatability.

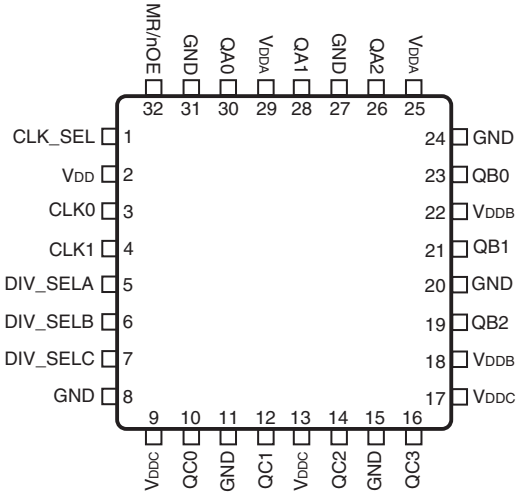
Features

- Ten single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable LVCMOS/LVTTL CLK0 and CLK1 inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum input frequency: 250MHz
- Bank skew: 30ps (maximum)
- Output skew: 175ps (maximum)
- Part-to-part skew: 850ps (maximum)
- Multiple frequency skew: 200ps (maximum)
- 3.3V core, 3.3V or 2.5V output supply modes
- -40°C to 85°C ambient operating temperature
- Lead-free packaging

Block Diagram



Pin Assignment



ICS87946I-147

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
2	V_{DD}	Power		Positive supply pin.
3, 4	CLK0, CLK1	Input	Pullup	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. See Table 3 LVCMOS/LVTTL interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. See Table 3. LVCMOS/LVTTL interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. See Table 3. LVCMOS/LVTTL interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground.
9, 13, 17	V_{DDC}	Power		Output supply pins for Bank C outputs.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Single-ended Bank C clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
18, 22	V_{DDB}	Power		Output supply pins for Bank B outputs.
19, 21, 23	QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
25, 29	V_{DDA}	Power		Output supply pins for Bank A outputs.
26, 28, 30	QA2, QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
32	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW Output Enable. When logic HIGH, the internal dividers are reset and the outputs are (High-Impedance). When logic LOW, the internal dividers and the outputs are enabled. See Table 3. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance	$V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.6V$		25		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

Function Tables

Table 3. Clock Input Function Table

Inputs				Outputs		
MR/nOE	**DIV_SELA**	**DIV_SELB**	**DIV_SELC**	**QA0:QA2**	**QB0:QB2**	**QC0:QC3**
1	X	X	X	High-Impedance	High-Impedance	High-Impedance
0	0	X	X	$f_{IN}/1$	Active	Active
0	1	X	X	$f_{IN}/2$	Active	Active
0	X	0	X	Active	$f_{IN}/1$	Active
0	X	1	X	Active	$f_{IN}/2$	Active
0	X	X	0	Active	Active	$f_{IN}/1$
0	X	X	1	Active	Active	$f_{IN}/2$

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDX}+ 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC}$ = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
V_{DDA}, V_{DDB}, V_{DDC}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				55	mA
I_{DDA}, I_{DDB}, I_{DDC}	Output Supply Current				23	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDA} = V_{DDB} = V_{DDC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}, V_{DDB}, V_{DDC}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA
I_{DDA}, I_{DDB}, I_{DDC}	Output Supply Current				22	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL	V_{DD} = V_{IN} = 3.6V			150	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.6V			5	µA
I_{IL}	Input Low Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDA} = V_{DDB} = V_{DDC} = 3.6V	2.6			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDA} = V_{DDB} = V_{DDC} = 3.63V			0.5	V
I_{OZL}	Output Hi-Z Current Low		V_{DDA} = V_{DDB} = V_{DDC} = 3.63V	-5			µA
I_{OZH}	Output Hi-Z Current High		V_{DDA} = V_{DDB} = V_{DDC} = 3.63V			5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4D. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDA} = V_{DDB} = V_{DDC} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR/nOE, DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDA} = V_{DDB} = V_{DDC} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDA} = V_{DDB} = V_{DDC} = 2.625V			0.5	V
I_{OZL}	Output Hi-Z Current Low		V_{DDA} = V_{DDB} = V_{DDC} = 2.625V	-5			µA
I_{OZH}	Output Hi-Z Current High		V_{DDA} = V_{DDB} = V_{DDC} = 2.625V			5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 250MHz	2		5	ns
*t*sk(b)	Bank Skew, NOTE 2, 7	Measured on rising edge at $V_{DDX}/2$			30	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDX}/2$			175	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDX}/2$			275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDX}/2$			850	ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%	400		950	ps
t_{PW}	Output Pulse Width		$t_{PERIOD}/2$ - 1	$t_{PERIOD}/2$	$t_{PERIOD}/2$ + 1	%
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			3	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			3	ns

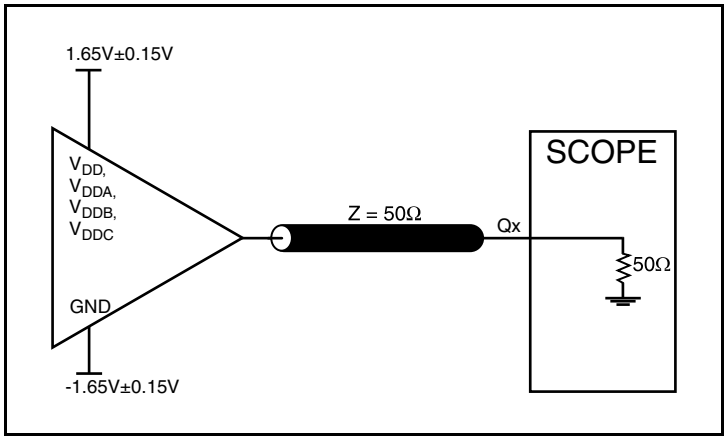
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDX}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDX}/2$.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltage and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDX}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDA} = V_{DDB} = V_{DDC} = 2.5V ± 5%, T_A = -40°C to 85°C

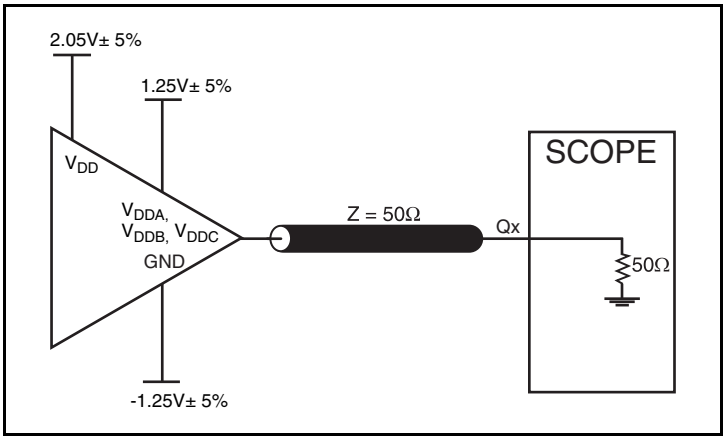
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 250MHz	2		5	ns
*t*sk(b)	Bank Skew, NOTE 2, 7	Measured on rising edge at V_{DDX}/2			35	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at V_{DDX}/2			175	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at V_{DDX}/2			200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at V_{DDX}/2			875	ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%	400		950	ps
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - 1	t_{PERIOD}/2	t_{PERIOD}/2 + 1	%
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			3	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			3	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDX}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltage and with equal load conditions. Measured at V_{DDX}/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltage and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDX}/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

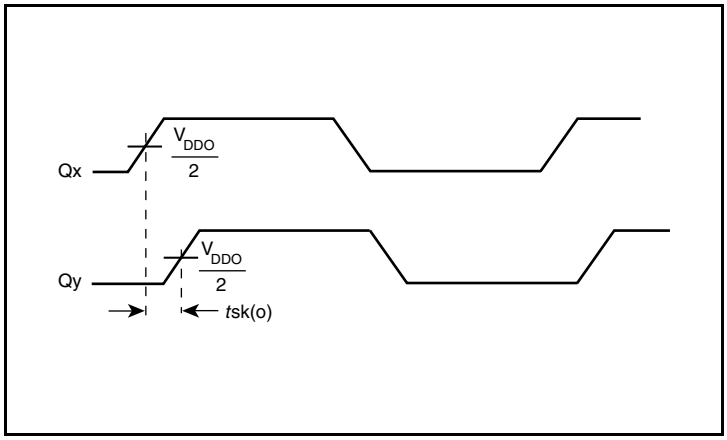
Parameter Measurement Information



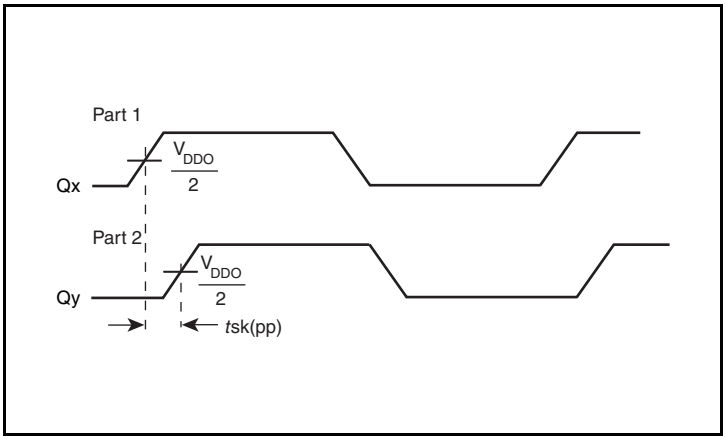
3.3V Core/3.3V Output Load AC Test Circuit



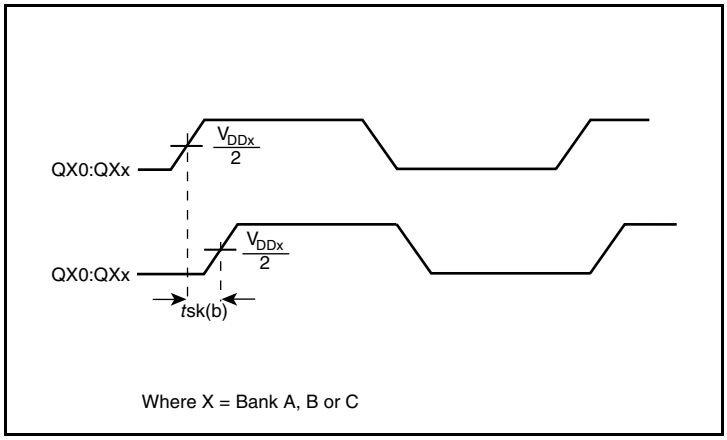
3.3V Core/2.5V Output Load AC Test Circuit



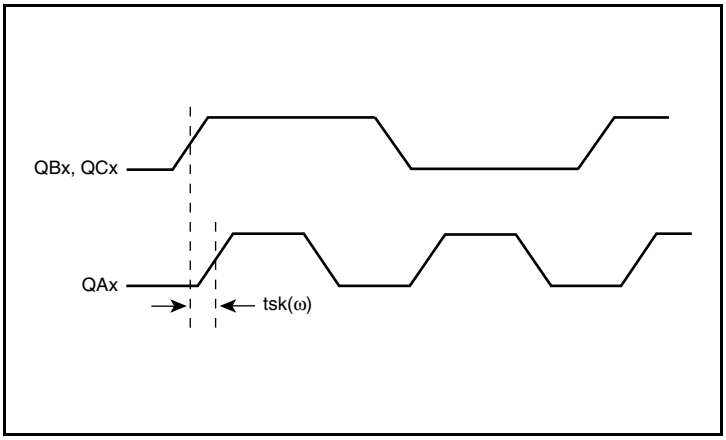
Output Skew



Part-to-Part Skew

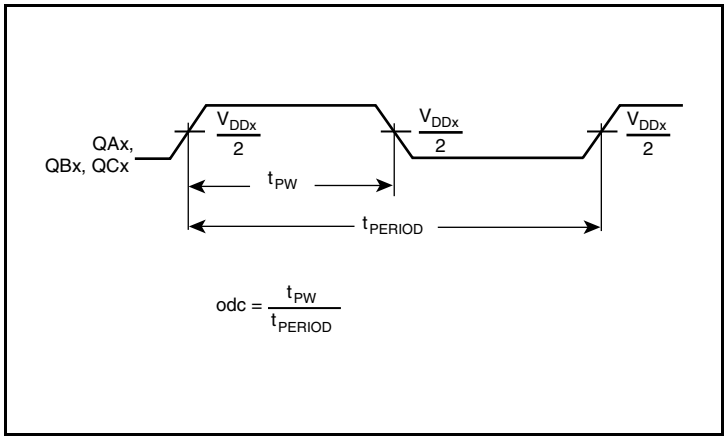


Bank Skew

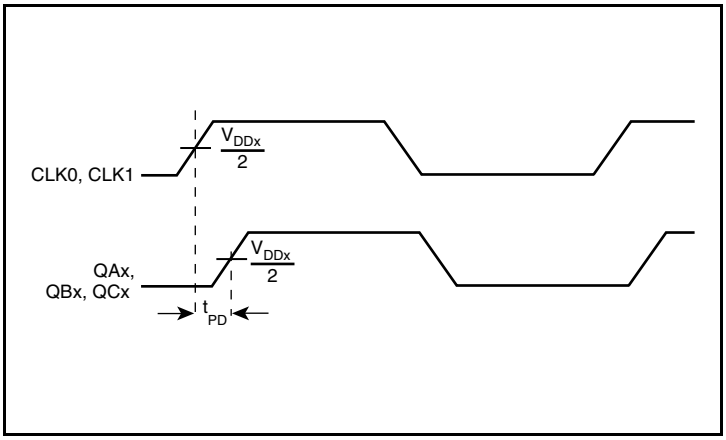


Multiple Frequency Skew

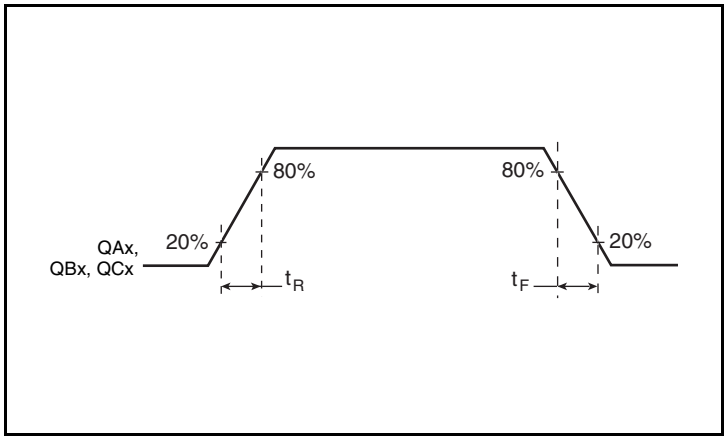
Parameter Measurement Information, continued



t_{PW} & t_{PERIOD}



Propagation Delay



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

OUTputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32-Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for ICS87946I-147 is: 1204
Pin compatible to the MPC9446 and MPC946

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32-Lead LQFP

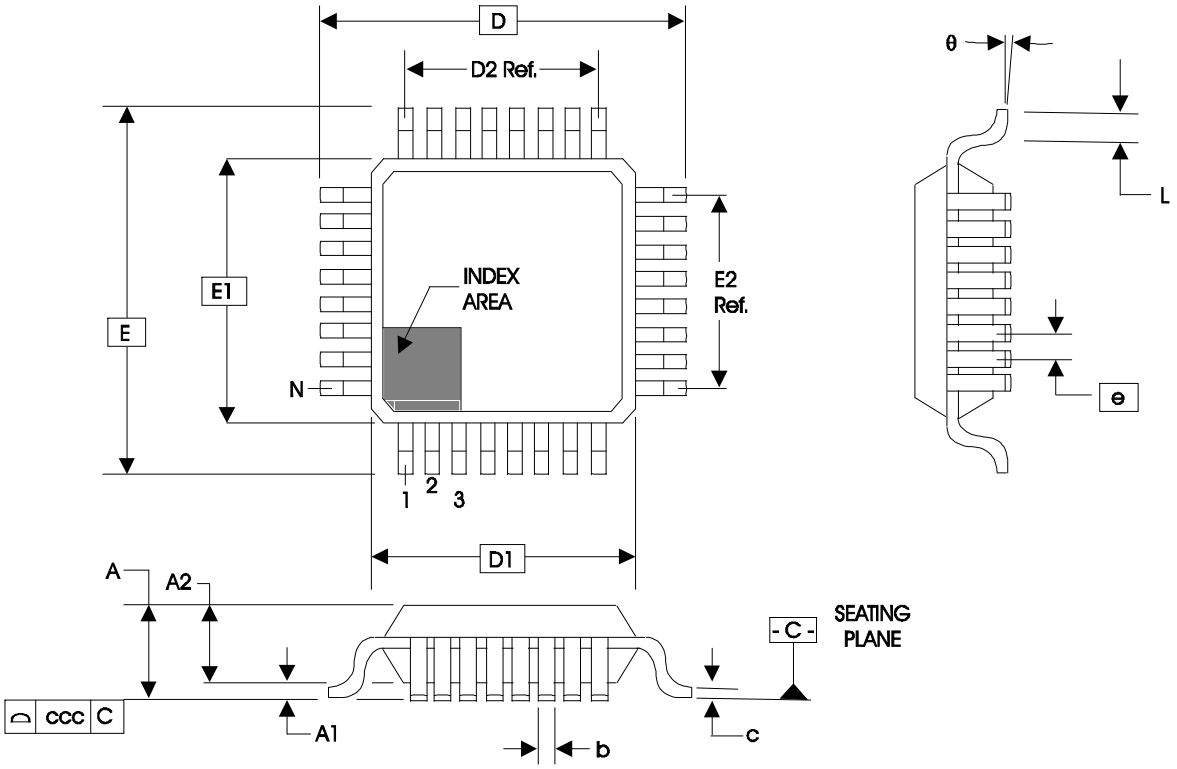


Table 7. Package Dimensions for 32-Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87946AYI-147LF	ICS7946AI147L	“Lead-Free” 32-Lead LQFP	Tray	-40°C to 85°C
87946AYI-147LFT	ICS7946AI147L	“Lead-Free” 32-Lead LQFP	Tape & Reel	-40°C to 85°C
87946AYI-147LF/W	ICS7946AI147L	“Lead-Free” 32-Lead LQFP	Tape & Reel, Pin1 Orientation: EIA-481-D	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T2 T8	1 2 8 10 12	Features section added *Lead-Free* bullet. Pin Description Table - corrected description for V_{DDA}, V_{DDB} and V_{DDC}. Parameter Measurement Information Section - added part-to-part skew, bank skew, and multiple frequency skew diagrams. Application Section - added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free marking. Updated format throughout the datasheet.	7/22/08
A	T5A - T5B T8	6 - 7 12	AC Tables - added thermal note. Ordering Information Table - corrected the Part/Order Numbers and corrected the non-LF marking. Updated Header/Footer of the datasheet.	8/7/09
A	T8	12	Removed leaded orderable parts from Ordering Information table	11/15/12
A	T8	12 14	Ordering Information Table - Added 87946AYI-147LF/W Ordering option. Updated Technical Support Contact Info to: clocks@idt.com	4/30/14

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