

BLF7G20L-250P; BLF7G20LS-250P

Power LDMOS transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I _{DQ} (mA)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR (dBc)
2-carrier W-CDMA	1805 to 1880	1900	28	70	18	35	-29.5 ^[1]

[1] Test signal: 3GPP; test model 1;64 DPCH; PAR = 8.4 dB at 0.01% probability on CCDF.

1.2 Features and benefits

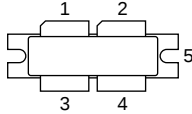
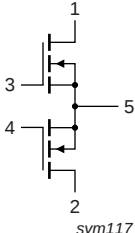
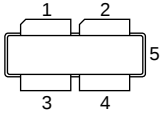
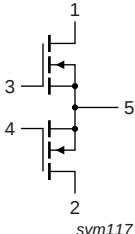
- Excellent ruggedness
- High-efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1880 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 1805 MHz to 1880 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF7G20L-250P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF7G20LS-250P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G20L-250P	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF7G20LS-250P	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	65	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 70\text{ W}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 1900\text{ mA}$; $T_j \leq 150\text{ °C}$	0.20	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 1.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 150\text{ mA}$	1.5	1.78	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	33.4	37.54	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	68.3	-	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 7.5\text{ A}$	-	12.37	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 5.25\text{ A}$	-	0.078	0.135	Ω

7. Test information

Table 7. 2-carrier W-CDMA functional test information

Class-AB production test circuit; $PAR = 8.4\text{ dB}$ at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; $f = 1805\text{ MHz}$ to 1880 MHz ; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 1900\text{ mA}$; $T_{case} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	70	-	W
G_p	power gain	$P_{L(AV)} = 70\text{ W}$	16	18	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 70\text{ W}$	-	-12	-	dB
η_D	drain efficiency	$P_{L(AV)} = 70\text{ W}$	30	35	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 70\text{ W}$	-	-29.5	-24.5	dBc

7.1 Ruggedness in class-AB operation

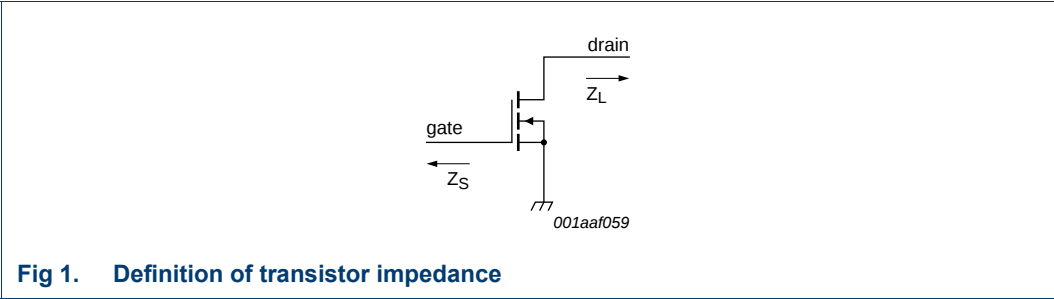
The BLF7G20L-250P and BLF7G20LS-250P are capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 1900\text{ mA}$; $P_{L(1dB)} = 245\text{ W}$ (CW); $f = 1805\text{ MHz}$ to 1880 MHz .

7.2 Impedance information

Table 8. Typical impedance
 Measured load-pull data half device; $I_{Dq} = 950\text{ mA}$; $V_{DS} = 28\text{ V}$.

f (MHz)	Z_S ^[1] (Ω)	Z_L ^[1] (Ω)
1750	1.31 – j3.53	2.47 – j3.91
1805	1.39 – j3.75	2.27 – j3.63
1845	1.48 – j4.10	2.32 – j3.19
1880	1.55 – j4.19	1.89 – j3.15
1930	1.97 – j4.48	1.70 – j2.95

[1] Z_S and Z_L defined in [Figure 1](#).



7.3 Single carrier W-CDMA

3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF. Channel bandwidth is 3.84 MHz; channel spacing = 5 MHz; $V_{DS} = 28$ V; $I_{Dq} = 1900$ mA

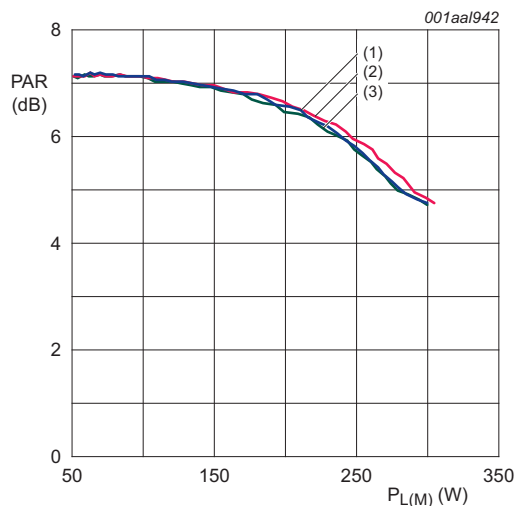


Fig 2. Peak-to-average power ratio as a function of peak output power; typical values

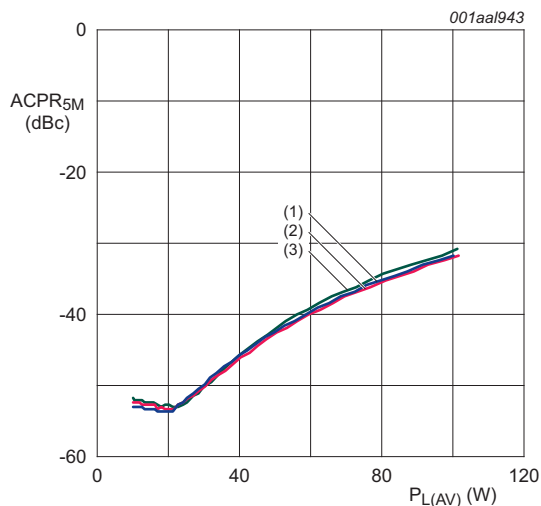


Fig 3. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values

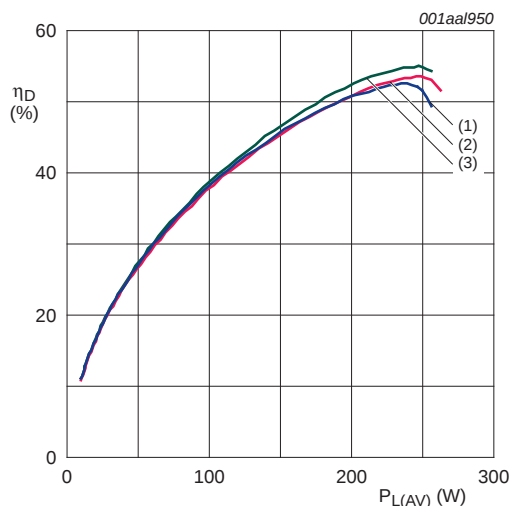


Fig 4. Efficiency as a function of average output power; typical values

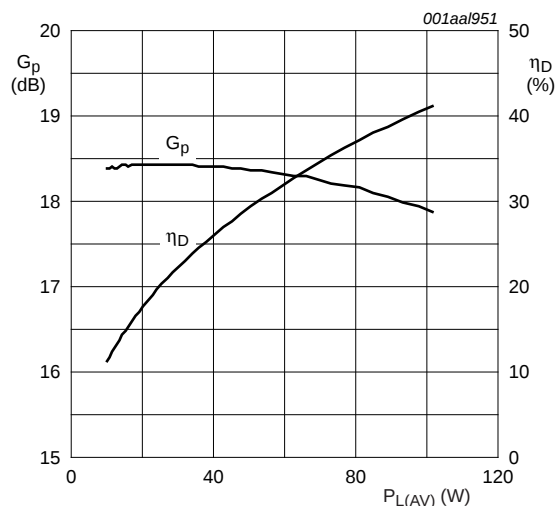
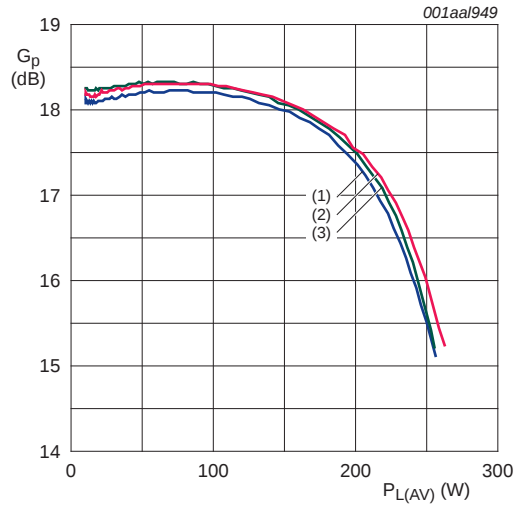


Fig 5. Power gain and drain efficiency as a function of average output power; typical values

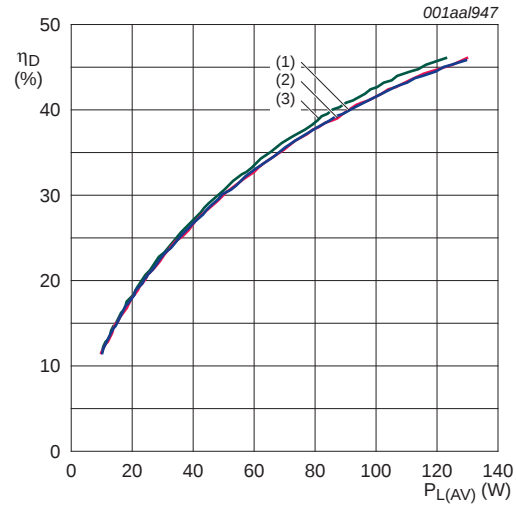
7.4 One tone CW

$V_{DS} = 28 \text{ V}$; $I_{DQ} = 1900 \text{ mA}$.



- (1) $f = 1805 \text{ MHz}$.
- (2) $f = 1845 \text{ MHz}$.
- (3) $f = 1880 \text{ MHz}$.

Fig 6. Power gain as a function of average output power; typical values

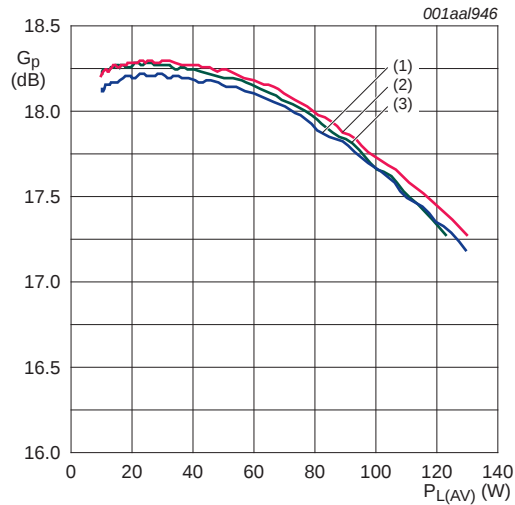


- (1) $f = 1805 \text{ MHz}$.
- (2) $f = 1845 \text{ MHz}$.
- (3) $f = 1880 \text{ MHz}$.

Fig 7. Efficiency as a function of average output power; typical values

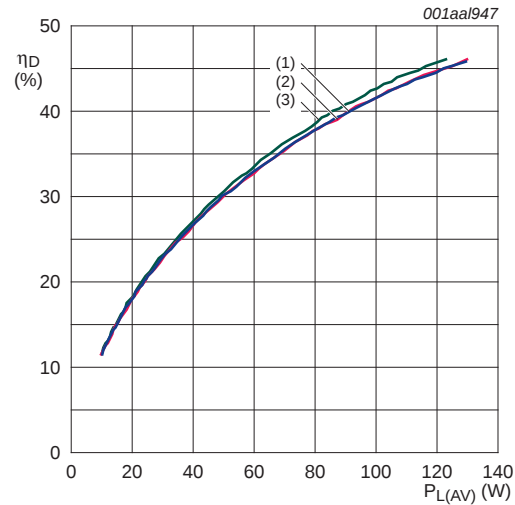
7.5 2-carrier WCDMA characteristics

$V_{DS} = 28 \text{ V}$; $I_{DQ} = 1900 \text{ mA}$; channel spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.



- (1) $f = 1805 \text{ MHz}$.
- (2) $f = 1845 \text{ MHz}$.
- (3) $f = 1880 \text{ MHz}$.

Fig 8. Power gain as a function of average output power; typical values



- (1) $f = 1805 \text{ MHz}$.
- (2) $f = 1845 \text{ MHz}$.
- (3) $f = 1880 \text{ MHz}$.

Fig 9. Efficiency as a function of average output power; typical values

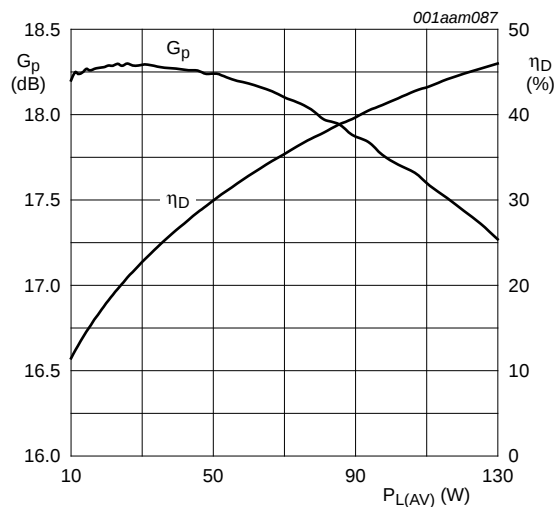
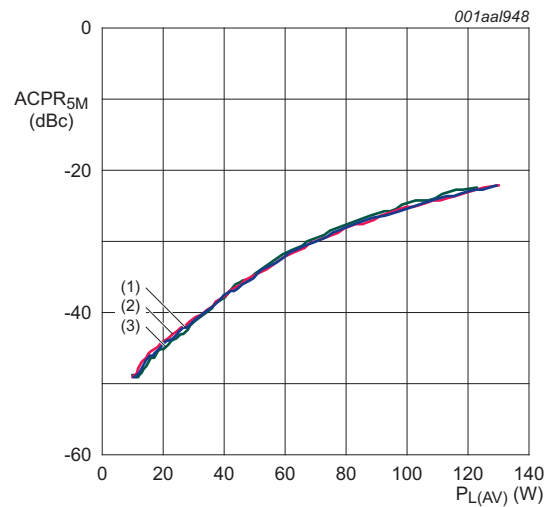


Fig 10. Average power gain and drain efficiency as a function of average output power; typical values



- (1) $f = 1805 \text{ MHz}$.
- (2) $f = 1845 \text{ MHz}$.
- (3) $f = 1880 \text{ MHz}$.

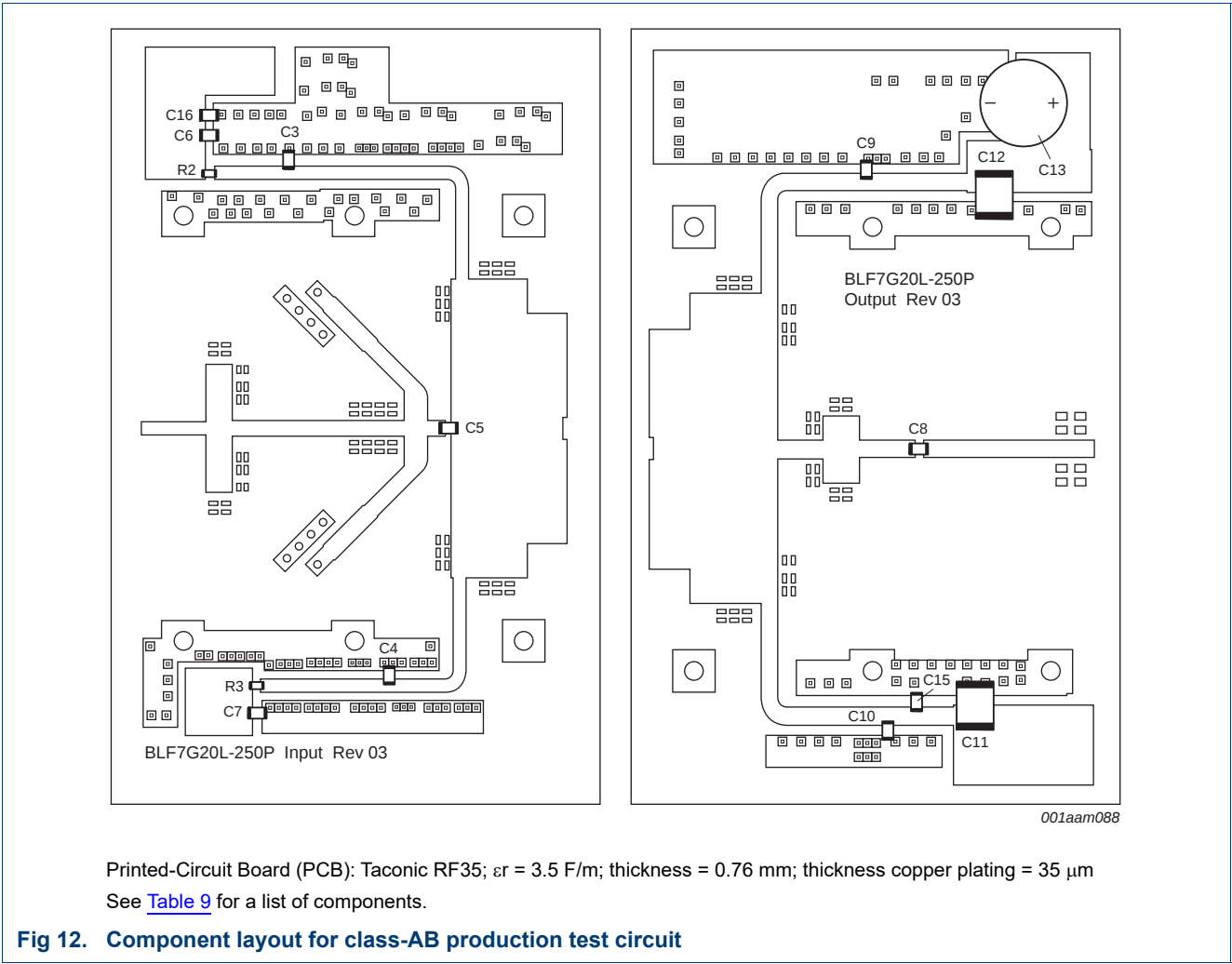
Fig 11. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values

7.6 Test circuit

Table 9. List of components
For test circuit see Figure 12.

Component	Description	Value	Code number	Type	Remarks
Base plate [1]					
C3, C4, C9, C10	multi layer ceramic chip capacitor	47 pF		ATC 800B	mount on edge
C5	multi layer ceramic chip capacitor	1.2 pF		ATC 800B	mount on edge
C6, C7	chip capacitor	560 pF		ATC 100A	
C8	multi layer ceramic chip capacitor	68 pF		ATC 800B	mount on edge
C11, C12	multi layer ceramic chip capacitor	10 µF		TDK	
C13	electrolytic capacitor	470 µF; 63 V			
C15, C16	multi layer ceramic chip capacitor	100 nF		Phillips 1206	
R2, R3	chip resistor	10 Ω		Philips 0603	

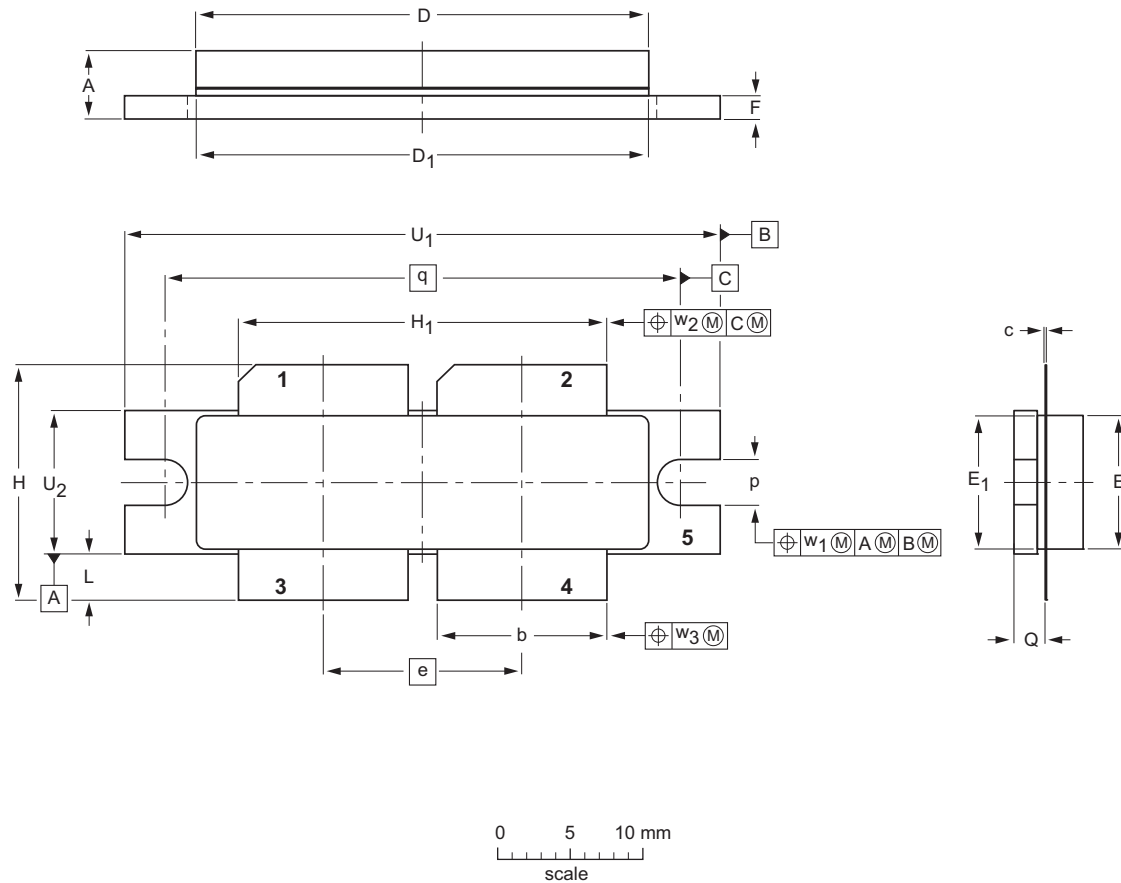
[1] See mechanical drawing (Figure 12).



8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note

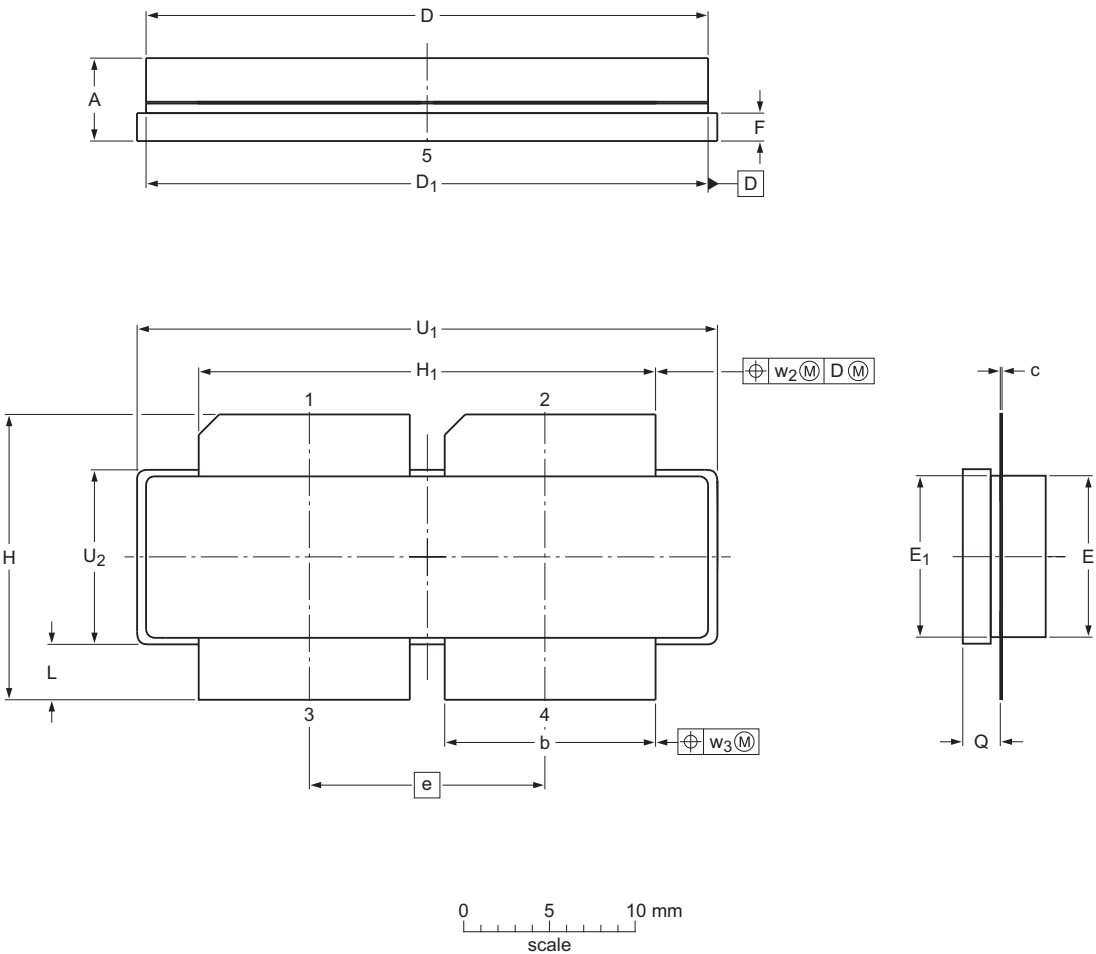
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						10-02-02 12-05-02

Fig 13. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	E	E ₁	e	F	H	H ₁	L	Q	U ₁	U ₂	w ₂	w ₃
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29	
	nom							13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03	
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405	
	nom							0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395	

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						12-05-02 13-05-24

Fig 14. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G20L-250P_7G20LS-250P#5	20150901	Product data sheet	-	BLF7G20L-250P_7G20LS-250P v.4
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.			
BLF7G20L-250P_7G20LS-250P v.4	20130712	Product data sheet	-	BLF7G20L-250P_7G20LS-250P v.3
BLF7G20L-250P_7G20LS-250P v.3	20110103	Product data sheet	-	BLF7G20L-250P_7G20LS-250P v.2
BLF7G20L-250P_7G20LS-250P v.2	20100909	Preliminary data sheet	-	BLF7G20L-250P_7G20LS-250P v.1
BLF7G20L-250P_7G20LS-250P v.1	20091216	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Test information	3
7.1	Ruggedness in class-AB operation	3
7.2	Impedance information	4
7.3	Single carrier W-CDMA	5
7.4	One tone CW	6
7.5	2-carrier WCDMA characteristics	7
7.6	Test circuit	8
8	Package outline	9
9	Handling information	11
10	Abbreviations	11
11	Revision history	12
12	Legal information	13
12.1	Data sheet status	13
12.2	Definitions	13
12.3	Disclaimers	13
12.4	Trademarks	14
13	Contact information	14
14	Contents	15

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