

32-Bit

Microcontroller

TC1784

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1.1 2014-05

Microcontrollers

Edition 2014-05

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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Microcontrollers

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1 Summary of Features

The **SAK-TC1784F-320F180EL / SAK-TC1784F-320F180EP** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
 - Superior real-time performance
 - Strong bit handling
 - Fully integrated DSP capabilities
 - Single precision Floating Point Unit (FPU)
 - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
 - 16 Kbyte Parameter Memory (PRAM)
 - 32 Kbyte Code Memory (CMEM)
 - 180 MHz operation at full temperature range
- Multiple on-chip memories
 - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
 - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
 - 128 Kbyte Data Memory (LDRAM)
 - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
 - 40 Kbyte Code Scratchpad Memory (SPRAM)
 - Data Cache: up to 4 Kbyte (DCACHE, configurable)
 - 8 Kbyte Overlay Memory (OVRAM)
 - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
 - 64-bit Local Memory Buses between CPU, Flash and Data Memory
 - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
 - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
 - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
 - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
 - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
 - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
 - One External Bus Interface (EBU) with 32-bit demultiplexed / 16-bit multiplexed external bus interface
 - Scalable external bus timing up to 75 MHz

Summary of Features

- One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
- One FlexRayTM module with 2 channels (E-Ray).
- One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
 - 2 independent kernels (ADC0 and ADC1)
 - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
 - channels with impedance control and overlaid with ADC1 inputs
 - Extreme fast conversion, 21 cycles of f_{FADC} clock
 - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 91 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1784ED)
 - multi-core debugging, real time tracing, and calibration
 - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

Summary of Features

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1784 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

This document describes the derivatives of the device. The [Table 1](#) enumerates these derivatives and summarizes the differences.

Table 1 TC1784 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1784F-320F180EL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
SAK-TC1784F-320F180EP	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

2 System Overview of the TC1784

The TC1784 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1784 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1784 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1784 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1784 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1784, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1784 ports are reserved for these peripheral units to communicate with the external world.

System Overview of the TC1784

2.1 TC1784 Block Diagram

Figure 1 shows the block diagram of the TC1784.

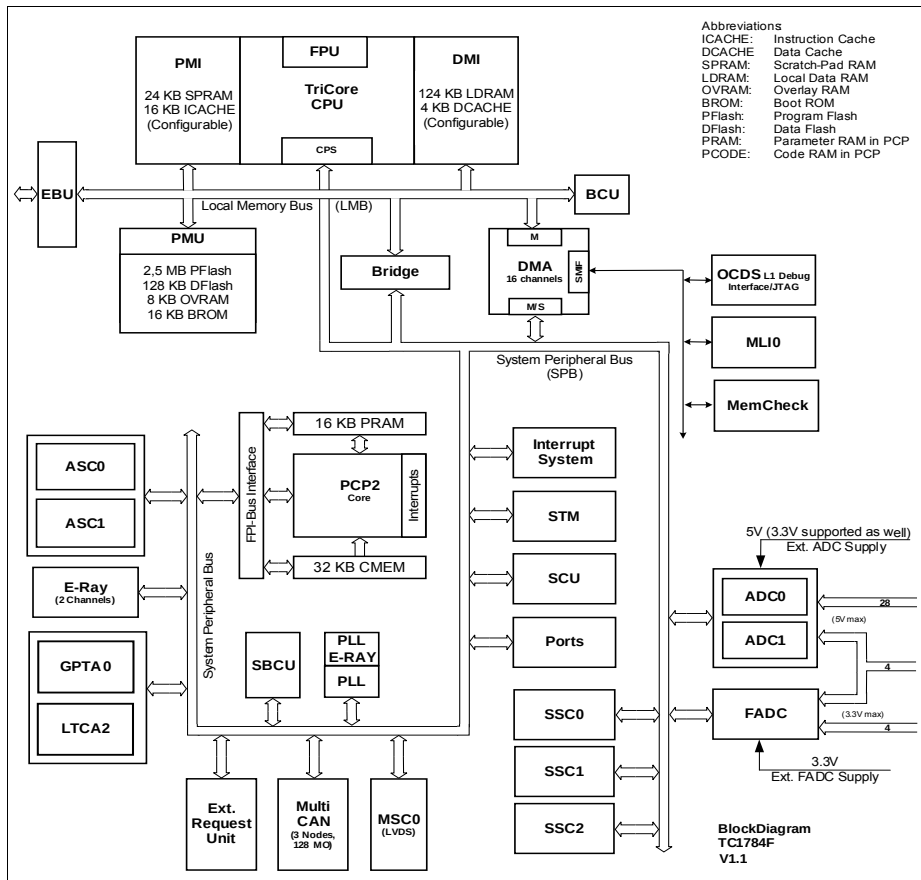


Figure 1 TC1784F Block Diagram

Figure 1 shows the block diagram of the SAK-TC1784F-320F180EL / SAK-TC1784F-320F180EP.

Pinning TC1784 Pin Configuration

3 Pinning

Figure 3-1 is showing the TC1784 Logic Symbol.

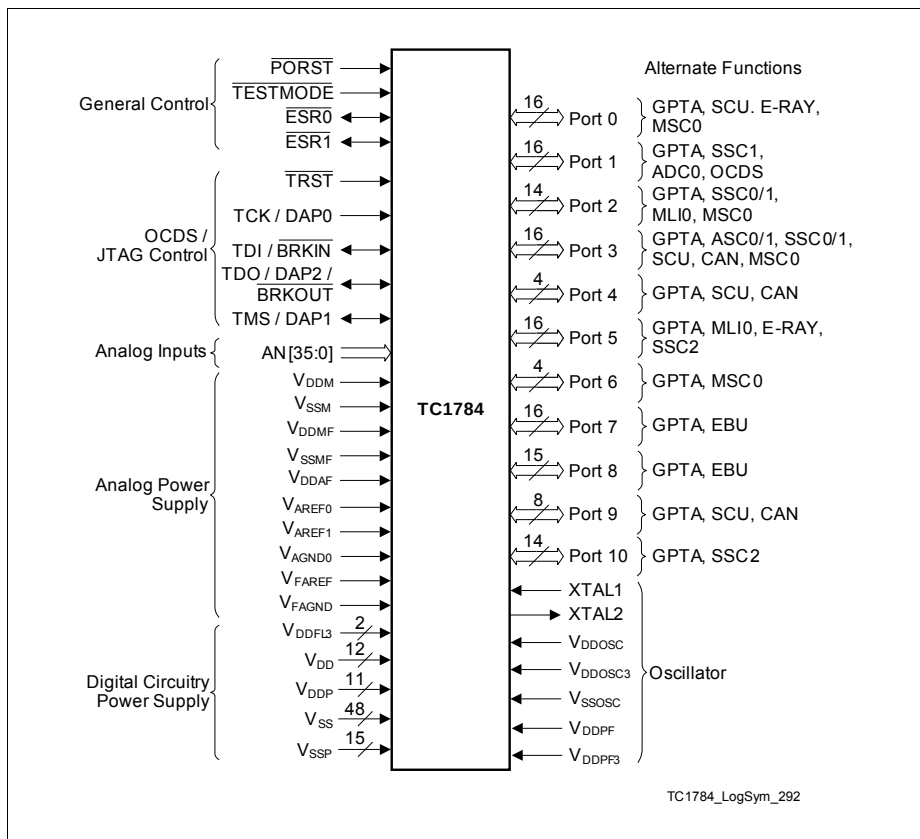


Figure 3-1 TC1784 Logic Symbol

3.1 TC1784 Pin Configuration

This chapter shows the pin configuration of package variant PG-LFBGA-292-6.

Pinning TC1784 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			
A	N.C.2	P10.9	P10.8	P10.6	P10.4	VSSP	P2.12	P2.11	P6.2	P6.0	VSSP	P0.12	P0.10	P0.8	P3.13	P3.15	P3.4	P3.2	P3.8	VSSP	A		
B	VDDP	VSSP	P10.7	P10.5	P10.3	VDDP	P0.15	P2.10	P6.3	P6.1	VDDP	P0.13	P0.11	P0.9	P3.12	P3.14	P3.7	P3.3	VSSP	VDDP	B		
C	P10.10	VDDP	Top-View																		VDDP	P3.6	C
D	P5.0	P10.11		VSSP	P10.2	P10.0	P0.14	P0.6	P2.13	P2.9	P0.2	P0.1	VDDFL3	VDDFL3	P3.0	P3.1	VSSP			P3.5	ESR0	D	
E	P5.5	P5.1		P10.12	VSSP	P10.1	P0.7	P0.5	P0.4	P2.8	P0.3	P0.0	P3.11	P3.9	P3.10	VSSP	P1.1			ESR1	PORST	E	
F	P5.6	P5.7		P5.2	P10.13											P1.15	P1.0		TEST MODE	TCK	F		
G	VSSP	VDDP		P9.0	P5.3			VDD	VSS	VSS	VSS	VSS	VDD			P1.6	P1.7		TRST	TDO	G		
H	P5.15	P5.8		P9.1	P5.4		VDD		VSS	VSS	VSS	VSS		VDD		P1.5	TMS		TDI	VDDOSC3	H		
J	P5.10	P5.9		P9.3	P9.2		VSS	VSS		VSS	VSS		VSS	VSS		P1.4	VDDPF3		XTAL2	XTAL1	J		
K	P5.12	P5.11		P9.4	P9.5		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		P1.3	VDDPF		VDDOSC	VSSOSC	K		
L	P5.14	P5.13		P9.6	P9.7		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		P1.10	P1.8		P1.9	P1.11	L		
M	VSSP	VDDP		N.C.3	N.C.4		VSS	VSS		VSS	VSS		VSS	VSS		P1.2	P8.14		VDDP	VSSP	M		
N	VDDMF	VDDAF		VFAREF	VFAGND		VDD		VSS	VSS	VSS	VSS		VDD		P8.13	P8.12		P8.11	P8.4	N		
P	AN35	VSSAF VSSMF		AN34	AN33		VDD	VSS	VSS	VSS	VSS	VDD				P8.10	P8.9		P8.8	P8.7	P		
R	AN32	AN31		AN30	AN29											VDD	P7.2		P8.6	P8.5	R		
T	AN28	AN7		AN25	AN24	VAGND0	VAREF1	AN6	AN2	P1.12	P2.3	P2.7	P4.0	P7.4	P7.7	VSS	VDD		P8.2	P8.3	T		
U	AN27	AN26		AN21	AN15	VAREF0	AN8	AN3	P1.14	P1.13	P2.2	P2.6	P4.1	P7.3	P7.8	P7.0	VSS		P8.0	P8.1	U		
V	AN23	AN22														VDD					V		
W	AN20	AN14	AN16	AN18	AN17	AN19	VSSM	AN5	AN1	VDDP	P2.1	P2.5	P4.2	P7.6	P7.9	VDDP	P7.11	P7.13	VSS	VDD	W		
Y	N.C.1	AN13	AN12	AN11	AN10	AN9	VDDM	AN4	AN0	VSSP	P2.0	P2.4	P4.3	P7.1	P7.5	VSSP	P7.10	P7.12	P7.14	VSS	Y		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

Figure 3-2 TC1784 Pinning for PG-LFBGA-292-6 Package

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6)

Pin	Symbol	Ctrl.	Type	Function
Port 0				
E12	P0.0	I/O0	A1/ PU	Port 0 General Purpose I/O Line 0
	IN0	I		GPTA0 Input 0
	IN0	I		LTCA2 Input 0
	HWCFG0	I		Hardware Configuration Input 0
	OUT0	O1		GPTA0 Output 0
	OUT56	O2		GPTA0 Output 56
	OUT0	O3		LTCA2 Output 0
D12	P0.1	I/O0	A1/ PU	Port 0 General Purpose I/O Line 1
	IN1	I		GPTA0 Input 1
	IN1	I		LTCA2 Input 1
	SDI1	I		MSC0 Serial Data Input 1
	HWCFG1	I		Hardware Configuration Input 1
	OUT1	O1		GPTA0 Output 1
	OUT57	O2		GPTA0 Output 57
	OUT1	O3		LTCA2 Output 1
D11	P0.2	I/O0	A1/ PU	Port 0 General Purpose I/O Line 2
	IN2	I		GPTA0 Input 2
	IN2	I		LTCA2 Input 2
	HWCFG2	I		Hardware Configuration Input 2
	OUT2	O1		GPTA0 Output 2
	OUT58	O2		GPTA0 Output 58
	OUT2	O3		LTCA2 Output 2
E11	P0.3	I/O0	A1+/ PU	Port 0 General Purpose I/O Line 3
	IN3	I		GPTA0 Input 3
	IN3	I		LTCA2 Input 3
	HWCFG3	I		Hardware Configuration Input 3
	OUT3	O1		GPTA0 Output 3
	OUT59	O2		GPTA0 Output 59
	OUT3	O3		LTCA2 Output 3

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E9	P0.4	I/O0	A1/ PU	Port 0 General Purpose I/O Line 4
	IN4	I		GPTA0 Input 4
	IN4	I		LTCA2 Input 4
	HWCFG4	I		Hardware Configuration Input 4
	OUT4	O1		GPTA0 Output 4
	OUT60	O2		GPTA0 Output 60
	OUT4	O3		LTCA2 Output 4
E8	P0.5	I/O0	A1/ PU	Port 0 General Purpose I/O Line 5
	IN5	I		GPTA0 Input 5
	IN5	I		LTCA2 Input 5
	HWCFG5	I		Hardware Configuration Input 5
	OUT5	O1		GPTA0 Output 5
	OUT61	O2		GPTA0 Output 61
	OUT5	O3		LTCA2 Output 5
D8	P0.6	I/O0	A1/ PU	Port 0 General Purpose I/O Line 6
	IN6	I		GPTA0 Input 6
	IN6	I		LTCA2 Input 6
	HWCFG6	I		Hardware Configuration Input 6
	REQ2	I		External Request Input 2
	OUT6	O1		GPTA0 Output 6
	OUT62	O2		GPTA0 Output 62
	OUT6	O3		LTCA2 Output 6
E7	P0.7	I/O0	A1/ PU	Port 0 General Purpose I/O Line 7
	IN7	I		GPTA0 Input 7
	IN7	I		LTCA2 Input 7
	HWCFG7	I		Hardware Configuration Input 7
	REQ3	I		External Request Input 3
	OUT7	O1		GPTA0 Output 7
	OUT63	O2		GPTA0 Output 63
	OUT7	O3		LTCA2 Output 7

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A14	P0.8	I/O0	A1/ PU	Port 0 General Purpose I/O Line 8
	IN8	I		GPTA0 Input 8
	IN8	I		LTCA2 Input 8
	RXDA0	I		E-Ray Channel A Receive Data Input 0
	OUT8	O1		GPTA0 Output 8
	OUT64	O2		GPTA0 Output 64
	OUT8	O3		LTCA2 Output 8
B14	P0.9	I/O0	A1/ PU	Port 0 General Purpose I/O Line 9
	IN9	I		GPTA0 Input 9
	IN9	I		LTCA2 Input 9
	RXDB0	I		E-Ray Channel B Receive Data Input 0
	OUT9	O1		GPTA0 Output 9
	OUT65	O2		GPTA0 Output 65
	OUT9	O3		LTCA2 Output 9
A13	P0.10	I/O0	A2/ PU	Port 0 General Purpose I/O Line 10
	IN10	I		GPTA0 Input 10
	OUT10	O1		GPTA0 Output 10
	TXDA0	O2		E-Ray Channel A transmit Data Output
	OUT10	O3		LTCA2 Output 10
B13	P0.11	I/O0	A2/ PU	Port 0 General Purpose I/O Line 11
	IN11	I		GPTA0 Input 11
	OUT11	O1		GPTA0 Output 11
	TXDB0	O2		E-Ray Channel B transmit Data Output
	OUT11	O3		LTCA2 Output 11
A12	P0.12	I/O0	A2/ PU	Port 0 General Purpose I/O Line 12
	IN12	I		GPTA0 Input 12
	OUT12	O1		GPTA0 Output 12
	TXENA	O2		E-Ray Channel A transmit Data Output enable
	OUT12	O3		LTCA2 Output 12

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B12	P0.13	I/O0	A2/ PU	Port 0 General Purpose I/O Line 13
	IN13	I		GPTA0 Input 13
	OUT13	O1		GPTA0 Output 13
	TXENB	O2		E-Ray Channel B transmit Data Output enable
	OUT13	O3		LTCA2 Output 13
D7	P0.14	I/O0	A1+/ PU	Port 0 General Purpose I/O Line 14
	IN14	I		GPTA0 Input 14
	REQ4	I		External Request Input 4
	OUT14	O1		GPTA0 Output 14
	FCLP0C	O2		MSC0 Clock Output Positive C
	OUT14	O3		LTCA2 Output 14
B7	P0.15	I/O0	A1+/ PU	Port 0 General Purpose I/O Line 15
	IN15	I		GPTA0 Input 15
	REQ5	I		External Request Input 5
	OUT15	O1		GPTA0 Output 15
	SOP0C	O2		MSC0 Serial Data Output Positive C
	OUT15	O3		LTCA2 Output 15

Port 1

F17	P1.0	I/O0	A2/ PU	Port 1 General Purpose I/O Line 0
	IN16	I		GPTA0 Input 16
	BRKIN	I		Break Input
	OUT16	O1		GPTA0 Output 16
	OUT72	O2		GPTA0 Output 72
	OUT16	O3		LTCA2 Output 16
	BRKOUT	O		Break Output (controlled by OCDS module)
E17	P1.1	I/O0	A1/ PU	Port 1 General Purpose I/O Line 1
	IN17	I		GPTA0 Input 17
	OUT17	O1		GPTA0 Output 17
	OUT73	O2		GPTA0 Output 73
	OUT17	O3		LTCA2 Output 17

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M16	P1.2	I/O0	A1/ PU	Port 1 General Purpose I/O Line 2
	IN18	I		GPTA0 Input 18
	OUT18	O1		GPTA0 Output 18
	OUT74	O2		GPTA0 Output 74
	OUT18	O3		LTCA2 Output 18
K16	P1.3	I/O0	A1/ PU	Port 1 General Purpose I/O Line 3
	IN19	I		GPTA0 Input 19
	IN19	I		LTCA2 Input 19
	OUT19	O1		GPTA0 Output 19
	OUT75	O2		GPTA0 Output 75
	OUT19	O3		LTCA2 Output 19
J16	P1.4	I/O0	A1/ PU	Port 1 General Purpose I/O Line 4
	IN20	I		GPTA0 Input 20
	IN20	I		LTCA2 Input 20
	EMGSTOP	I		Emergency Stop Input
	OUT20	O1		GPTA0 Output 20
	OUT76	O2		GPTA0 Output 76
	OUT20	O3		LTCA2 Output 20
H16	P1.5	I/O0	A1/ PU	Port 1 General Purpose I/O Line 35
	IN21	I		GPTA0 Input 21
	IN21	I		LTCA2 Input 21
	OUT21	O1		GPTA0 Output 21
	OUT77	O2		GPTA0 Output 77
	OUT21	O3		LTCA2 Output 21
G16	P1.6	I/O0	A1/ PU	Port 1 General Purpose I/O Line 6
	IN22	I		GPTA0 Input 22
	IN22	I		LTCA2 Input 22
	OUT22	O1		GPTA0 Output 22
	OUT78	O2		GPTA0 Output 78
	OUT22	O3		LTCA2 Output 22

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G17	P1.7	I/O0	A1/ PU	Port 1 General Purpose I/O Line 7
	IN23	I		GPTA0 Input 23
	IN23	I		LTCA2 Input 23
	OUT23	O1		GPTA0 Output 23
	OUT79	O2		GPTA0 Output 79
	OUT23	O3		LTCA2 Output 23
L17	P1.8	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 8
	IN24	I		GPTA0 Input 24
	IN48	I		GPTA0 Input 48
	MTSR1B	I		SSC1 Slave Receive Input B (Slave Mode)
	OUT24	O1		GPTA0 Output 24
	OUT48	O2		GPTA0 Output 48
	MTSR1B	O3		SSC1 Master Transmit Output B (Master Mode)
L19	P1.9	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 9
	IN25	I		GPTA0 Input 25
	IN49	I		GPTA0 Input 49
	MRST1B	I		SSC1 Master Receive Input B (Master Mode)
	OUT25	O1		GPTA0 Output 25
	OUT49	O2		GPTA0 Output 49
	MRST1B	O3		SSC1 Slave Transmit Output B (Slave Mode)
L16	P1.10	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 10
	IN26	I		GPTA0 Input 26
	IN50	I		GPTA0 Input 50
	OUT26	O1		GPTA0 Output 26
	OUT50	O2		GPTA0 Output 50
	SLSO17	O3		SSC1 Slave Select Output 7

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L20	P1.11	I/O0	A1/ PU	Port 1 General Purpose I/O Line 11
	IN27	I		GPTA0 Input 27
	IN51	I		GPTA0 Input 51
	SCLK1B	I		SSC1 Clock Input B
	OUT27	O1		GPTA0 Output 27
	OUT51	O2		GPTA0 Output 51
	SCLK1B	O3		SSC1 Clock Output B
T10	P1.12	I/O0	A1/ PU	Port 1 General Purpose I/O Line 12
	IN16	I		LTCA2 Input 16
	AD0EMUX0	O1		ADC0 External Multiplexer Control Output 0
	AD0EMUX0	O2		ADC0 External Multiplexer Control Output 0
	OUT16	O3		LTCA2 Output 16
U10	P1.13	I/O0	A1/ PU	Port 1 General Purpose I/O Line 13
	IN17	I		LTCA2 Input 17
	AD0EMUX1	O1		ADC0 External Multiplexer Control Output 1
	AD0EMUX1	O2		ADC0 External Multiplexer Control Output 1
	OUT17	O3		LTCA2 Output 17
U9	P1.14	I/O0	A1/ PU	Port 1 General Purpose I/O Line 14
	IN18	I		LTCA2 Input 18
	AD0EMUX2	O1		ADC0 External Multiplexer Control Output 2
	AD0EMUX2	O2		ADC0 External Multiplexer Control Output 2
	OUT18	O3		LTCA2 Output 18
F16	P1.15	I/O0	A2/ PU	Port 1 General Purpose I/O Line 15
	BRKIN	I		OCDS Break Input
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BRKOUT	O		OCDS Break Output

Port 2

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Y11	P2.0	I/O0	A2/ PU	Port 2 General Purpose I/O Line 0
	IN32	I		GPTA0 Input 32
	OUT32	O1		GPTA0 Output 32
	TCLK0	O2		MLI0 Transmitter Clock Output 0
	OUT28	O3		LTCA2 Output 28
W11	P2.1	I/O0	A2/ PU	Port 2 General Purpose I/O Line 1
	IN33	I		GPTA0 Input 33
	TREADY0A	I		MLI0 Transmitter Ready Input A
	OUT33	O1		GPTA0 Output 33
	SLSO03	O2		SSC0 Slave Select Output Line 3
	SLSO13	O3		SSC1 Slave Select Output Line 3
U11	P2.2	I/O0	A2/ PU	Port 2 General Purpose I/O Line 2
	IN34	I		GPTA0 Input 34
	OUT34	O1		GPTA0 Output 34
	TVALID0	O2		MLI0 Transmitter Valid Output
	OUT29	O3		LTCA2 Output 29
T11	P2.3	I/O0	A2/ PU	Port 2 General Purpose I/O Line 3
	IN35	I		GPTA0 Input 35
	OUT35	O1		GPTA0 Output 35
	TDATA0	O2		MLI0 Transmitter Data Output
	OUT30	O3		LTCA2 Output 30
Y12	P2.4	I/O0	A2/ PU	Port 2 General Purpose I/O Line 4
	IN36	I		GPTA0 Input 36
	RCLK0A	I		MLI Receiver Clock Input A
	OUT36	O1		GPTA0 Output 36
	OUT36	O2		GPTA0 Output 36
	OUT31	O3		LTCA2 Output 31

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W12	P2.5	I/O0	A2/ PU	Port 2 General Purpose I/O Line 5
	IN37	I		GPTA0 Input 37
	OUT37	O1		GPTA0 Output 37
	RREADY0A	O2		MLI0 Receiver Ready Output A
	OUT110	O3		LTCA2 Output 110
U12	P2.6	I/O0	A2/ PU	Port 2 General Purpose I/O Line 6
	IN38	I		GPTA0 Input 38
	RVALID0A	I		MLI Receiver Valid Input A
	OUT38	O1		GPTA0 Output 38
	OUT38	O2		GPTA0 Output 38
	OUT111	O3		LTCA2 Output 111
T12	P2.7	I/O0	A2/ PU	Port 2 General Purpose I/O Line 7
	IN39	I		GPTA0 Input 39
	RDATA0A	I		MLI Receiver Data Input A
	OUT39	O1		GPTA0 Output 39
	OUT39	O2		GPTA0 Output 39
	Reserved	O3		-
E10	P2.8	I/O0	A2/ PU	Port 2 General Purpose I/O Line 8
	SLSO04	O1		SSC0 Slave Select Output 4
	SLSO14	O2		SSC1 Slave Select Output 4
	EN00	O3		MSC0 Enable Output 0
D10	P2.9	I/O0	A2/ PU	Port 2 General Purpose I/O Line 9
	SLSO05	O1		SSC0 Slave Select Output 5
	SLSO15	O2		SSC1 Slave Select Output 5
	EN01	O3		MSC0 Enable Output 1

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B8	P2.10	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 10
	MRST1A	I		SSC1 Master Receive Input A
	IN10	I		LTCA2 Input 10
	MRST1A	O1		SSC1 Slave Transmit Output
	OUT0	O2		LTCA2 Output 0
	Reserved	O3		-
A8	P2.11	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 11
	SCLK1A	I		SSC1 Clock Input A
	IN11	I		LTCA2 Input 11
	SCLK1A	O1		SSC1 Clock Output A
	OUT1	O2		LTCA2 Output 1
	FCLP0B	O3		MSC0 Clock Output Positive B
A7	P2.12	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 12
	MTSR1A	I		SSC1 Slave Receive Input A
	IN12	I		LTCA2 Input 12
	MTSR1A	O1		SSC1 Master Transmit Output A
	OUT2	O2		LTCA2 Output 2
	SOP0B	O3		MSC0 Serial Data Output Positive B
D9	P2.13	I/O0	A1/ PU	Port 2 General Purpose I/O Line 13
	SLSI11	I		SSC1 Slave Select Input 1
	SDI0	I		MSC0 Serial Data Input 0
	IN13	I		LTCA2 Input 13
	OUT3	O1		LTCA2 Output 3
	Reserved	O2		-
	Reserved	O3		-

Port 3

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
D15	P3.0	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 0
	RXD0A	I		ASC0 Receiver Input A (Async. & Sync. Mode)
	RXD0A	O1		ASC0 Clock Output (Sync. Mode)
	RXD0A	O2		ASC0 Clock Output (Sync. Mode)
	OUT84	O3		GPTA0 Output 84
D16	P3.1	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 1
	TXD0	O1		ASC0 Transmit
	TXD0	O2		ASC0 Transmit
	OUT85	O3		GPTA0 Output 85
A18	P3.2	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 2
	SCLK0	I		SSC0 Clock Input (Slave Mode)
	SCLK0	O1		SSC0 Clock Output (Master Mode)
	SCLK0	O2		SSC0 Clock Input (Master Mode)
	OUT86	O3		GPTA0 Output 86
B18	P3.3	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 3
	MRST0	I		SSC0 Master Receive Input (Master Mode)
	MRST0	O1		SSC0 Slave Transmit Output (Slave Mode)
	MRST0	O2		SSC0 Slave Transmit Output (Slave Mode)
	OUT87	O3		GPTA0 Output 87
A17	P3.4	I/O0	A2/ PU	Port 3 General Purpose I/O Line 4
	MTSR0	I		SSC0 Slave Receive Input (Slave Mode)
	MTSR0	O1		SSC0 Master Transmit Output (Master Mode)
	MTSR0	O2		SSC0 Master Transmit Output (Master Mode)
	OUT88	O3		GPTA0 Output 88
D19	P3.5	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 5
	SLSO00	O1		SSC0 Slave Select Output 0
	SLSO10	O2		SSC1 Slave Select Output 0
	SLSOANDO0	O3		SSC0 AND SSC1 Slave Select Output 0

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C20	P3.6	I/O0	A1+/PU	Port 3 General Purpose I/O Line 6
	SLSO01	O1		SSC0 Slave Select Output 1
	SLSO11	O2		SSC1 Slave Select Output 1
	SLSOANDO1	O3		SSC0 AND SSC1 Slave Select Output 1
B17	P3.7	I/O0	A2/PU	Port 3 General Purpose I/O Line 7
	SLSI0	I		SSC0 Slave Select Input 1
	SLSO02	O1		SSC0 Slave Select Output 2
	SLSO12	O2		SSC1 Slave Select Output 2
	OUT89	O3		GPTA0 Output 89
A19	P3.8	I/O0	A2/PU	Port 3 General Purpose I/O Line 8
	SLSO06	O1		SSC0 Slave Select Output 6
	TXD1	O2		ASC1 Transmit Output
	OUT90	O3		GPTA0 Output 90
E14	P3.9	I/O0	A1/PU	Port 3 General Purpose I/O Line 9
	RXD1A	I		ASC1 Receiver Input A
	RXD1A	O1		ASC1 Receiver Output A (Synchronous Mode)
	RXD1A	O2		ASC1 Receiver Output A (Synchronous Mode)
	OUT91	O3		GPTA0 Output 91
E15	P3.10	I/O0	A1/PU	Port 3 General Purpose I/O Line 10
	REQ0	I		External Request Input 0
	Reserved	O1		-
	Reserved	O2		-
	OUT92	O3		GPTA0 Output 92
E13	P3.11	I/O0	A1/PU	Port 3 General Purpose I/O Line 11
	REQ1	I		External Request Input 1
	Reserved	O1		-
	Reserved	O2		-
	OUT93	O3		GPTA0 Output 93

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B15	P3.12	I/O0	A1/ PU	Port 3 General Purpose I/O Line 12
	RXDCAN0	I		CAN Node 0 Receiver Input
	RXD0B	I		ASC0 Receiver Input B
	RXD0B	O1		ASC0 Receiver Output B (Synchronous Mode)
	RXD0B	O2		ASC0 Receiver Output B (Synchronous Mode)
	OUT94	O3		GPTA0 Output 94
A15	P3.13	I/O0	A2/ PU	Port 3 General Purpose I/O Line 13
	TXDCAN0	O1		CAN Node 0 Transmitter Output
	TXD0	O2		ASC0 Transmit Output
	OUT95	O3		GPTA0 Output 95
B16	P3.14	I/O0	A1/ PU	Port 3 General Purpose I/O Line 14
	RXDCAN1	I		CAN Node 1 Receiver Input
	RXD1B	I		ASC1 Receiver Input B
	SDI2	I		MSC0 Serial Data Input 2
	RXD1B	O1		ASC1 Receiver Output B (Synchronous Mode)
	RXD1B	O2		ASC1 Receiver Output B (Synchronous Mode)
	OUT96	O3		GPTA0 Output 96
A16	P3.15	I/O0	A2/ PU	Port 3 General Purpose I/O Line 15
	TXDCAN1	O1		CAN Node 1 Transmitter Output
	TXD1	O2		ASC1 Transmit Output
	OUT97	O3		GPTA0 Output 97

Port 4

T13	P4.0	I/O0	A1+/ PU	Port 4 General Purpose I/O Line 0
	IN28	I		GPTA0 Input 28
	IN52	I		GPTA0 Input 52
	RXDCAN2	I		CAN Node 2 Receiver Input
	OUT28	O1		GPTA0 Output 28
	OUT28	O1		GPTA0 Output 28
	OUT52	O2		GPTA0 Output 52

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U13	P4.1	I/O0	A1+/ PU	Port 4 General Purpose I/O Line 1
	IN29	I		GPTA0 Input 29
	IN53	I		GPTA0 Input 53
	OUT29	O1		GPTA0 Output 29
	OUT53	O2		GPTA0 Output 53
	TXDCAN2	O3		CAN Node 2 Transmitter Output
W13	P4.2	I/O0	A2/ PU	Port 4 General Purpose I/O Line 2
	IN30	I		GPTA0 Input 30
	IN54	I		GPTA0 Input 54
	OUT30	O1		GPTA0 Output 30
	OUT54	O2		GPTA0 Output 54
	EXTCLK1	O3		External Clock 1 Output
Y13	P4.3	I/O0	A2/ PU	Port 4 General Purpose I/O Line 3
	IN31	I		GPTA0 Input 31
	IN55	I		GPTA0 Input 55
	OUT31	O1		GPTA0 Output 31
	OUT55	O2		GPTA0 Output 55
	EXTCLK0	O3		External Clock 0 Output

Port 5

D1	P5.0	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 0
	IN40	I		GPTA0 Input 40
	IN26	I		LTCA2 Input 26
	OUT40	O1		GPTA0 Output 40
	OUT8	O2		LTCA2 Output 8
	SLSO20	O3		SSC2 Slave Select Output 0

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E2	P5.1	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 1
	IN41	I		GPTA0 Input 41
	IN27	I		LTCA2 Input 27
	OUT41	O1		GPTA0 Output 41
	OUT9	O2		LTCA2 Output 9
	SLSO21	O3		SSC2 Slave Select Output 1
F4	P5.2	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 2
	IN42	I		GPTA0 Input 42
	IN28	I		LTCA2 Input 28
	OUT42	O1		GPTA0 Output 42
	OUT10	O2		LTCA2 Output 10
	SLSO22	O3		SSC2 Slave Select Output 2
G5	P5.3	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 3
	IN43	I		GPTA0 Input 43
	OUT43	O1		GPTA0 Output 43
	OUT11	O2		LTCA2 Output 11
	SLSO23	O3		SSC2 Slave Select Output 3
H5	P5.4	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 4
	IN44	I		GPTA0 Input 44
	IN29	I		LTCA2 Input 29
	SLSI2A	I		SSC2 Slave Select Input A
	OUT44	O1		GPTA0 Output 44
	OUT12	O2		LTCA2 Output 12
	SLSO24	O3		SSC2 Slave Select Output 4

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E1	P5.5	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 5
	IN45	I		GPTA0 Input 45
	IN30	I		LTCA2 Input 30
	MRST2A	I		SSC2 Master Receive Input (Master Mode)
	OUT45	O1		GPTA0 Output 45
	OUT13	O2		LTCA2 Output 13
	MRST2	O3		SSC2 Slave Transmit Output (Slave Mode)
F1	P5.6	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 6
	IN46	I		GPTA0 Input 46
	IN31	I		LTCA2 Input 31
	MTSR2A	I		SSC2 Slave Receive Input (Slave Mode)
	OUT46	O1		GPTA0 Output 46
	OUT14	O2		LTCA2 Output 14
	MTSR2	O3		SSC2 Master Transmit Output (Master Mode)
F2	P5.7	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 7
	IN47	I		GPTA0 Input 47
	SCLK2A	I		SSC0 Clock Input (Slave Mode)
	OUT47	O1		GPTA0 Output 47
	OUT15	O2		LTCA2 Output 15
	SCLK2	O3		SSC0 Clock Output (Master Mode)
H2	P5.8	I/O0	A2/ PU	Port 5 General Purpose I/O Line 8
	RDATA0B	I		MLI0 Receiver Data Input B
	Reserved	O1		-
	TXDA1	O2		E-Ray Channel A transmit Data Output
	OUT89	O3		LTCA2 Output 89
J2	P5.9	I/O0	A2/ PU	Port 5 General Purpose I/O Line 9
	RVALID0B	I		MLI0 Receiver Data Valid Input B
	Reserved	O1		-
	TXDB1	O2		E-Ray Channel B transmit Data Output
	OUT90	O3		LTCA2 Output 90

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J1	P5.10	I/O0	A2/ PU	Port 5 General Purpose I/O Line 10
	RREADY0B	O1		MLI0 Receiver Ready Input B
	TXENA	O2		E-Ray Channel A transmit Data Output enable
	OUT91	O3		LTCA2 Output 91
K2	P5.11	I/O0	A2/ PU	Port 5 General Purpose I/O Line 11
	RCLK0B	I		MLI0 Receiver Clock Input B
	Reserved	O1		-
	TXENB	O2		E-Ray Channel B transmit Data Output enable
	OUT92	O3		LTCA2 Output 92
K1	P5.12	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 12
	TDATA0	O1		MLI0 Transmitter Data Output
	SLSO07	O2		SSC0 Slave Select Output 7
	OUT93	O3		LTCA2 Output 93
L2	P5.13	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 13
	TVALID0B	O1		MLI0 Transmitter Valid Input B
	SLSO16	O2		SSC1 Slave Select Output 6
	Reserved	O3		-
L1	P5.14	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 14
	TREADY0B	I		MLI0 Transmitter Ready Input B
	RXDA1	I		E-Ray Channel A Receive Data Input 1
	Reserved	O1		-
	Reserved	O2		-
	OUT94	O3		LTCA2 Output 94
H1	P5.15	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 15
	RXDB1	I		E-Ray Channel B Receive Data Input 1
	TCLK0	O1		MLI0 Transmitter Clock Output
	Reserved	O2		-
	OUT95	O3		LTCA2 Output 95

Port 6

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A10	P6.0	I/O0	F/ PU	Port 6 General Purpose I/O Line 0
	IN14	I		LTCA2 Input 14
	FCLN0	O1		MSC0 Clock Output Negative
	OUT80	O2		GPTA0 Output 80
	OUT4	O3		LTCA2 Output 4
B10	P6.1	I/O0	F/ PU	Port 6 General Purpose I/O Line 1
	IN15	I		LTCA2 Input 15
	FCLP0A	O1		MSC0 Clock Output Positive A
	OUT81	O2		GPTA0 Output 81
	OUT5	O3		LTCA2 Output 5
A9	P6.2	I/O0	F/ PU	Port 6 General Purpose I/O Line 2
	IN24	I		LTCA2 Input 24
	SON0	O1		MSC0 Serial Data Output Negative
	OUT82	O2		GPTA0 Output 82
	OUT6	O3		LTCA2 Output 6
B9	P6.3	I/O0	F/ PU	Port 6 General Purpose I/O Line 3
	IN25	I		LTCA2 Input 25
	SOP0A	O1		MSC0 Serial Data Output Positive A
	OUT83	O2		GPTA0 Output 83
	OUT7	O3		LTCA2 Output 7

Port 7

U16	P7.0	I/O0	A2/ PU	Port 7 General Purpose I/O Line 0
	AD0	I/O		EBU Address/Data Bus Line 0
	OUT32	O1		GPTA0 Output 32
	Reserved	O2		-
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Y14	P7.1	I/O0	A2/ PU	Port 7 General Purpose I/O Line 1
	AD1	I/O		EBU Address/Data Bus Line 1
	OUT33	O1		GPTA0 Output 33
	Reserved	O2		-
	Reserved	O3		-
R17	P7.2	I/O0	A2/ PU	Port 7 General Purpose I/O Line 2
	AD2	I/O		EBU Address/Data Bus Line 2
	OUT34	O1		GPTA0 Output 34
	Reserved	O2		-
	Reserved	O3		-
U14	P7.3	I/O0	A2/ PU	Port 7 General Purpose I/O Line 3
	AD3	I/O		EBU Address/Data Bus Line 3
	OUT35	O1		GPTA0 Output 35
	Reserved	O2		-
	Reserved	O3		-
T14	P7.4	I/O0	A2/ PU	Port 7 General Purpose I/O Line 4
	AD4	I/O		EBU Address/Data Bus Line 4
	OUT36	O1		GPTA0 Output 36
	Reserved	O2		-
	Reserved	O3		-
Y15	P7.5	I/O0	A2/ PU	Port 7 General Purpose I/O Line 5
	AD5	I/O		EBU Address/Data Bus Line 5
	OUT37	O1		GPTA0 Output 37
	Reserved	O2		-
	Reserved	O3		-
W14	P7.6	I/O0	A2/ PU	Port 7 General Purpose I/O Line 6
	AD6	I/O		EBU Address/Data Bus Line 6
	OUT38	O1		GPTA0 Output 38
	Reserved	O2		-
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T15	P7.7	I/O0	A2/ PU	Port 7 General Purpose I/O Line 7
	AD7	I/O		EBU Address/Data Bus Line 7
	OUT39	O1		GPTA0 Output 39
	Reserved	O2		-
	Reserved	O3		-
U15	P7.8	I/O0	A2/ PU	Port 7 General Purpose I/O Line 8
	AD8	I/O		EBU Address/Data Bus Line 8
	OUT40	O1		GPTA0 Output 40
	Reserved	O2		-
	Reserved	O3		-
W15	P7.9	I/O0	A2/ PU	Port 7 General Purpose I/O Line 9
	AD9	I/O		EBU Address/Data Bus Line 9
	OUT41	O1		GPTA0 Output 41
	Reserved	O2		-
	Reserved	O3		-
Y17	P7.10	I/O0	A2/ PU	Port 7 General Purpose I/O Line 10
	AD10	I/O		EBU Address/Data Bus Line 10
	OUT42	O1		GPTA0 Output 42
	Reserved	O2		-
	Reserved	O3		-
W17	P7.11	I/O0	A2/ PU	Port 7 General Purpose I/O Line 11
	AD11	I/O		EBU Address/Data Bus Line 11
	OUT43	O1		GPTA0 Output 43
	Reserved	O2		-
	Reserved	O3		-
Y18	P7.12	I/O0	A2/ PU	Port 7 General Purpose I/O Line 12
	AD12	I/O		EBU Address/Data Bus Line 12
	OUT44	O1		GPTA0 Output 44
	Reserved	O2		-
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W18	P7.13	I/O0	A2/ PU	Port 7 General Purpose I/O Line 13
	AD13	I/O		EBU Address/Data Bus Line 13
	OUT45	O1		GPTA0 Output 45
	Reserved	O2		-
	Reserved	O3		-
Y19	P7.14	I/O0	A2/ PU	Port 7 General Purpose I/O Line 14
	AD14	I/O		EBU Address/Data Bus Line 14
	OUT46	O1		GPTA0 Output 46
	Reserved	O2		-
	Reserved	O3		-
V20	P7.15	I/O0	A2/ PU	Port 7 General Purpose I/O Line 15
	AD15	I/O		EBU Address/Data Bus Line 15
	OUT47	O1		GPTA0 Output 47
	Reserved	O2		-
	Reserved	O3		-

Port 8

U19	P8.0	I/O0	A2/ PU	Port 8 General Purpose I/O Line 0
	Reserved	O1		-
	OUT48	O2		GPTA0 Output 48
	OUT95	O3		LTCA2 Output 95
	A16	O		EBU Address Bus Line Output 16
U20	P8.1	I/O0	A2/ PU	Port 8 General Purpose I/O Line 1
	Reserved	O1		-
	OUT49	O2		GPTA0 Output 49
	OUT96	O3		LTCA2 Output 96
	A17	O		EBU Address Bus Line Output 17

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T19	P8.2	I/O0	A2/ PU	Port 8 General Purpose I/O Line 2
	Reserved	O1		-
	OUT50	O2		GPTA0 Output 50
	OUT97	O3		LTCA2 Output 97
	A18	O		EBU Address Bus Line Output 18
T20	P8.3	I/O0	A2/ PU	Port 8 General Purpose I/O Line 3
	Reserved	O1		-
	OUT51	O2		GPTA0 Output 51
	OUT98	O3		LTCA2 Output 98
	A19	O		EBU Address Bus Line Output 19
N20	P8.4	I/O0	A2/ PU	Port 8 General Purpose I/O Line 4
	Reserved	O1		-
	OUT52	O2		GPTA0 Output 52
	OUT99	O3		LTCA2 Output 99
	A20	O		EBU Address Bus Line Output 20
R20	P8.5	I/O0	A2/ PU	Port 8 General Purpose I/O Line 5
	Reserved	O1		-
	OUT53	O2		GPTA0 Output 53
	OUT100	O3		LTCA2 Output 100
	CS0	O		EBU Chip Select Output 0
R19	P8.6	I/O0	A2/ PU	Port 8 General Purpose I/O Line 6
	Reserved	O1		-
	OUT54	O2		GPTA0 Output 54
	OUT101	O3		LTCA2 Output 101
	CS1	O		EBU Chip Select Output 1
P20	P8.7	I/O0	A2/ PU	Port 8 General Purpose I/O Line 7
	Reserved	O1		-
	OUT55	O2		GPTA0 Output 55
	OUT102	O3		LTCA2 Output 102
	CS2	O		EBU Chip Select Output 2

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
P19	P8.8	I/O0	A2/ PU	Port 8 General Purpose I/O Line 8
	Reserved	O1		-
	OUT56	O2		GPTA0 Output 56
	OUT103	O3		LTCA2 Output 103
	$\overline{\text{CS3}}$	O		EBU Chip Select Output 3
P17	P8.9	I/O0	A2/ PU	Port 8 General Purpose I/O Line 9
	Reserved	O1		-
	OUT57	O2		GPTA0 Output 57
	OUT104	O3		LTCA2 Output 104
	$\overline{\text{BC0}}$	O		EBU Byte Control Line Output 0
P16	P8.10	I/O0	A2/ PU	Port 8 General Purpose I/O Line 10
	Reserved	O1		-
	OUT58	O2		GPTA0 Output 58
	OUT105	O3		LTCA2 Output 105
	$\overline{\text{BC1}}$	O		EBU Byte Control Line Output 1
N19	P8.11	I/O0	A2/ PU	Port 8 General Purpose I/O Line 11
	Reserved	O1		-
	OUT59	O2		GPTA0 Output 59
	OUT106	O3		LTCA2 Output 106
	$\overline{\text{RD}}$	O		EBU Read Control Line
N17	P8.12	I/O0	A2/ PU	Port 8 General Purpose I/O Line 12
	Reserved	O1		-
	OUT60	O2		GPTA0 Output 60
	OUT107	O3		LTCA2 Output 107
	$\overline{\text{RD}}/\overline{\text{WR}}$	O		EBU Write Control Line
N16	P8.13	I/O0	A2/ PU	Port 8 General Purpose I/O Line 13
	Reserved	O1		-
	OUT61	O2		GPTA0 Output 61
	OUT108	O3		LTCA2 Output 108
	ADV	O		EBU Address Valid Line

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M17	P8.14	I/O0	A1/ PU	Port 8 General Purpose I/O Line 14
	WAIT	I		EBU Wait Line
	Reserved	O1		-
	OUT62	O2		GPTA0 Output 62
	OUT109	O3		LTCA2 Output 109
Port 9				
G4	P9.0	I/O0	A1/ PU	Port 9 General Purpose I/O Line 0
	RXDCAN2	I		CAN Node 2 Receiver Input
	Reserved	O1		-
	OUT80	O2		GPTA0 Output 80
	OUT80	O3		LTCA2 Output 80
H4	P9.1	I/O0	A2/ PU	Port 9 General Purpose I/O Line 1
	Reserved	I		-
	TXDCAN2	O1		CAN Node 2 Transmitter Output
	OUT81	O2		GPTA0 Output 81
	OUT81	O3		LTCA2 Output 81
J5	P9.2	I/O0	A1/ PU	Port 9 General Purpose I/O Line 2
	Reserved	I		-
	Reserved	O1		-
	OUT82	O2		GPTA0 Output 82
	OUT82	O3		LTCA2 Output 82
J4	P9.3	I/O0	A1/ PU	Port 9 General Purpose I/O Line 3
	Reserved	I		-
	Reserved	O1		-
	OUT83	O2		GPTA0 Output 83
	OUT83	O3		LTCA2 Output 83

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K4	P9.4	I/O0	A1/ PU	Port 9 General Purpose I/O Line 4
	Reserved	I		-
	Reserved	O1		-
	OUT84	O2		GPTA0 Output 84
	OUT84	O3		LTCA2 Output 84
K5	P9.5	I/O0	A1/ PU	Port 9 General Purpose I/O Line 5
	Reserved	I		-
	Reserved	O1		-
	OUT85	O2		GPTA0 Output 85
	OUT85	O3		LTCA2 Output 85
L4	P9.6	I/O0	A1/ PU	Port 9 General Purpose I/O Line 6
	Reserved	I		-
	Reserved	O1		-
	OUT86	O2		GPTA0 Output 86
	OUT86	O3		LTCA2 Output 86
L5	P9.7	I/O0	A1/ PU	Port 9 General Purpose I/O Line 7
	Reserved	I		-
	Reserved	O1		-
	OUT87	O2		GPTA0 Output 87
	OUT87	O3		LTCA2 Output 87

Port 10

D6	P10.0	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 0
	MRST2B	I		SSC2 Master Receive Input (Master Mode)
	MRST2	O1		SSC2 Master Transmit Input (Slave Mode)
	EVT00	O2		MCDS Event Output 0
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E6	P10.1	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 1
	Reserved	I		-
	MTSR2	O1		SSC0 Slave Receive Input (Slave Mode)
	EVT01	O2		MCDS Event Output 1
	Reserved	O3		-
D5	P10.2	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 2
	SCLK2B	I		SSC0 Clock Input (Slave Mode)
	SCLK2	O1		SSC0 Clock Output (Master Mode)
	EVT02	O2		MCDS Event Output 2
	Reserved	O3		-
B5	P10.3	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 3
	SLSI2B	I		SSC2 Slave Select Input B
	SLSO20	O1		SSC2 Slave Select Output 0
	EVT03	O2		MCDS Event Output 3
	Reserved	O3		LTCA2 Output 83
A5	P10.4	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 4
	Reserved	I		-
	SLSO21	O1		SSC2 Slave Select Output 1
	Reserved	O2		GPTA0 Output 84
	Reserved	O3		-
B4	P10.5	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 5
	Reserved	I		-
	SLSO22	O1		SSC2 Slave Select Output 0
	Reserved	O2		GPTA0 Output 85
	Reserved	O3		-
A4	P10.6	I/O0	A1+/ PU	Port 10 General Purpose I/O Line 6
	Reserved	I		-
	SLSO23	O1		SSC2 Slave Select Output 3
	SLSOAND03	O2		SSC0 AND SSC2 Slave Select Output 3
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B3	P10.7	I/O0	A1/ PU	Port 10 General Purpose I/O Line 7
	Reserved	I		-
	SLSO24	O1		SSC2 Slave Select Output 4
	SLSOAND04	O2		SSC1 AND SSC2 Slave Select Output 4
	Reserved	O3		-
A3	P10.8	I/O0	A1/ PU	Port 10 General Purpose I/O Line 8
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
A2	P10.9	I/O0	A1/ PU	Port 10 General Purpose I/O Line 9
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
C1	P10.10	I/O0	A1/ PU	Port 10 General Purpose I/O Line 10
	RXDCAN2	I		CAN Node 2 Receiver Input
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
D2	P10.11	I/O0	A1/ PU	Port 10 General Purpose I/O Line 11
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
E4	P10.12	I/O0	A1/ PU	Port 10 General Purpose I/O Line 12
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F5	P10.13	I/O0	A1/ PU	Port 10 General Purpose I/O Line 13
	Reserved	I		-
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

Analog Input Port

Y9	AN0	I	D	Analog Input 0
W9	AN1	I	D	Analog Input 1
T9	AN2	I	D	Analog Input 2
U8	AN3	I	D	Analog Input 3
Y8	AN4	I	D	Analog Input 4
W8	AN5	I	D	Analog Input 5
T8	AN6	I	D	Analog Input 6
T2	AN7	I	D	Analog Input 7
U7	AN8	I	D	Analog Input 8
Y6	AN9	I	D	Analog Input 9
Y5	AN10	I	D	Analog Input 10
Y4	AN11	I	D	Analog Input 11
Y3	AN12	I	D	Analog Input 12
Y2	AN13	I	D	Analog Input 13
W2	AN14	I	D	Analog Input 14
U5	AN15	I	D	Analog Input 15
W3	AN16	I	D	Analog Input 16
W5	AN17	I	D	Analog Input 17
W4	AN18	I	D	Analog Input 18
W6	AN19	I	D	Analog Input 19
W1	AN20	I	D	Analog Input 20
U4	AN21	I	D	Analog Input 21
V2	AN22	I	D	Analog Input 22
V1	AN23	I	D	Analog Input 23

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T5	AN24	I	D	Analog Input 24
T4	AN25	I	D	Analog Input 25
U2	AN26	I	D	Analog Input 26
U1	AN27	I	D	Analog Input 27
T1	AN28	I	D	Analog Input 28
R5	AN29	I	D	Analog Input 29
R4	AN30	I	D	Analog Input 30
R2	AN31	I	D	Analog Input 31
R1	AN32	I	D	Analog Input 32
P5	AN33	I	D	Analog Input 33
P4	AN34	I	D	Analog Input 34
P1	AN35	I	D	Analog Input 35
Y7	V_{DDM}	-	-	ADC Analog Part Power Supply (3.3V - 5V)
W7	V_{SSM}	-	-	ADC Analog Part Ground
U6	V_{AREF0}	-	-	ADC0 Reference Voltage
T7	V_{AREF1}	-	-	ADC1 Reference Voltage
T6	V_{AGND0}	-	-	ADC Reference Ground
N1	V_{DDMF}	-	-	FADC Analog Part Power Supply (3.3V)
N2	V_{DDAF}	-	-	FADC Analog Part Logic Power Supply (1.3V)
P2	V_{SSMF}	-	-	FADC Analog Part Ground
P2	V_{SSAF}	-	-	FADC Analog Part Ground
N4	V_{FAREF}	-	-	FADC Reference Voltage
N5	V_{FAGND}	-	-	FADC Reference Ground

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G8, G13, H7, H14, N7, N14, P8, P13, R16, T17, V19, W20	V_{DD}	-	-	Digital Core Power Supply (1.3V)
B1, B6, B11, B20, C2, C19, G2, M2, M19, W10, W16	V_{DDP}	-	-	Port Power Supply (3.3V)
M4, M5	$V_{DDE(SB)}$	-	-	Emulation Stand-by SRAM Power Supply (1.3V) (Emulation device only) <i>Note: This pin is N.C. in a productive device.</i>

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A6, A11, A20, B2, B19, D4, D17, E5, E16, G1, M1, M20, Y10, Y16	V_{SSP}	-	-	Digital Ground
G9, G10, G11, G12	V_{SS}	-	-	Digital Ground
H9, H10, H11, H12	V_{SS}	-	-	Digital Ground
J7, J8, J10, J11, J13, J14	V_{SS}	-	-	Digital Ground
K7, K8, K9, K10, K11, K12, K13, K14	V_{SS}	-	-	Digital Ground

Pinning TC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L7, L8, L9, L10, L11, L12, L13, L14	V_{SS}	-	-	Digital Ground
M7, M8, M10, M11, M13, M14	V_{SS}	-	-	Digital Ground
N9, N10, N11, N12	V_{SS}	-	-	Digital Ground (cont'd)
P9, P10, P11, P12	V_{SS}	-	-	Digital Ground (cont'd)
T16, U17, W19, Y20	V_{SS}	-	-	Digital Ground (cont'd)
K19	V_{DDOSC}	-	-	Main Oscillator and PLL Power Supply (1.3V)
H20	V_{DDOSC3}	-	-	Main Oscillator Power Supply (3.3V)
K17	V_{DDPF}	-	-	Flexray Oscillator and PLL Power Supply (1.3V)
J17	V_{DDPF3}	-	-	Flexray Oscillator Power Supply (3.3V)
K20	V_{SSOSC}	-	-	Main Oscillator and PLL Ground
D13, D14	V_{DDFL3}	-	-	Power Supply for Flash (3.3V)
J20	XTAL1	I		Oscillator/PLL/Clock Generator Input
J19	XTAL2	O		Oscillator/PLL/Clock Generator Output

PinningTC1784 Pin Configuration

Table 3-1 Pin Definitions and Functions (PG-LFBGA-292-6) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H19	TDI	I	A2/ PU	JTAG Serial Data Input
	BRKIN	I		OCDS Break Input (Alternate Input)
	BRKOUT	O		OCDS Break Output (Alternate Output)
H17	TMS	I	A2/ PD	JTAG State Machine Control Input
	DAP1	I/O		Device Access Port Line 1
G20	TDO	I/O	A2/ PU	JTAG Serial Data Output
	DAP2	I/O		Device Access Port Line 2
	BRKIN	I		OCDS Break Input (Alternate Input)
	BRKOUT	O		OCDS Break Output (Alternate Output)
G19	<u>TRST</u>	I	A1/ PD	JTAG Reset Input
F20	TCK	I	A1/ PD	JTAG Clock Input
	DAP0	I		Device Access Port Line 0
F19	<u>TESTMODE</u>	I	PU	Test Mode Select Input
E19	<u>ESR1</u>	I/O	A2/ PD	External System Request Reset Input 1
E20	<u>PORST</u>	I	PD	Power On Reset Input
D20	<u>ESR0</u>	I/O	A2	External System Request Reset Input 0 Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset.
A1, Y1	N.C.	-	-	Not connected. These pins are reserved for future extension and shall not be connected externally

Legend for Table 3-1

Column “Ctrl.”:

I = Input (for GPIO port lines with IOCR bit field selection PCx = 0XXX_B)

O = Output

O0 = Output with IOCR bit field selection PCx = 1X00_B

O1 = Output with IOCR bit field selection PCx = 1X01_B (ALT1)

O2 = Output with IOCR bit field selection PCx = 1X10_B (ALT2)

O3 = Output with IOCR bit field selection PCx = 1X11 (ALT3)

Column “Type”:

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A1 = Pad class A1 (LVTTL)

A1+ = Pad class A1+ (LVTTL)

A2 = Pad class A2 (LVTTL)

F = Pad class F (LVDS/CMOS)

D = Pad class D (ADC)

I = Pad class I (LVTTL)

PU = with pull-up device connected during reset ($\overline{\text{PORST}} = 0$)

PD = with pull-down device connected during reset ($\overline{\text{PORST}} = 0$)

TR = tri-state during reset ($\overline{\text{PORST}} = 0$)

4 Identification Registers

The Identification Registers uniquely identify the whole device.

Table 2 SAK-TC1784F-320F180EL Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 _H	F000 0408 _H	BA
CBS_JTAGID	1018 E083 _H	F000 0464 _H	BA
SCU_CHIPID	0500 9610 _H	F000 0640 _H	BA
SCU_MANID	0000 1820 _H	F000 0644 _H	BA
SCU_RTID	0000 0000 _H	F000 0648 _H	BA

Table 3 SAK-TC1784F-320F180EP Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 _H	F000 0408 _H	BA
CBS_JTAGID	1018 E083 _H	F000 0464 _H	BA
SCU_CHIPID	8500 9610 _H	F000 0640 _H	BA
SCU_MANID	0000 1820 _H	F000 0644 _H	BA
SCU_RTID	0000 0000 _H	F000 0648 _H	BA

5 Electrical Parameters

This specification provides all electrical parameters of the TC1784.

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1784 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column "Symbol":

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1784 and must be regarded for a system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1784 designed in.

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5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the [Section 5.2.1](#).

Table 4 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade ¹⁾	Load ¹⁾	Leakage 150°C ¹⁾	Termination
A	3.3 V	LVTTTL I/O, LVTTTL outputs	A1 (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	1 µA	Series termination recommended
			A2 (e.g. serial I/Os)	40 MHz	50 pF	3 µA	Series termination recommended
F	3.3 V	LVDS	–	50 MHz	–	–	Parallel termination, 100 Ω ± 10% ²⁾
		CMOS	–	6 MHz	50 pF	–	
D_E	5 V	ADC	–	–	–	–	
I	3.3 V	LVTTTL (input only)	–	–	–	–	

1) These values show typical application configurations for the pad. Complete and detailed pad parameters are available in the individual pad parameter table on the following pages.

2) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

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5.1.3 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Voltage at 1.3 V power supply pins with respect to V_{SS}	V_{DD}	SR	–	–	2.0	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP} SR		–	–	4.33	V	–
Voltage at 5 V power supply pins with respect to V_{SS}	V_{DDM}	SR	–	–	7.0	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.7	–	$V_{DDP} + 0.5$ or max. 4.33	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND0}	V_{AIN} V_{AREFX}	SR	-0.6	–	7.0	V	–
Voltage on any shared Class D analog input pin with respect to V_{SSAF} , if the FADC is switched through to the pin.	V_{AINF}	SR	-0.6	–	7.0	V	–
Input current on any pin during overload condition	I_{IN}		-10	–	+10	mA	–
Absolute maximum sum of all input circuit currents for one port group during overload condition ¹⁾	I_{IN}		-25	–	+25	mA	–
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}		-200	–	200	mA	–

1) The port groups are defined in [Table 10](#).

5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 6 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP} or V_{DDM})
 - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 6 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition except LVDS pins	I_{IN}	-5	–	+5	mA	–
Input current on LVDS pins	I_{INLVDS}	-3	–	+3	mA	–
Absolute sum of all input circuit currents for one port group during overload condition ¹⁾	I_{ING}	-20	–	+20	mA	–
Input current on analog pins	I_{INANA}	-3	–	+3	mA	–
Absolute sum of all analog input currents for analog inputs of a single ADC during overload condition	I_{INSAS}	-15	–	+15	mA	–
Absolute sum of all input circuit currents during overload condition	ΣI_{INS}	-100	–	100	mA	–

1) The port groups are defined in **Table 10**.

Note: FADC input pins count as analog pin as they are overlayed with an ADC pins.

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Table 7 PN-Junction Characterisitcs for positive Overload

Pad Type	$I_{IN} = 3 \text{ mA}$	$I_{IN} = 5 \text{ mA}$
A1 / A1+ / F	$U_{IN} = V_{DDP} + 0.6 \text{ V}$	$U_{IN} = V_{DDP} + 0.7 \text{ V}$
A2	$U_{IN} = V_{DDP} + 0.5 \text{ V}$	$U_{IN} = V_{DDP} + 0.6 \text{ V}$
LVDS	$U_{IN} = V_{DDP} + 0.7 \text{ V}$	-
D	$U_{IN} = V_{DDM} + 0.6 \text{ V}$	-

Table 8 PN-Junction Characterisitcs for negative Overload

Pad Type	$I_{IN} = -3 \text{ mA}$	$I_{IN} = -5 \text{ mA}$
A1 / A1+ / F	$U_{IN} = V_{SS} - 0.6 \text{ V}$	$U_{IN} = V_{SS} - 0.7 \text{ V}$
A2	$U_{IN} = V_{SS} - 0.5 \text{ V}$	$U_{IN} = V_{SS} - 0.6 \text{ V}$
LVDS	$U_{IN} = V_{SS} - 0.7 \text{ V}$	-
D	$U_{IN} = V_{SSM} - 0.6 \text{ V}$	-

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery without having any negative reliability impact on the operational life-time.

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5.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1784. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC1784 must be static regulated voltages which allow a typical voltage swing of $\pm 5\%$.

All parameters specified in the following tables ([Table 11](#) and following) refer to these operating conditions ([Table 9](#)), unless otherwise noticed in the Note / Test Condition column.

The [Extended Range Operating Conditions](#) did not increase area of validity of the parameters defined in table 9 and later.

Table 9 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, negative	K_{OVAN} CC	—	—	0.0001		$I_{OV} \leq 0$ mA; $I_{OV} \geq -2$ mA; analog pad= 5.0 V
Overload coupling factor for analog inputs, positive	K_{OVAP} CC	—	—	0.00001		$I_{OV} \leq 3$ mA; $I_{OV} \geq 0$ mA; analog pad= 5.0 V
CPU Frequency	f_{CPU} SR	—	—	180	MHz	
FPI bus frequency	f_{FPI} SR	—	—	90	MHz	
LMB frequency	f_{LMB} CC	—	—	180	MHz	
PCP Frequency	f_{PCP} SR	—	—	180	MHz	
Inactive device pin current	I_{ID} SR	-1	—	1	mA	All power supply voltages $V_{DDx} = 0$
Short circuit current of digital outputs ¹⁾	I_{SC} SR	-5	—	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} CC	—	—	100	mA	

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Table 9 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute sum of short circuit currents per pin group	ΣI_{SC_PG} CC	—	—	20	mA	
Ambient Temperature	T_A SR	-40	—	125	°C	
Junction temperature	T_J SR	-40	—	150	°C	
Core Supply Voltage	V_{DD} SR	1.235	1.3	1.365 ²⁾	V	
Flash supply voltage 3.3V	V_{DDFL3} SR	3.13	3.3	3.47 ⁴⁾	V	
ADC analog supply voltage	V_{DDM} SR	3.13	3.3	5.5 ³⁾	V	
Oscillator core supply voltage	V_{DDOSC} SR	1.235	1.3	1.365 ²⁾	V	
Oscillator 3.3V supply voltage	V_{DDOSC3} SR	3.05	3.3	3.47 ⁴⁾	V	
E-Ray PLL core supply voltage	V_{DDPF} SR	1.235	1.3	1.365 ²⁾	V	
E-Ray PLL 3.3V supply voltage	V_{DDPF3} SR	3.05	3.3	3.47 ⁴⁾	V	
Digital supply voltage for IO pads	V_{DDP} SR	3.13	3.3	3.47 ⁴⁾	V	
VDDP voltage to ensure defined pad states ⁵⁾	V_{DDPPA} CC	0.65	—	—	V	
Digital ground voltage	V_{SS} SR	0	—	—	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.235	1.3	1.365 ²⁾	V	
FADC / ADC analog supply voltage	V_{DDMF} SR	3.13	3.3	3.47 ⁴⁾	V	
Analog ground voltage for V_{DDMF}	V_{SSAF} SR	-0.1	0	0.1	V	

1) Applicable for digital outputs.

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- 2) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 μs and the cumulated sum of the pulses does not exceed 1 h.
- 3) Voltage overshoot to 6.5V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 μs and the cumulated sum of the pulses does not exceed 1 h.
- 4) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 μs and the cumulated sum of the pulses does not exceed 1 h.
- 5) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of V_{DDP} .

Extended Range Operating Conditions

The following extended operating conditions are defined:

- $1.3\text{V} + 5\% < V_{\text{DD}} / V_{\text{DDPF}} / V_{\text{DDOSC}} / V_{\text{DDAF}} < 1.3\text{V} + 7.5\%$ (overvoltage condition):
 - limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $1.3\text{V} + 7.5\% < V_{\text{DD}} / V_{\text{DDOSC}} / V_{\text{DDAF}} < 1.3\text{V} + 10\%$ (overvoltage condition):
 - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $V_{\text{DDP}} / V_{\text{DDOSC3}} / V_{\text{DDFL3}} / V_{\text{DDMF}} < 3.3\text{V} \pm 10\%$
 - $3.3\text{V} + 5\% < V_{\text{DDP}} / V_{\text{DDOSC3}} / V_{\text{DDFL3}} / V_{\text{DDMF}} < 3.3\text{V} + 10\%$ (overvoltage condition):
 - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
 - $3.3\text{V} - 10\% < V_{\text{DDP}} / V_{\text{DDOSC3}} / V_{\text{DDFL3}} / V_{\text{DDMF}} < 3.3\text{V} - 5\%$ (undervoltage condition):
 - reduces GPIO pads performance

Table 10 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P5.[7:2], P5.15
2	P5.[9:8]
3	P5.[11:10]
4	P5.[14:12]
5	P1.[14:12], P2.0
6	P2.[4:1]
7	P2.[7:5]
8	P4.[2:0]

Table 10 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
9	P4.3
10	P1.2, P1.8
11	P1.[10:9]
12	P1.3, P1.11
13	P1.[7:4]
14	P1.[1:0], P1.15
15	P3.[8:5], P3.[3:2]
16	P3.[1:0], P3.4, P3.[10:9], P3.[15:14]
17	P0.[1:0], P3.[13:11]
18	P0.[3:2], P0.[9:8]
19	P0.[11:10]
20	P6.[3:0]
21	P2.[13:8]
22	P0.[5:4], P0.[13:12]
23	P0.[7:6], P0.[15:14], P5.[1:0]

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5.2 DC Parameters

5.2.1 Input/Output Pins

Table 11 Standard_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	$T_A = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ MHz}$
Pull-down current	$ I_{PDL} $ CC	–	–	150	μA	$V_i \geq 0.6 \times V_{DDP}$ V
		10	–	–	μA	$V_i \geq 0.36 \times V_{DDP}$ V
Pull-Up current	$ I_{PUH} $ CC	10	–	–	μA	$V_i \leq 0.6 \times V_{DDP}$ V
		–	–	100	μA	$V_i \leq 0.36 \times V_{DDP}$ V
Spike filter always blocked pulse duration	t_{SF1} CC	–	–	10	ns	only PORST pin
Spike filter pass-through pulse duration	t_{SF2} CC	100	–	–	ns	only PORST pin

Table 12 Standard_Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1 pads ¹⁾	HYS_{A1} CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage Current Class A1	I_{OZA1} CC	-500	–	500	nA	$V_i \geq 0\text{ V}$; $V_i \leq V_{DDP}$ V
Ratio V_{il}/V_{ih} , A1 pads	V_{ILA1} / V_{IHA1} CC	0.6	–	–		
On-Resistance of the class A1 pad, weak driver	$R_{DS_{ONW}}$ CC	–	450	600	Ohm	$I_{OH} > -0.5\text{ mA}$; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5\text{ mA}$; N_MOS

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Table 12 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1 pad, medium driver	$R_{\text{DS(on)M}}$ CC	—	—	155	Ohm	$I_{\text{OH}} > -2 \text{ mA}$; P_MOS
		—	—	110	Ohm	$I_{\text{OL}} < 2 \text{ mA}$; N_MOS
Fall time, pad type A1	t_{FA1} CC	—	—	150	ns	$C_{\text{L}} = 20 \text{ pF}$; pin out driver= weak
		—	—	50	ns	$C_{\text{L}} = 50 \text{ pF}$; pin out driver= medium
		—	—	140	ns	$C_{\text{L}} = 150 \text{ pF}$; pin out driver= medium
		—	—	550	ns	$C_{\text{L}} = 150 \text{ pF}$; pin out driver= weak
		—	—	18000	ns	$C_{\text{L}} = 20000 \text{ pF}$; pin out driver= medium
		—	—	65000	ns	$C_{\text{L}} = 20000 \text{ pF}$; pin out driver= weak

Electrical ParametersDC Parameters

Table 12 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1	t_{RA1} CC	—	—	150	ns	$C_L = 20$ pF; pin out driver= weak
		—	—	50	ns	$C_L = 50$ pF; pin out driver= medium
		—	—	140	ns	$C_L = 150$ pF; pin out driver= medium
		—	—	550	ns	$C_L = 150$ pF; pin out driver= weak
		—	—	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		—	—	65000	ns	$C_L = 20000$ pF; pin out driver= weak
Input high voltage class A1 pads	V_{IHA1} SR	$0.6 \times V_{DDP}$	—	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage class A1 pads	V_{ILA1} SR	-0.3	—	$0.36 \times V_{DDP}$	V	

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Table 12 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1 pads	V_{OHA1} CC	$V_{DDP} - 0.4$	—	—	V	$I_{OH} \geq -1.4$ mA; pin out driver= medium
		2.4	—	—	V	$I_{OH} \geq -2$ mA; pin out driver= medium
		$V_{DDP} - 0.4$	—	—	V	$I_{OH} \geq -400$ μ A; pin out driver= weak
		2.4	—	—	V	$I_{OH} \geq -500$ μ A; pin out driver= weak
Output voltage low class A1 pads	V_{OLA1} CC	—	—	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= medium
		—	—	0.4	V	$I_{OL} \leq 500$ μ A; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 13 Standard_Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1+ pads ¹⁾	$H_{YSA1} + CC$	$0.1 \times V_{DDP}$	—	—	V	
Input Leakage Current Class A1+	I_{OZA1+} CC	-1000	—	1000	nA	
On-Resistance of the class A1+ pad, weak driver	R_{DSONW} CC	—	450	600	Ohm	$I_{OH} > -0.5$ mA; P_MOS
		—	210	340	Ohm	$I_{OL} < 0.5$ mA; N_MOS

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Table 13 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, medium driver	R_{DSONM} CC	—	—	155	Ohm	$I_{\text{OH}} > -2 \text{ mA}$; P_MOS
		—	—	110	Ohm	$I_{\text{OL}} < 2 \text{ mA}$; N_MOS
On-Resistance of the class A1+ pad, strong driver	$R_{\text{DSON1+}}$ CC	—	—	100	Ohm	$I_{\text{OH}} > -2 \text{ mA}$; P_MOS
		—	—	80	Ohm	$I_{\text{OL}} < 2 \text{ mA}$; N_MOS
Fall time, pad type A1+	$t_{\text{FA1+}}$ CC	—	—	150	ns	$C_{\text{L}} = 20 \text{ pF}$; pin out driver= weak
		—	—	28	ns	$C_{\text{L}} = 50 \text{ pF}$; edge= slow ; pin out driver= strong
		—	—	16	ns	$C_{\text{L}} = 50 \text{ pF}$; edge= soft ; pin out driver= strong
		—	—	50	ns	$C_{\text{L}} = 50 \text{ pF}$; pin out driver= medium
		—	—	140	ns	$C_{\text{L}} = 150 \text{ pF}$; pin out driver= medium
		—	—	550	ns	$C_{\text{L}} = 150 \text{ pF}$; pin out driver= weak
		—	—	18000	ns	$C_{\text{L}} = 20000 \text{ pF}$; pin out driver= medium
		—	—	65000	ns	$C_{\text{L}} = 20000 \text{ pF}$; pin out driver= weak

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Table 13 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	t_{RA1+} CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	28	ns	$C_L = 50$ pF; edge= slow ; pin out driver= strong
		–	–	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak
Input high voltage, Class A1+ pads	V_{IHA1+} SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage Class A1+ pads	V_{ILA1+} SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Ratio V_{il}/V_{ih} , A1+ pads	V_{ILA1+} / V_{IHA1+} CC	0.6	–	–		

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Table 13 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1+ pads	$V_{OHA1+CC}$	$V_{DDP} - 0.4$	—	—	V	$I_{OH} \geq -1.4$ mA; pin out driver= medium
		$V_{DDP} - 0.4$	—	—	V	$I_{OH} \geq -1.4$ mA; pin out driver= strong
		2.4	—	—	V	$I_{OH} \geq -2$ mA; pin out driver= medium
		2.4	—	—	V	$I_{OH} \geq -2$ mA; pin out driver= strong
		$V_{DDP} - 0.4$	—	—	V	$I_{OH} \geq -400$ μ A; pin out driver= weak
		2.4	—	—	V	$I_{OH} \geq -500$ μ A; pin out driver= weak
Output voltage low class A1+ pads	$V_{OLA1+CC}$	—	—	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= medium
		—	—	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= strong
		—	—	0.4	V	$I_{OL} \leq 500$ μ A; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

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Table 14 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads ¹⁾	H_{YSA2} CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP} / 2 - 1 \text{ V}$; $V_i > V_{DDP} / 2 + 1 \text{ V}$; $V_i \geq 0 \text{ V}$; $V_i \leq V_{DDP} \text{ V}$
		-3000	–	3000	nA	$V_i > V_{DDP} / 2 - 1 \text{ V}$; $V_i < V_{DDP} / 2 + 1 \text{ V}$
Ratio V_{il}/V_{ih} , A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	$I_{OH} > -0.5 \text{ mA}$; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5 \text{ mA}$; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	$I_{OH} > -2 \text{ mA}$; P_MOS
		–	–	110	Ohm	$I_{OL} < 2 \text{ mA}$; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	$I_{OH} > -2 \text{ mA}$; P_MOS
		–	–	22	Ohm	$I_{OL} < 2 \text{ mA}$; N_MOS

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Table 14 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, pad type A2	t_{FA2} CC	—	—	150	ns	$C_L = 20$ pF; pin out driver= weak
		—	—	7	ns	$C_L = 50$ pF; edge= medium ; pin out driver= strong
		—	—	10	ns	$C_L = 50$ pF; edge= medium-minus ; pin out driver= strong
		—	—	3.7	ns	$C_L = 50$ pF; edge= sharp ; pin out driver= strong
		—	—	5	ns	$C_L = 50$ pF; edge= sharp-minus ; pin out driver= strong
		—	—	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		—	—	50	ns	$C_L = 50$ pF; pin out driver= medium
		—	—	7.5	ns	$C_L = 100$ pF; edge= sharp ; pin out driver= strong
		—	—	140	ns	$C_L = 150$ pF; pin out driver= medium

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Table 14 **Standard_Pads Class_A2** (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	$C_L = 150 \text{ pF}$; pin out driver= weak
		–	–	18000	ns	$C_L = 20000 \text{ pF}$; pin out driver= medium
		–	–	65000	ns	$C_L = 20000 \text{ pF}$; pin out driver= weak

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Table 14 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A2	t_{RA2} CC	—	—	150	ns	$C_L = 20$ pF; pin out driver= weak
		—	—	7.0	ns	$C_L = 50$ pF; edge= medium ; pin out driver= strong
		—	—	10	ns	$C_L = 50$ pF; edge= medium-minus ; pin out driver= strong
		—	—	3.7	ns	$C_L = 50$ pF; edge= sharp ; pin out driver= strong
		—	—	5	ns	$C_L = 50$ pF; edge= sharp-minus ; pin out driver= strong
		—	—	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		—	—	50	ns	$C_L = 50$ pF; pin out driver= medium
		—	—	7.5	ns	$C_L = 100$ pF; edge= sharp ; pin out driver= strong
		—	—	140	ns	$C_L = 150$ pF; pin out driver= medium

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Table 14 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	$C_L = 150 \text{ pF}$; pin out driver= weak
		–	–	18000	ns	$C_L = 20000 \text{ pF}$; pin out driver= medium
		–	–	65000	ns	$C_L = 20000 \text{ pF}$; pin out driver= weak
Input high voltage, class A2 pads	V_{IHA2} SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage Class A2 pads	V_{ILA2} SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Output voltage high class A2 pads	V_{OHA2} CC	$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4 \text{ mA}$; pin out driver= medium
		$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4 \text{ mA}$; pin out driver= strong
		2.4	–	–	V	$I_{OH} \geq -2 \text{ mA}$; pin out driver= medium
		2.4	–	–	V	$I_{OH} \geq -2 \text{ mA}$; pin out driver= strong
		$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -400 \mu\text{A}$; pin out driver= weak
		2.4	–	–	V	$I_{OH} \geq -500 \mu\text{A}$; pin out driver= weak

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Table 14 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage low class A2 pads	V_{OLA2} CC	—	—	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= medium
		—	—	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= strong
		—	—	0.4	V	$I_{OL} \leq 500$ μ A; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 15 Standard_Pads Class_F

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis F ¹⁾	$HYSF$ CC	$0.05 \times V_{DDP}$	—	—	V	
Input Leakage Current Class F	I_{OZF} CC	-6000	—	6000	nA	$V_i < V_{DDP} / 2 - 1$ V; $V_i > V_{DDP} / 2 + 1$ V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	—	3000	nA	$V_i > V_{DDP} / 2 - 1$ V; $V_i < V_{DDP} / 2 + 1$ V
Ratio Vil/ Vih, F pads	V_{ILF} / V_{IHF} CC	0.6	—	—		
On-Resistance of the class F pad, medium driver	R_{DSONM} CC	—	—	170	Ohm	$I_{OH} > -2$ mA; P_MOS
		—	—	145	Ohm	$I_{OL} \leq 2$ mA; N_MOS
Fall time, pad type F, CMOS mode	t_{FF} CC	—	—	60	ns	$C_L = 50$ pF
Rise time, pad type F, CMOS mode	t_{RF} CC	—	—	60	ns	$C_L = 50$ pF

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Table 15 Standard_Pads Class_F (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage, pad class F, CMOS mode	V_{IHF} SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage, Class F pads, CMOS mode	V_{ILF} SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Output high voltage, class F pads, CMOS mode	V_{OHF} CC	$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4 \text{ mA}$
		2.4	–	–	V	$I_{OH} \geq -2 \text{ mA}$
Output low voltage, class F pads, CMOS mode	V_{OLF} CC	–	–	0.4	V	$I_{OL} \leq 2 \text{ mA}$

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 16 Standard_Pads Class_I

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis Class I ¹⁾	$HYSI$ CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage Current	I_{OZI} CC	-1000	–	1000	nA	
Ratio between low and high input threshold	V_{ILI} / V_{IHI} CC	0.6	–	–		
Input high voltage, class I pins	V_{IHI} SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage, Class I pads	V_{ILI} SR	-0.3	–	$0.36 \times V_{DDP}$	V	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

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Table 17 LVDS_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance, pad class F, LVDS mode	$R_{O\ CC}$	40	–	140	Ohm	
Fall time, pad type LVDS	$t_{FL\ CC}$	–	–	2	ns	termination 100 $\Omega \pm 1\%$; differential capacitance = 10 pF; input capacitance = 20 pF
Rise time, pad type LVDS	$t_{RL\ CC}$	–	–	2	ns	termination 100 $\Omega \pm 1\%$; differential capacitance = 10 pF; input capacitance = 20 pF
Pad set-up time	$t_{SET_LVDS\ CC}$	–	–	13	μs	termination 100 $\Omega \pm 1\%$
Output Differential Voltage	$V_{OD\ CC}$	150	–	400	mV	termination 100 $\Omega \pm 1\%$
Output voltage high, pad class F, LVDS mode	$V_{OH\ CC}$	–	–	1525	mV	termination 100 $\Omega \pm 1\%$
Output voltage low, pad class F, LVDS mode	$V_{OL\ CC}$	875	–	–	mV	termination 100 $\Omega \pm 1\%$
Output Offset Voltage	$V_{OS\ CC}$	1075	–	1325	mV	termination 100 $\Omega \pm 1\%$

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DDM} = 4.75 \text{ V}$ to 5.25 V .

Table 18 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs ¹⁾	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input ²⁾⁽³⁾	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs ²⁾	C_{AREFTO} T CC	–	20	40	pF	
Differential Non-Linearity Error ⁴⁾⁽⁵⁾⁽⁶⁾⁽⁷⁾	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit ^{8) 9)}
Gain Error ⁴⁾⁽⁵⁾⁽⁶⁾⁽⁷⁾	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit ^{8) 9)}
Integral Non-Linearity ⁴⁾⁽⁵⁾⁽⁶⁾⁽⁷⁾	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit ^{8) 9)}
Offset Error ⁴⁾⁽⁵⁾⁽⁶⁾⁽⁷⁾	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit ^{8) 9)}
Converter clock	f_{ADC} SC	4	–	90	MHz	$f_{ADC} = f_{FPI}$
Internal ADC clock	f_{ADCI} CC	1	–	18	MHz	
Charge consumption per conversion	Q_{CONV} CC	70	85 ¹⁰⁾	100	pC	charge needs to be provided via V_{AREFx}

Electrical ParametersDC Parameters

Table 18 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage at analog inputs ¹¹⁾	I_{OZ1} CC	-100	—	500	nA	$V_i \leq V_{DDM} V$; $V_i \geq 0.97 \times V_{DDM} V$; overlaid= No
		-100	—	600	nA	$V_i \geq 0.97 \times V_{DDM} V$; $V_i \leq V_{DDM} V$; overlaid= Yes
		-500	—	100	nA	$V_i \leq 0.03 \times V_{DDM} V$; $V_i \geq 0 V$; overlaid= No
		-600	—	100	nA	$V_i \leq 0.03 \times V_{DDM} V$; $V_i \geq 0 V$; overlaid= Yes
		-100	—	200	nA	$V_i > 0.03 \times V_{DDM} V$; $V_i < 0.97 \times V_{DDM} V$; overlaid= No
		-100	—	300	nA	$V_i < 0.97 \times V_{DDM} V$; $V_i > 0.03 \times V_{DDM} V$; overlaid= Yes
Input leakage current at Vref0	I_{OZ2} CC	-1	—	1	μA	$V_{AREF0} \leq V_{DDM} V$
Input leakage current at Vref1		-1	—	1	μA	$V_{AREF1} \leq V_{DDM} V$
Input leakage current at Vagnd0	I_{OZ3} CC	-2	—	2	μA	$V_{AGND0} \leq V_{DDM} V$
ON resistance of the transmission gates in the analog voltage path	R_{AIN} CC	—	900	1500	Ohm	

Electrical ParametersDC Parameters

Table 18 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	—	500	1000	Ohm	
Sample time	t_S CC	2	—	257	T_{ADCI}	
Calibration time after bit ADC_GLOBCFG.SUCAL is set	t_{CAL} CC	—	—	4352	cycle s	
Total Unadjusted Error ⁶⁾⁵⁾¹²⁾	TUE CC	-4	—	$4^{13)}$	LSB	ADC resolution= 12-bit
Analog reference ground ²⁾	V_{AGND0} SR	$V_{SSM} - 0.05$	—	$V_{AREFX} - 1$	V	
Analog input voltage	V_{AIN} SR	V_{AGND0}	—	V_{AREFX}	V	
Analog reference voltage ²⁾	V_{AREFX} SR	$V_{AGND0} + 1$	—	$V_{DDM} + 0.05^{14)}$ ¹⁵⁾	V	
Analog reference voltage range ⁶⁾⁵⁾¹²⁾	$V_{AREFX} - V_{AGND0}$ SR	$V_{DDM}/2$	—	$V_{DDM} + 0.05$	V	

1) The sampling capacity of the conversion C-network is pre-charged to $V_{AREFX}/2$ before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from $V_{AREFX}/2$.

2) Applies to AINx, when used as auxiliary reference input.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.

4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.

5) If a reduced analog reference voltage between 1V and $V_{DDM}/2$ is used, then there are additional decrease in the ADC speed and accuracy.

6) If the analog reference voltage range is below V_{DDM} but still in the defined range of $V_{DDM}/2$ and V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k ($k < 1$), TUE, DNL, INL, Gain, and Offset errors increase also by the factor $1/k$.

7) If the analog reference voltage is $> V_{DDM}$, then the ADC converter errors increase.

8) For 10-bit conversions the error value must be multiplied with a factor 0.25.

9) For 8-bit conversions the error value must be multiplied with a factor 0.0625.

10) For a conversion time of 1 μ s a rms value of 85 μ A result for I_{AREFX} .

Electrical ParametersDC Parameters

- 11) The leakage current definition is a continuous function, as shown in figure ADCx Analoge Input Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.
- 12) Measured without noise.
- 13) For 10-bit conversion the TUE is $\pm 2\text{LSB}$; for 8-bit conversion the TUE is $\pm 1\text{LSB}$
- 14) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).
- 15) If the reference voltage $V_{\text{AREF}x}$ increase or the V_{DDM} decrease, so that $V_{\text{AREF}} = (V_{\text{DDM}} + 0.05\text{V to } V_{\text{DDM}} + 0.07\text{V})$, then the accuracy of the ADC decrease by 4LSB12.

Table 19 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{\text{ADC}} + (4 + \text{STC} + n) \times T_{\text{ADCI}}$	μs	$n = 8, 10, 12$ for n - bit conversion $T_{\text{ADC}} = 1 / f_{\text{FPI}}$ $T_{\text{ADCI}} = 1 / f_{\text{ADCI}}$
Conversion time without post-calibration		$2 \times T_{\text{ADC}} + (2 + \text{STC} + n) \times T_{\text{ADCI}}$		

The power-up calibration of the ADC requires a maximum number of 4352 f_{ADCI} cycles.

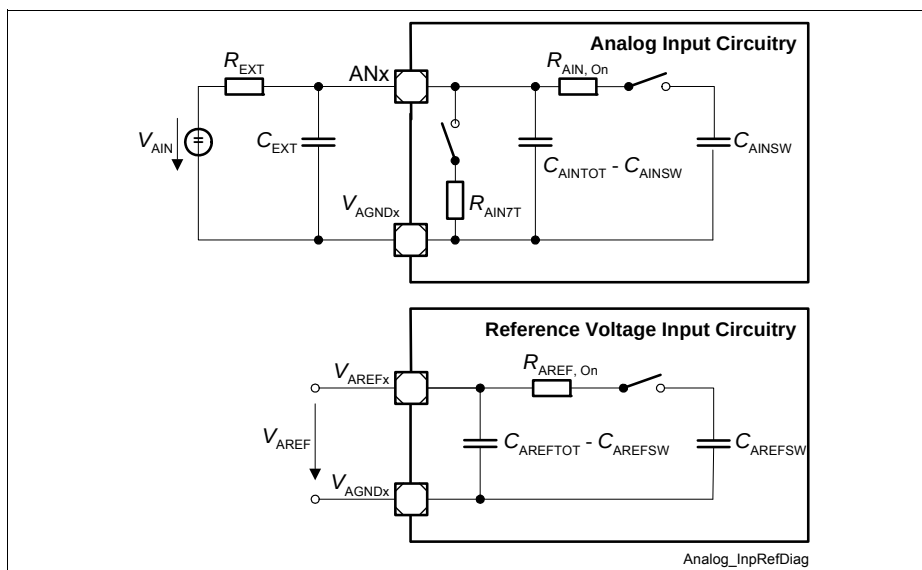


Figure 2 ADCx Input Circuits

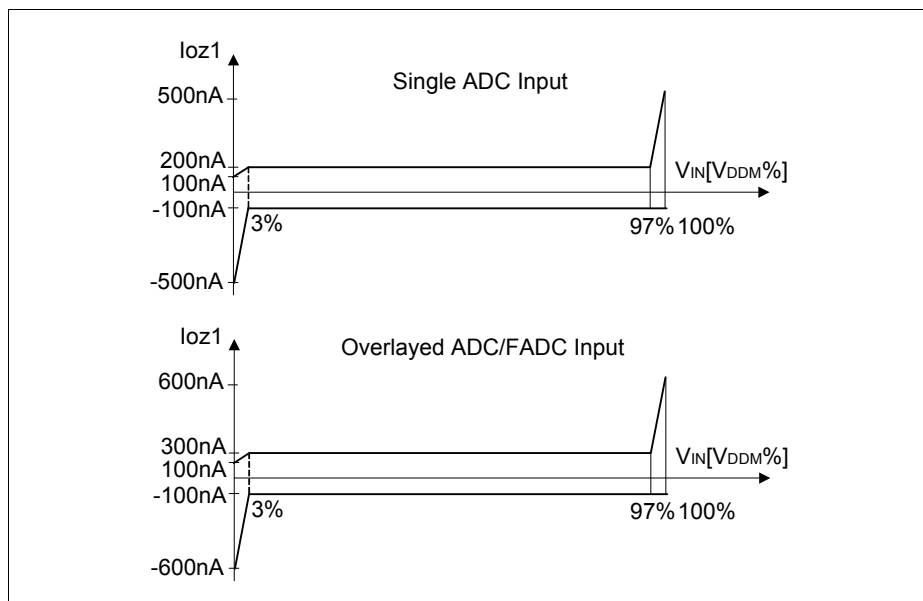


Figure 3 **ADCx Analog Inputs Leakage**

5.2.3 Fast Analog to Digital Converter (FADC)

Table 20 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at VFAREF	$I_{FAREF\ CC}$	–	–	120	μA	
Input leakage current at VFAREF ¹⁾	$I_{FOZ2\ CC}$	-500	–	500	nA	$V_{FAREF} \leq V_{DDMF}$ $V; V_{FAREF} \geq 0\ V$
Input leakage current at VFAGND	$I_{FOZ3\ CC}$	-500	–	500	nA	
DNL error	$EF_{DNL\ CC}$	-1	–	1	LSB	V_{IN} mode= differential; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= differential; Gain = 4 or 8 ²⁾
		-1	–	1	LSB	V_{IN} mode= single ended; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= single ended; Gain = 4 or 8 ²⁾
GRADient error	$EF_{GRAD\ CC}$	-5	–	5	%	V_{IN} mode= differential ; Gain ≤ 4
		-5	–	5	%	V_{IN} mode= single ended ; Gain ≤ 4
		-6	–	6	%	V_{IN} mode= differential ; Gain= 8
		-6	–	6	%	V_{IN} mode= single ended ; Gain= 8

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Table 20 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
INL error	EF_{INL} CC	-4	—	4	LSB	V_{IN} mode= differential
		-4	—	4	LSB	V_{IN} mode= single ended
Offset error	EF_{OFF} CC	-90	—	90	mV	V_{IN} mode= differential ; Calibration= No
		-90	—	90	mV	V_{IN} mode= single ended ; Calibration= No
		-20	—	20	mV	V_{IN} mode= differential ; Calibration= Yes ³⁾⁴⁾
		-20	—	20	mV	V_{IN} mode= single ended ; Calibration= Yes ³⁾⁴⁾
Error of common mode voltage $V_{\text{FAREF}}/2$	EF_{REF} CC	-60	—	60	mV	
Channel amplifier cutoff frequency	f_{COFF} CC	2	—	—	MHz	
Converter clock	f_{FADC} SC	1	—	90	MHz	$f_{\text{FADC}} = f_{\text{FPI}}$
Conversion time	t_{C} CC	—	—	21	1 / f_{FADC}	For 10-bit conversion
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN} CC	100	—	200	kOhm	
Settling time of a channel amplifier after changing ENN or ENP	t_{SET} CC	—	—	5	μs	
Analog input voltage range	V_{AINF} SR	V_{FAGND}	—	V_{DDMF}	V	

Electrical ParametersDC Parameters

Table 20 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference ground	V_{FAGND} SR	$V_{SSAF} - 0.05$	—	$V_{SSAF} + 0.05$	V	
Analog reference voltage	V_{FAREF} SR	3.0	—	3.63 ⁵⁾ 6)	V	

1) This value applies in power-down mode.

2) No missing codes.

3) Calibration should be performed at each power-up. In case of a continuous operation, it should be performed minimum once per week.

4) The offset error voltage drifts over the whole temperature range maximum $\pm 3\text{LSB}$.

5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 μs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

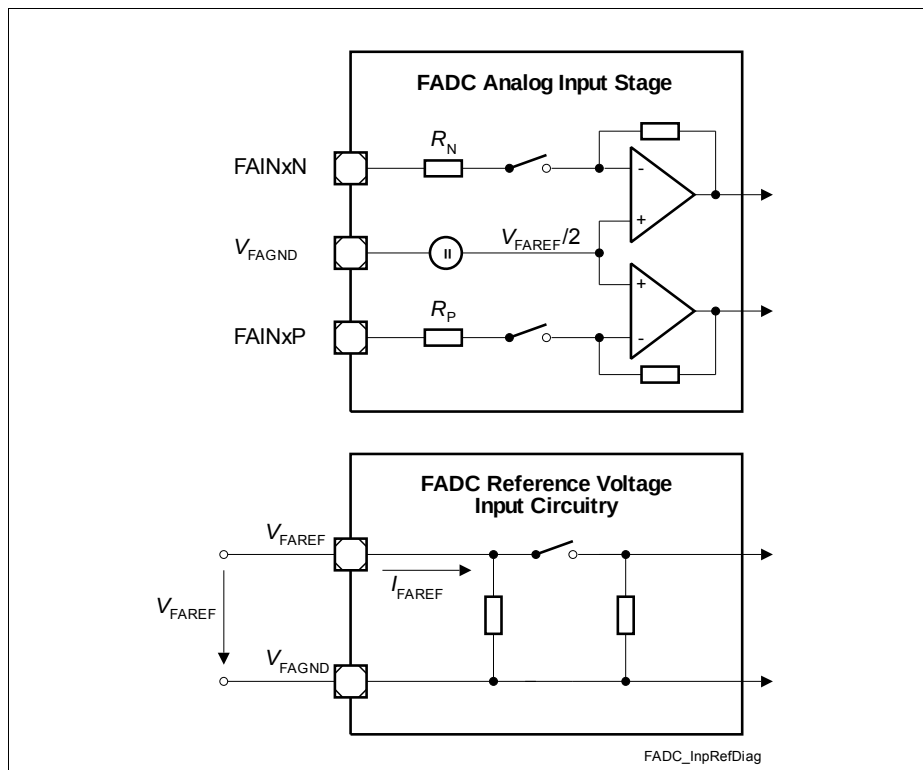


Figure 4 FADC Input Circuits

Electrical ParametersDC Parameters

5.2.4 Oscillator Pins

Table 21 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	—	25	μA	$V_{IN} < V_{DDOSC3}$; $V_{IN} > 0$ V
Input frequency	f_{OSC} SR	4	—	40	MHz	Direct Input Mode selected
		8	—	25	MHz	External Crystal Mode selected
Oscillator start-up time ¹⁾	t_{OSCS} CC	—	—	10	ms	
Input high voltage at XTAL1 ²⁾	V_{IHx} SR	$0.7 \times V_{DDOSC3}$	—	$V_{DDOSC3} + 0.5$	V	
Input low voltage at XTAL1	V_{ILx} SR	-0.5	—	$0.3 \times V_{DDOSC3}$	V	
Input Hysteresis for XTAL1 pad ³⁾	$HYSAX$ CC	—	—	200	mV	

1) t_{OSCS} is defined from the moment when $V_{DDOSC3} = 3.13$ V until the oscillations reach an amplitude at XTAL1 of $0.3 \times V_{DDOSC3}$. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of $0.4 \times V_{DDOSC3}$ is necessary.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

5.2.5 Temperature Sensor

Table 22 DTS Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	100	μs	
Temperature sensor range	T_{SR} SR	-40	–	150	°C	
Sensor Accuracy (calibrated)	T_{TSA} CC	-6	–	6	°C	
Start-up time after resets inactive	t_{TSST} SR	–	–	20	μs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(1)

$$T_j = \frac{DTSSTAT_{RESULT} - 596}{2,03}$$

5.2.6 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following two tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

$V_{DD}=1.365\text{ V}$, $V_{DDP}=3.47\text{ V}$, $V_{DDM}=5.1\text{ V}$, $f_{LMB}=180$, $T_J=150\text{ °C}$

The realistic power pattern defines the following conditions:

- $T_J=150\text{ °C}$
- $f_{LMB} = f_{PCP} = f_{CPU} = 180\text{ MHz}$
- $f_{FPI} = 90\text{ MHz}$
- $V_{DD} = V_{DDOSC} = V_{DDAF} = 1.326\text{ V}$
- $V_{DDP} = V_{DDOSC3} = V_{DDFL3} = V_{DDMF} = 3.366\text{ V}$
- $V_{DDM} = 5.1\text{ V}$

The max power pattern defines the following conditions:

- $T_J=150\text{ °C}$
- $f_{LMB} = f_{PCP} = f_{CPU} = 180\text{ MHz}$
- $f_{FPI} = 90\text{ MHz}$
- $V_{DD} = V_{DDOSC} = V_{DDAF} = 1.365\text{ V}$
- $V_{DDP} = V_{DDOSC3} = V_{DDFL3} = V_{DDMF} = 3.47\text{ V}$
- $V_{DDM} = 5.5\text{ V}$

Table 23 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Core active mode supply current ¹⁾²⁾	$I_{DD\text{ CC}}$	–	–	585 ³⁾	mA	power pattern= max
		–	–	433 ⁴⁾	mA	power pattern= realistic
I_{DD} current at PORST Low	$I_{DD_PORS\text{ T CC}}$	–	–	300	mA	
		–	–	291	mA	$V_{DD}=1.326\text{ V}$
Analog core supply current	$I_{DDAF\text{ CC}}$	–	–	23	mA	
Oscillator core supply current	$I_{DDOSC\text{ CC}}$	–	–	2	mA	
E-Ray PLL core supply current	$I_{DDPF\text{ CC}}$	–	–	2	mA	

Electrical ParametersDC Parameters

Table 23 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP} current at PORST Low	$I_{DDP_POR_ST}$ CC	–	–	2.5	mA	
I_{DDP} current no pad activity, LVDS off ⁵⁾	I_{DDP} CC	–	–	$I_{DDP_P_ORST}^{+12}$	mA	including flash read current
		–	–	$I_{DDP_P_ORST}^{+27}$	mA	including flash programming current ⁶⁾
		–	–	$I_{DDP_P_ORST}^{+20}{}^{7)}$	mA	including flash erase current ⁶⁾
Flash memory current ⁵⁾	I_{DDFL3} CC	–	–	56	mA	flash read current
		–	–	21	mA	flash programming current ⁶⁾
		–	–	56	mA	flash erase current ⁶⁾
Oscillator power supply current, 3.3V	I_{DDOSC3} CC	–	–	11.5	mA	
E-Ray PLL supply current, 3.3V	I_{DDPF3} CC	–	–	3.5	mA	
FADC analog supply current, 3.3V	I_{DDMF} CC	–	–	15	mA	
Current Consumption of LVDS Pad Pairs	I_{LVDS} CC	–	–	24	mA	for all LVDS pads in total
ADC 5V power supply current	I_{DDM} CC	–	–	2	mA	
Maximum power dissipation	PD CC	–	–	1277	mW	power pattern= max
		–	–	1042	mW	power pattern= realistic

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.

2) This current includes the E-Ray module power consumption, including the PCP operation component.

Electrical ParametersDC Parameters

- 3) The I_{DD} decreases typically by 79mA if the f_{CPU} decreases by 50MHz, at constant T_J
- 4) The I_{DD} decreases typically by 38mA if the f_{CPU} decreases by 50MHz, at constant T_J
- 5) For operations including the D-Flash the required currents are always lower than the currents for non D-Flash operation.
- 6) Relevant for the power supply dimensioning, not for thermal considerations.
- 7) In case of erase of Program Flash PF, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.

5.2.6.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(2)

$$I_0 = 2,20897 \left[\frac{\text{mA}}{\text{C}} \right] \times e^{0,02696 \times T_J[\text{C}]}$$

(3)

$$I_0 = 10,68 \left[\frac{\text{mA}}{\text{C}} \right] \times e^{0,02203 \times T_J[\text{C}]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for $V_{DD} = 1.326 \text{ V}$.

For the dynamic current consumption using the application pattern and $f_{LMB} = 2 * f_{FPI}$ the function 4 applies:

(4)

$$I_{Dym} = 0,77 \left[\frac{\text{mA}}{\text{MHz}} \right] \times f_{CPU}[\text{MHz}]$$

and this finally results in

(5)

$$I_{DD} = I_0 + I_{DYM}$$

5.3 AC Parameters

That means, keeping the pads constantly at maximum strength.

5.3.1 Testing Waveforms

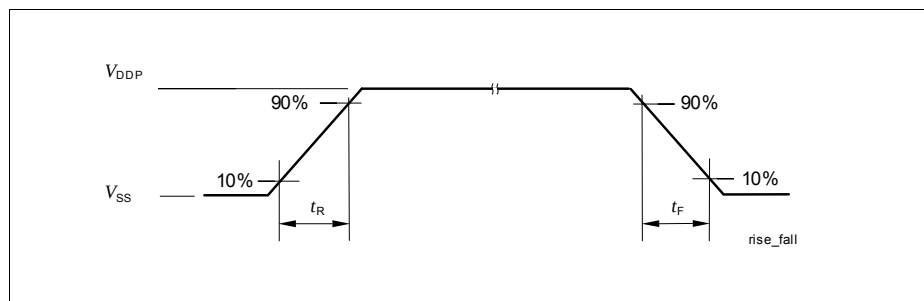


Figure 5 Rise/Fall Time Parameters

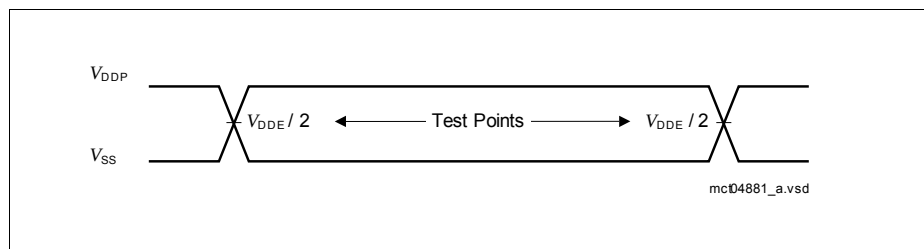


Figure 6 Testing Waveform, Output Delay

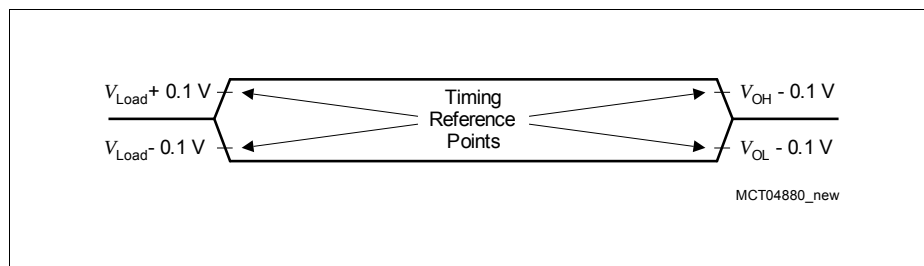


Figure 7 Testing Waveform, Output High Impedance

5.3.2 Power Sequencing

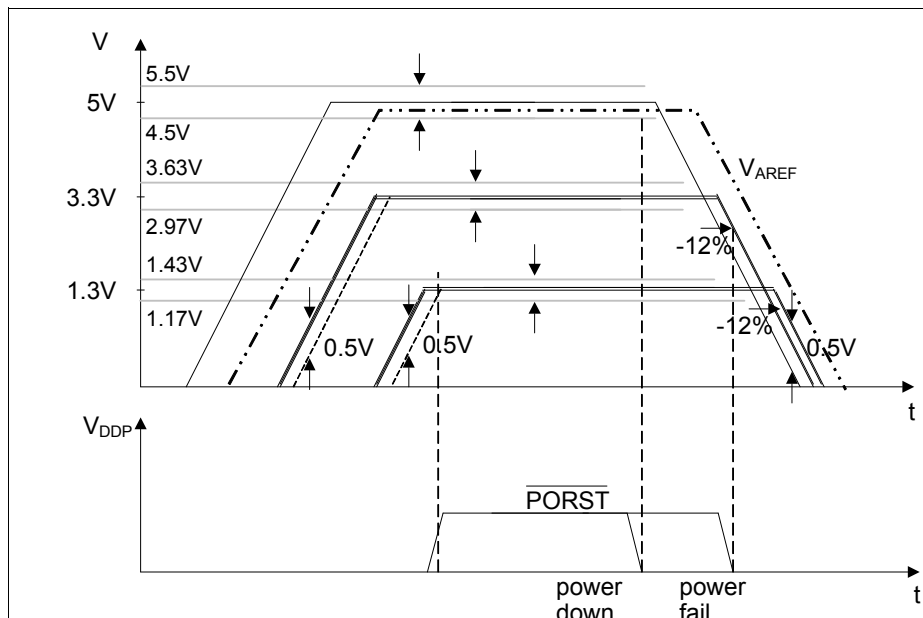


Figure 8 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk, each power supply must be higher than any lower power supply - 0.5 V, or:
 $V_{DD5} > V_{DD3.3} - 0.5 \text{ V}$; $V_{DD5} > V_{DD1.3} - 0.5 \text{ V}$; $V_{DD3.3} > V_{DD1.3} - 0.5 \text{ V}$, see [Figure 8](#).
 - The latch-up risk is minimized if the I/O currents are limited to:
 - 20 mA for one pin group
 - AND 100 mA for the completed device I/Os
 - AND additionally before power-up / after power-down:
 1 mA for one pin in inactive mode (0 V on all power supplies)
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names (for example V_{DDP} , V_{DDFL3} ...), that are internally connected via diodes, must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all V_{DDP}),

Electrical Parameters AC Parameters

are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

1. The PORST signal may be deactivated after all V_{DD5} , $V_{DD3.3}$, $V_{DD1.3}$, and V_{AREF} power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
2. At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
3. At power fail the PORST signal must be activated at latest when any 3.3 V or 1.3 V power supply voltage falls 12% below the nominal level. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the PORST signal should be activated as close as possible to the normal operating voltage range.
4. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
5. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
6. Additionally, regarding the ADC reference voltage V_{AREF} :
 - V_{AREF} must power-up at the same time or later then V_{DDM} , and
 - V_{AREF} must power-down either earlier or at latest to satisfy the condition $V_{AREF} < V_{DDM} + 0.5 \text{ V}$. This is required in order to prevent discharge of V_{AREF} filter capacitance through the ESD diodes through the V_{DDM} power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

5.3.3 Power, Pad and Reset Timing

Table 24 Reset Timings Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time ¹⁾²⁾	$t_{B\ CC}$	150	—	665	μs	$f_{CPU} = 180\ MHz$
Power on Reset Boot Time ³⁾⁴⁾	$t_{BP\ CC}$	—	—	2.5	ms	
HWCFG pins hold time from ESR0 rising edge	$t_{HDH\ SR}$	16 / f_{FPI}	—	—	ns	
HWCFG pins setup time to ESR0 rising edge	$t_{HDS\ CC}$	0	—	—	ns	
Ports inactive after ESR0 reset active	$t_{PI\ CC}$	—	—	8 / f_{FPI}	ns	
Ports inactive after PORST reset active ⁵⁾	$t_{PIP\ CC}$	—	—	150	ns	
Minimum PORST active time after power supplies are stable at operating levels	$t_{POA\ CC}$	10	—	—	ms	
$\overline{TESTMODE} / \overline{TRST}$ hold time from PORST rising edge	$t_{POH\ SR}$	100	—	—	ns	
PORST rise time	$t_{POR\ SR}$	—	—	50	ms	
$\overline{TESTMODE} / \overline{TRST}$ setup time to PORST rising edge	$t_{POS\ SR}$	0	—	—	ns	
Application Reset inactive after PORST deassertion	$t_{POR_APP\ SR}$	—	—	40 ⁶⁾	μs	

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.

3) The duration of the boot time is defined between the rising edge of the $\overline{PORST}$ and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

Electrical Parameters AC Parameters

- 4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.
- 5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
- 6) Application Reset is assumed not to be extended from external, otherwise the time extends by the time the Application Reset is extended.

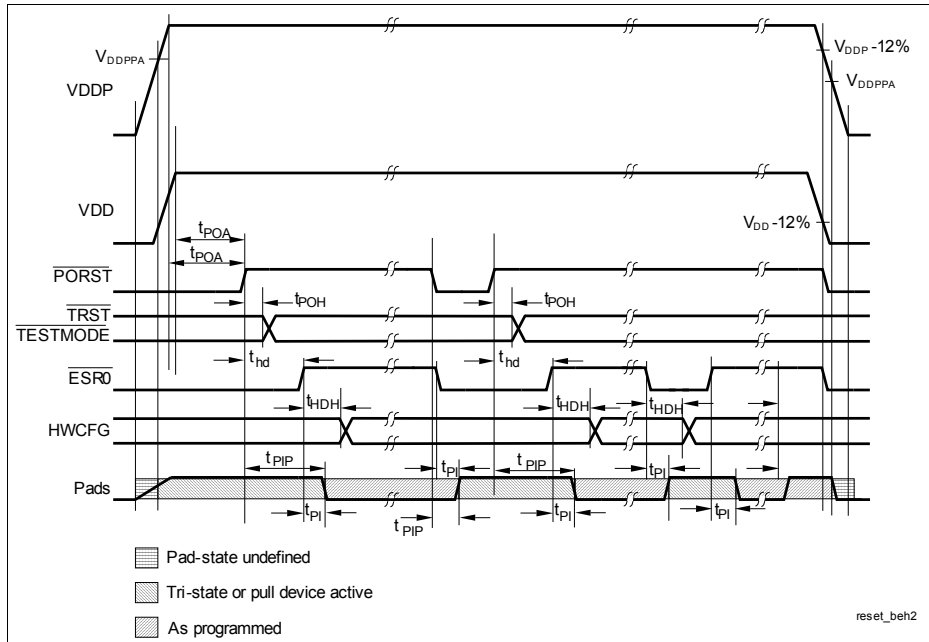


Figure 9 Power, Pad and Reset Timing

5.3.4 Phase Locked Loop (PLL)

Table 25 PLL_SysClk Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_p CC	-7	—	7	ns	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	f_{REF} CC	8	—	16	MHz	
VCO frequency range	f_{VCO} CC	400	—	720	MHz	
PLL lock-in time	t_L CC	14	—	200	μ s	$N > 32$
		14	—	400	μ s	$N \leq 32$

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the $K2$ -factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for } (K2 \leq 100) \quad \text{and} \quad (m \leq (f_{LMB}[\text{MHz}]) / 2)$$

$$|D_m[\text{ns}]| = \left(\frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[\text{MHz}] - 1} + 0,01 \times K2 \right) \quad (6)$$

$$\text{else} \quad |D_m[\text{ns}]| = \frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \quad (7)$$

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the $K2$ -factor of the PLL. Beyond this value of m the maximum

Electrical Parameters AC Parameters

accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20$ pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} and V_{SSOSC} , is limited to a peak-to-peak voltage of $V_{PP} = 100$ mV for noise frequencies below 300 KHz and $V_{PP} = 40$ mV for noise frequencies above 300 KHz.

The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC} and V_{SSOSC} , is limited to a peak-to-peak voltage of $V_{PP} = 100$ mV for noise frequencies below 300 KHz and $V_{PP} = 40$ mV for noise frequencies above 300 KHz.

These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

Oscillator Watchdog (OSC_WDT)

The expected input frequency is selected via the bit field SCU_OSCCON.OSCVAL. The OSC_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is f_{OSCREF} which is derived for f_{OSC} .

(8)

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1}$$

The divider value SCU_OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is 2.5 MHz.

Note: f_{OSCREF} has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.

The monitored frequency is too low if it is below 1.25 MHz and too high if it is above 7.5 MHz. This leads to the following two conditions:

- Too low: $f_{OSC} < 1.25 \text{ MHz} \times (SCU_OSCCON.OSCVAL + 1)$
- Too high: $f_{OSC} > 7.5 \text{ MHz} \times (SCU_OSCCON.OSCVAL + 1)$

Note: The accuracy is 30% for these boundaries.

5.3.5 ERAY Phase Locked Loop (ERAY_PLL)

Table 26 PLL_ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at SYSCLK pin	D_{PP} CC	-0.8	—	0.8	ns	
Accumulated_Jitter	D_P CC	-0.5	—	0.5	ns	
PLL Base Frequency of the ERAY PLL	$f_{PLLBASE_ERAY}$ CC	50	250	360	MHz	
VCO input frequency of the ERAY PLL	f_{REF} CC	20	—	40	MHz	
VCO frequency range of the ERAY PLL	f_{VCO_ERAY} CC	450	—	500	MHz	
PLL lock-in time	t_L CC	5.6	—	200	μs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20$ pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDPF3} and V_{SSOSC} , is limited to a peak-to-peak voltage of $V_{PP} = 100$ mV for noise frequencies below 300 KHz and $V_{PP} = 40$ mV for noise frequencies above 300 KHz.

These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

5.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

**Table 27 JTAG Interface Timing Parameters
(Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	10	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge ¹⁾ (propagation delay)	t_8 CC	–	–	13	ns	$C_L = 50$ pF
	t_8 CC	3	–	–	ns	$C_L = 20$ pF
TDO hold after TCK falling edge ¹⁾	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge ¹⁾²⁾	t_9 CC	–	–	14	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge ¹⁾	t_{10} CC	–	–	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

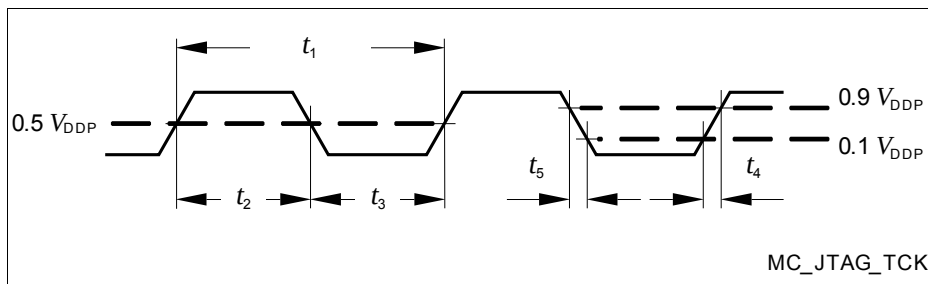


Figure 10 Test Clock Timing (TCK)

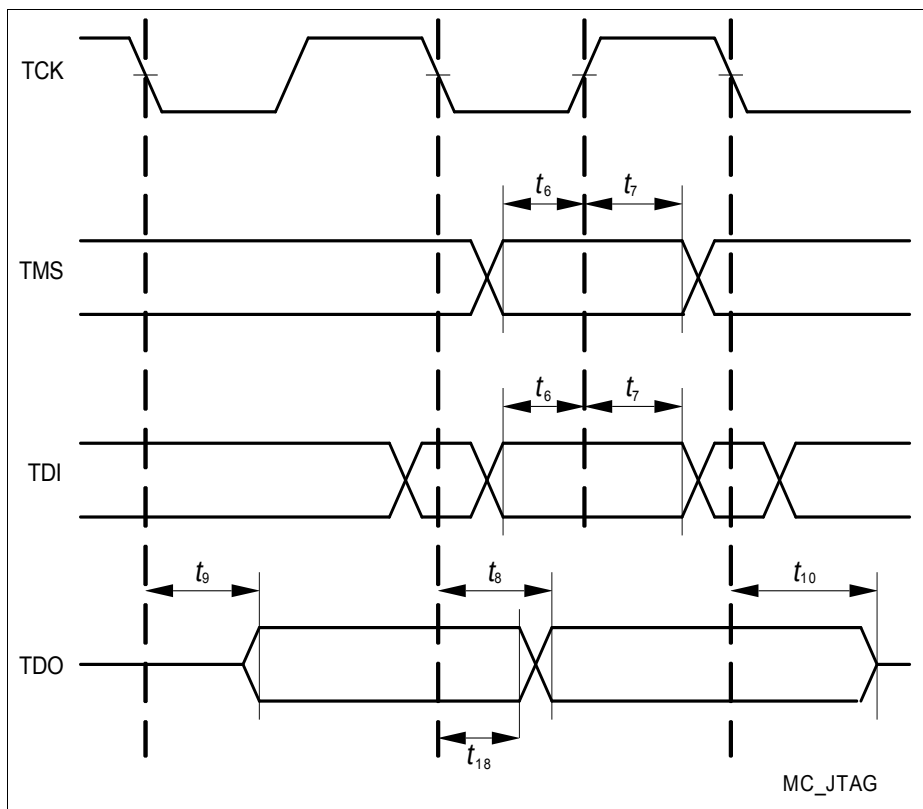


Figure 11 JTAG Timing

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 28 DAP Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period ¹⁾	t_{TCK} SR	12.5	–	–	ns	
DAP0 high time	t_{12} SR	4	–	–	ns	
DAP0 low time ¹⁾	t_{13} SR	4	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	2	ns	
DAP0 clock fall time	t_{15} SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period ²⁾	t_{19} CC	8	–	–	ns	$C_L = 20$ pF; $f = 80$ MHz
		10	–	–	ns	$C_L = 50$ pF; $f = 40$ MHz

1) See the DAP chapter for clock rate restrictions in the Active:IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

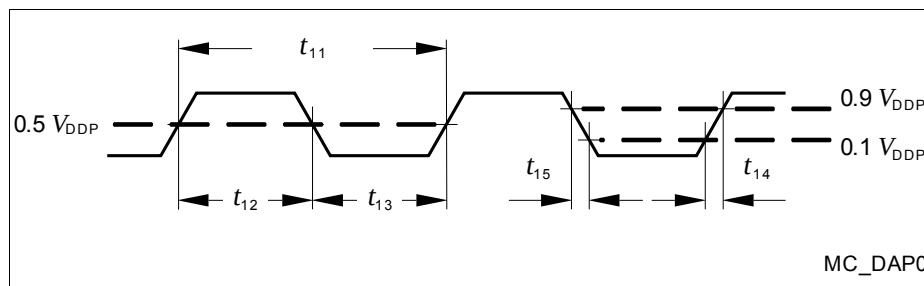


Figure 12 Test Clock Timing (DAP0)

Electrical ParametersAC Parameters

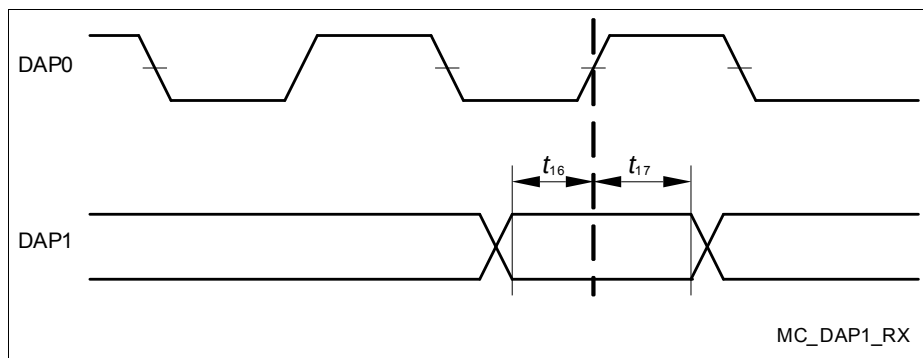


Figure 13 DAP Timing Host to Device

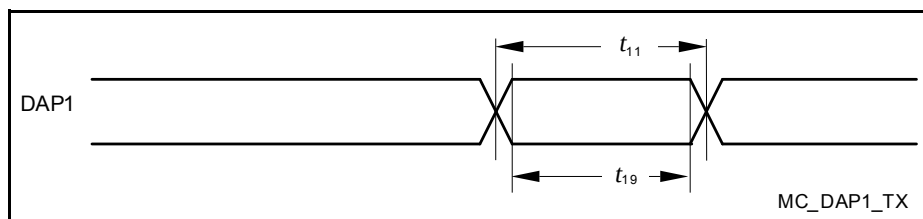


Figure 14 DAP Timing Device to Host

5.3.8 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

5.3.8.1 Micro Link Interface (MLI) Timing

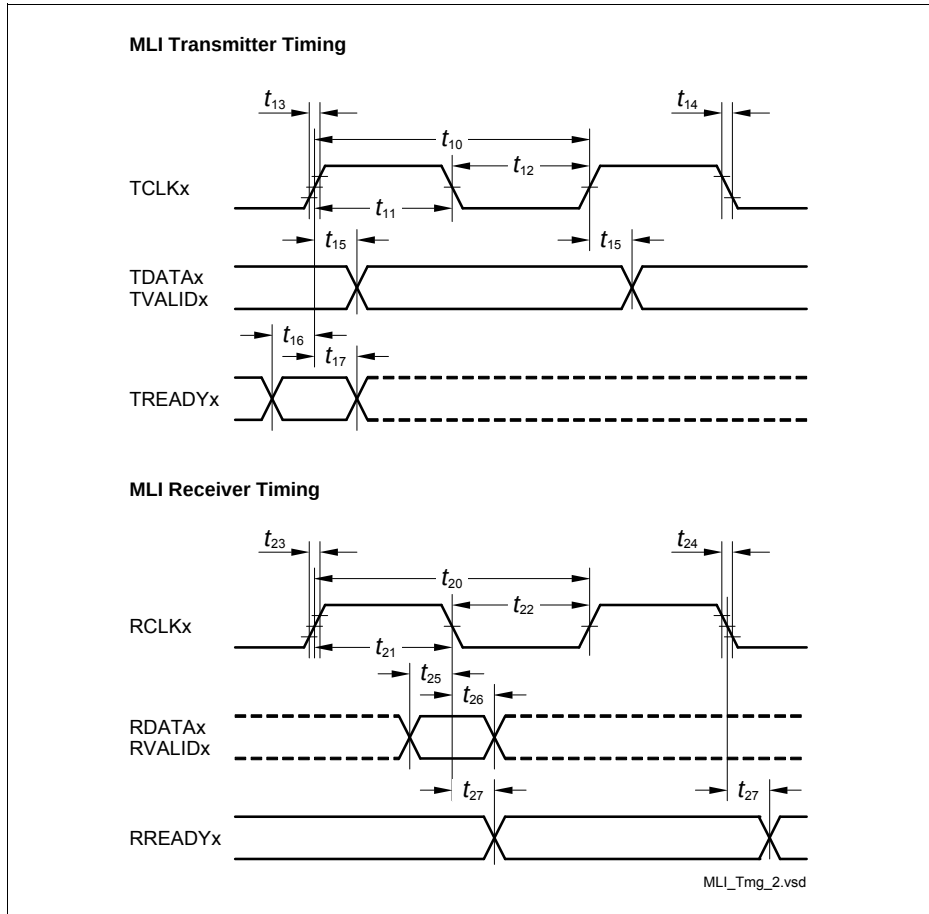


Figure 15 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

Electrical Parameters AC Parameters

The MLI parameters are valid for $C_L = 50 \text{ pF}$ and strong driver medium edge.

Table 29 MLI Receiver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	t_{20} SR	$1 / f_{FPI}$	—	—	ns	
RCLK high time ¹⁾²⁾	t_{21} SR	—	$0.5 \times t_{20}$	—	ns	
RCLK low time ¹⁾²⁾	t_{22} SR	—	$0.5 \times t_{20}$	—	ns	
RCLK rise time ³⁾	t_{23} SR	—	—	4	ns	
RCLK fall time ³⁾	t_{24} SR	—	—	4	ns	
RDATA/RVALID setup time before RCLK falling edge	t_{25} SR	4.2	—	—	ns	
RDATA/RVALID hold time after RCLK falling edge	t_{26} CC	2.2	—	—	ns	
RREADY output delay time	t_{27} CC	0	—	16	ns	

1) The following formula is valid: $t_{21} + t_{22} = t_{20}$.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for $f_{SYS} = 90 \text{ MHz}$. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

Table 30 MLI Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	t_{10} CC	$2 \times 1 / f_{FPI}$	—	—	ns	
TCLK high time ¹⁾²⁾	t_{11} CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	
TCLK low time ¹⁾²⁾	t_{12} CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	
TCLK rise time	t_{13} CC	—	—	$0.3 \times t_{10}$ ³⁾	ns	

Electrical Parameters AC Parameters

Table 30 MLI Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK fall time	t_{14} CC	—	—	$0.3 \times t_{10}^{3)}$	ns	
TDATA/TVALID output delay time	t_{15} CC	-3	—	4.4	ns	
TREADY setup time before TCLK rising edge	t_{16} SR	18	—	—	ns	
TREADY hold time after TCLK rising edge	t_{17} SR	-2	—	—	ns	

1) The following formula is valid: $t_{11} + t_{12} = t_{10}$.

2) The min./max. TCLK low/high times t_{11}/t_{12} include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t_{11} / t_{12} .

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

The MSC parameters are valid for $C_L = 50$ pF.

Table 31 MSC Parameters

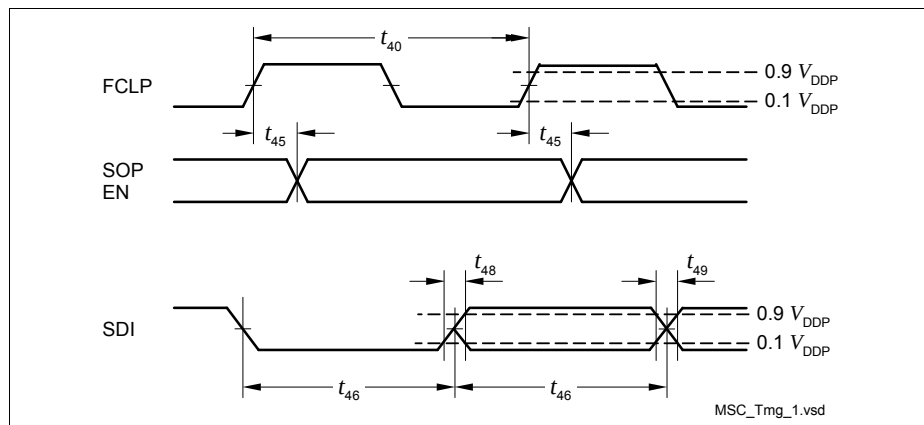
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period ¹⁾²⁾	t_{40} CC	$2 \times T_{MSC}^{3)}$	—	—	ns	
SOP ⁴⁾ /ENx outputs delay from FCLP ⁴⁾ rising edge	t_{45} CC	-2	—	5	ns	ENx with strong driver and sharp (minus) edge
		-2	—	10	ns	ENx with strong driver and medium (minus) edge
		0	—	21	ns	ENx with strong driver and soft edge

Electrical ParametersAC Parameters

Table 31 MSC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} CC	$8 \times T_{MSC}$	—	—	ns	
SDI rise time	t_{48} SR	—	—	200	ns	
SDI fall time	t_{49} SR	—	—	200	ns	

- 1) FCLP signal rise/fall times are only defined by the pad rise/fall times.
- 2) FCLP signal high and low can be minimum $1 \times T_{MSC}$
- 3) $T_{MSC} = T_{SYS} = 1 / f_{SYS}$.
- 4) SOP / FCLP either propagated by LVDS or by CMOS strong driver and non soft edge.


Figure 16 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

5.3.8.3 SSC Master/Slave Mode Timing

The SSC parameters are valid for $C_L = 50 \text{ pF}$ and strong driver medium edge.

Table 32 SSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period ¹⁾²⁾³⁾	t_{50} CC	$2 \times 1 / f_{FPI}$	—	—	ns	
MTSR/SLSOx delay from SCLK rising edge	t_{51} CC	0	—	8	ns	
MRST setup to SCLK latching edge ³⁾	t_{52} SR	16.5	—	—	ns	
MRST hold from SCLK latching edge ³⁾	t_{53} SR	0	—	—	ns	
SCLK input clock period ¹⁾³⁾	t_{54} SR	$4 \times 1 / f_{FPI}$	—	—	ns	
SCLK input clock duty cycle	t_{55} – t_{54} SR	45	—	55	%	
MTSR setup to SCLK latching edge ³⁾⁴⁾	t_{56} SR	$1 / f_{FPI}$	—	—	ns	
MTSR hold from SCLK latching edge	t_{57} SR	$1 / f_{FPI} + 5$	—	—	ns	
SLSI setup to first SCLK latching edge	t_{58} SR	$1 / f_{FPI} + 5$	—	—	ns	
SLSI hold from last SCLK latching edge ⁵⁾	t_{59} SR	7	—	—	ns	
MRST delay from SCLK shift edge	t_{60} CC	0	—	16.5	ns	
SLSI to valid data on MRST	t_{61} CC	—	—	16.5	ns	

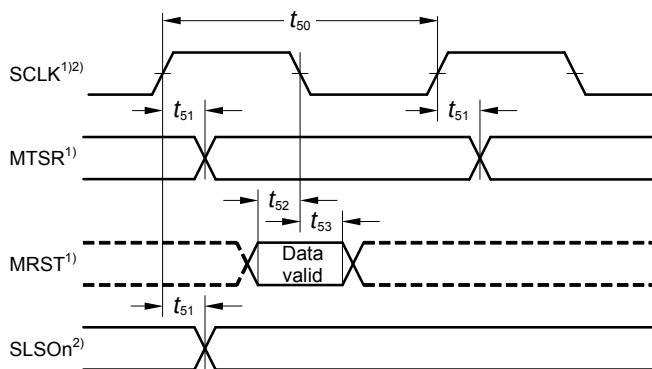
1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum $1 \times TSSC$.

3) $TSSC_{min} = T_{SYS} = 1/f_{SYS}$.

4) Fractional divider switched off, SSC internal baud rate generation used.

5) For $CON.PH=1$ slave select must not be removed before the following shifting edge. This means, that whatever is configured (shifting / latching first), SLSI must not be de-activated before the last trailing edge from the pair of shifting / latching edges.

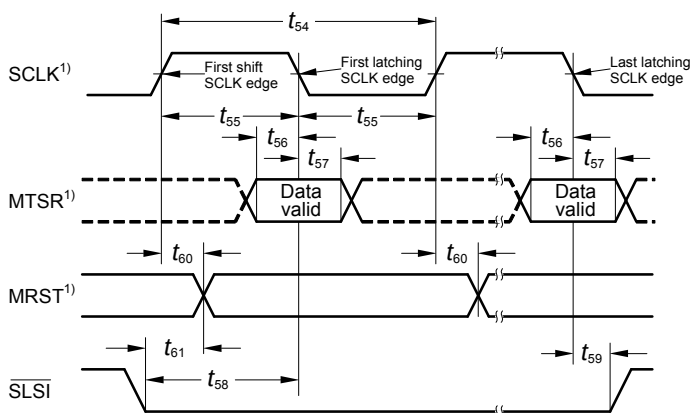


1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOn is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_TmgMM

Figure 17 SSC Master Mode Timing



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_TmgSM

Figure 18 SSC Slave Mode Timing

Electrical Parameters AC Parameters

5.3.8.4 ERAY Interface Timing

The timings of this section are valid for the strong driver and either sharp edge or medium edge settings of the output drivers with $C_L = 25 \text{ pF}$.

Table 33 ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Time span from last BSS to FES without the influence of quartz tolerancies (d10Bit_TX) ¹⁾	$t_{60} \text{ CC}$	997.75	—	1002.25	ns	
TxD data valid from fsample flip flop txd_reg TxDA, TxDB (dTxAsym) ²⁾³⁾	$t_{61}-t_{62} \text{ CC}$	—	—	1.5	ns	Asymmetrical delay of rising and falling edge (TxDA, TxDB)
Time span between last BSS and FES without influence of quartz tolerancies (d10Bit_RX) ¹⁾⁴⁾⁵⁾	$t_{63} \text{ SR}$	966	—	1046.1	ns	
RxD capture by fsample (RxDA/RxDB sampling flip-flop) (dRxAsym) ⁵⁾	$t_{64}-t_{65} \text{ CC}$	—	—	3.0	ns	Asymmetrical delay of rising and falling edge (RxDA, RxDB)
TxD data delay from sampling flip-flop	$dTxdly \text{ CC}$	—	—	10.0	ns	$Px_PDR.PDy = 000_B$
		—	—	15.0	ns	$Px_PDR.PDy = 001_B$
RxD capture delay by sampling flip-flop	$dRxdly \text{ CC}$	—	—	10.0	ns	

1) This includes the PLL_ERAY accumulated jitter.

2) Refers to delays caused by the asymmetries of the output drivers of the digital logic and the GPIO pad drivers. Quarz tolerance and PLL_ERAY accumulated jitter are not included.

3) E-Ray TxD output drivers have an asymmetry of rising and falling edges of $|t_{FA2} - t_{RA2}| \leq 1 \text{ ns}$.

4) Limits of 966ns and 1046.1ns correspond to (30%, 70%) * V_{DDP} FlexRay standard input thresholds. For input thresholds of this product, a correction of - 0.5 ns and +0.1 ns has to be applied.

5) Valid for output slopes of the bus driver of $dRxSlope \leq 5\text{ns}$, 20% * V_{DDP} to 80% * V_{DDP} , according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: $-1.6\text{ns} \leq t_{FA2} - t_{RA2} \leq 1.3\text{ns}$.

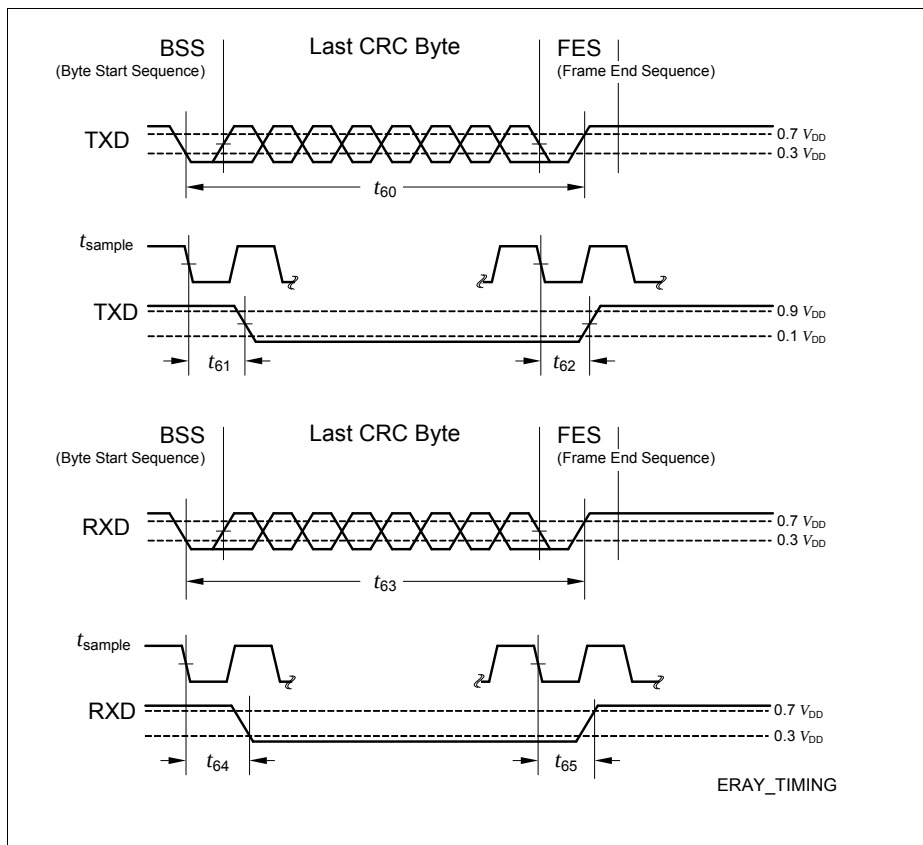


Figure 19 ERAY Timing

5.3.8.5 EBU Timings

EBU Asynchronous Timings

$V_{SS} = 0\text{ V}$; $V_{DD} = 1.3\text{ V} \pm 5\%$; $V_{DDEBU} = 2.5\text{ V} \pm 5\%$ and $3.3\text{ V} \pm 5\%$, Class A2 pins;
 $C_L = 35\text{ pF}$ for address/data; $C_L = 40\text{ pF}$ for the control lines.

For each timing, the accumulated PLL jitter of the programed duration in number of clock periods must be added separately. Operating conditions apply and $C_L = 35\text{ pF}$.

Table 34 EBU Common Asynchronous Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pulse width deviation from the ideal programmed width due to B pad asymmetry, rise delay - fall delay	t_a CC	-0.8	—	0.8	ns	edge= medium
		-0.8	—	0.8	ns	edge= sharp
AD(31:0) output delay to ADV# rising edge, multiplexed read / write	t_{13} CC	-5.5	—	2	ns	
AD(31:0) output delay to ADV# rising edge, multiplexed read / write	t_{14} CC	-5.5	—	2	ns	

Table 35 EBU Asynchronous Read Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to $\overline{RD}$ rising edge, deviation from the ideal programmed value	t_0 CC	-2.5	—	2.5	ns	
A(23:0) output delay to RD rising edge, deviation from the ideal programmed value	t_1 CC	-2.5	—	2.5	ns	

Electrical Parameters AC Parameters

Table 35 EBU Asynchronous Read Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CS rising edge to RD rising edge, deviation from the ideal programmed value	t_2 CC	-2	—	2.5	ns	
ADV rising edge to RD rising edge, deviation from the ideal programmed value	t_3 CC	-1.5	—	4.5	ns	
BC rising edge to RD rising edge, deviation from the ideal programmed value	t_4 CC	-2.5	—	2.5	ns	
WAIT input setup to RD rising edge, deviation from the ideal programmed value	t_5 SR	12	—	—	ns	
WAIT input hold to RD rising edge, deviation from the ideal programmed value	t_6 SR	0	—	—	ns	
Data input setup to RD rising edge, deviation from the ideal programmed value	t_7 SR	12	—	—	ns	
Data input hold to RD rising edge, deviation from the ideal programmed value	t_8 SR	0	—	—	ns	
MR / W output delay to RD# rising edge, deviation from the ideal programmed value	t_9 CC	-2.5	—	1.5	ns	

Electrical Parameters AC Parameters

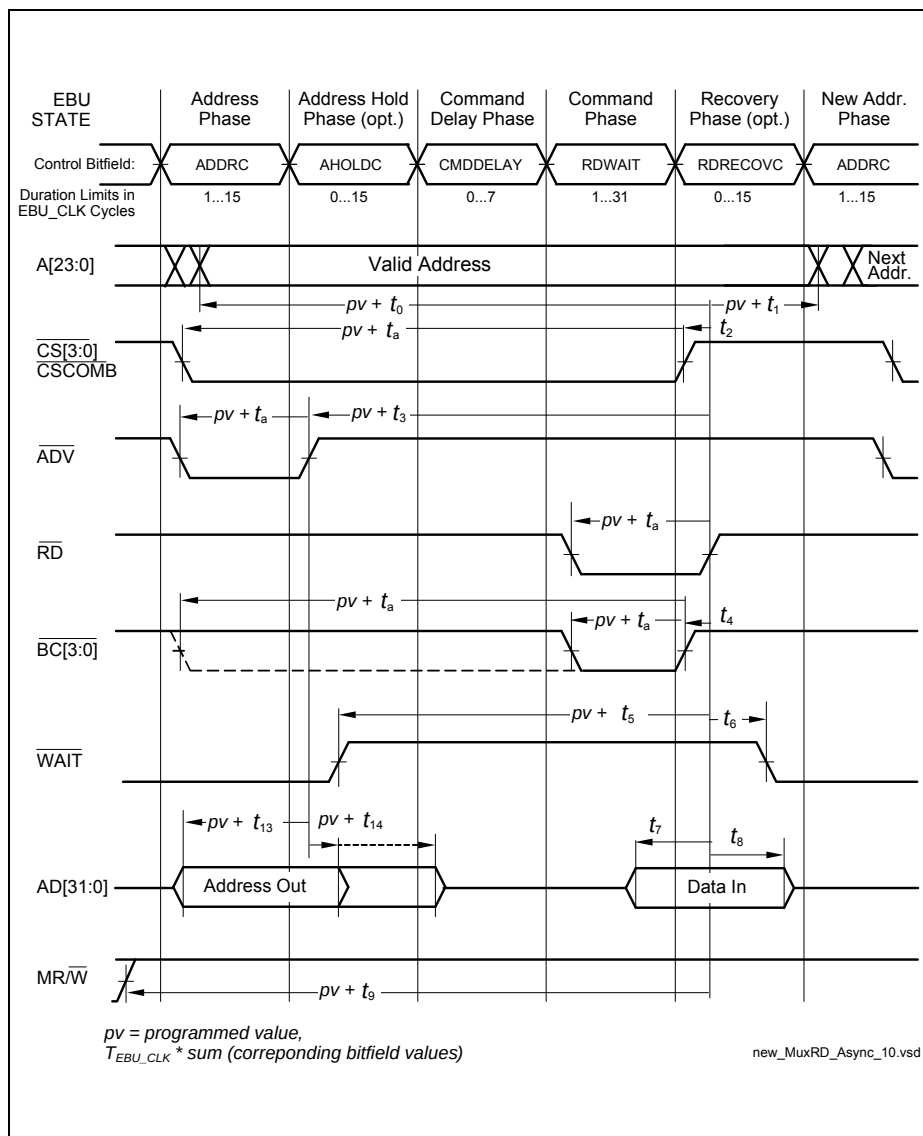


Figure 20 Multiplexed Read Access

Electrical ParametersAC Parameters

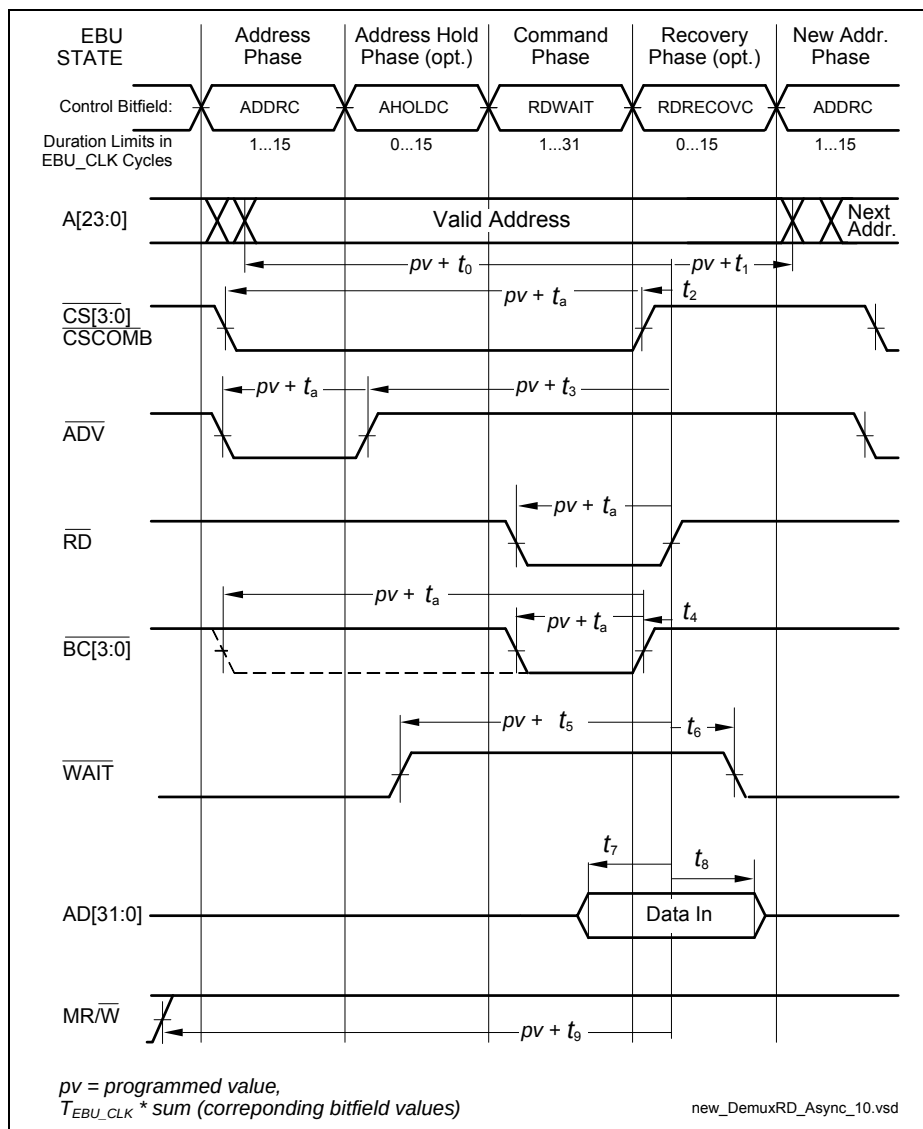


Figure 21 Demultiplexed Read Access

Table 36 EBU Asynchronous Write Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value	t_{30} CC	-2.5	—	2.5	ns	
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value	t_{31} CC	-2.5	—	2.5	ns	
CS rising edge to WR rising edge, deviation from the ideal programmed value	t_{32} CC	-2	—	2	ns	
ADV rising edge to WR rising edge, deviation from the ideal programmed value	t_{33} CC	-2.5	—	2	ns	
BC rising edge to WR rising edge, deviation from the ideal programmed value	t_{34} CC	-2.5	—	2	ns	
WAIT input setup to WR rising edge, deviation from the ideal programmed value	t_{35} SR	12	—	—	ns	
WAIT input hold to WR rising edge, deviation from the ideal programmed value	t_{36} SR	0	—	—	ns	
Data output delay to WR rising edge, deviation from the ideal programmed value	t_{37} CC	-5.5	—	2	ns	

Electrical ParametersAC Parameters

Table 36 EBU Asynchronous Write Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data output delay to WR rising edge, deviation from the ideal programmed value	t_{38} CC	-5.5	—	2	ns	
MR / W output delay to WR rising edge, deviation from the ideal programmed value	t_{39} CC	-2.5	—	1.5	ns	

Electrical Parameters AC Parameters

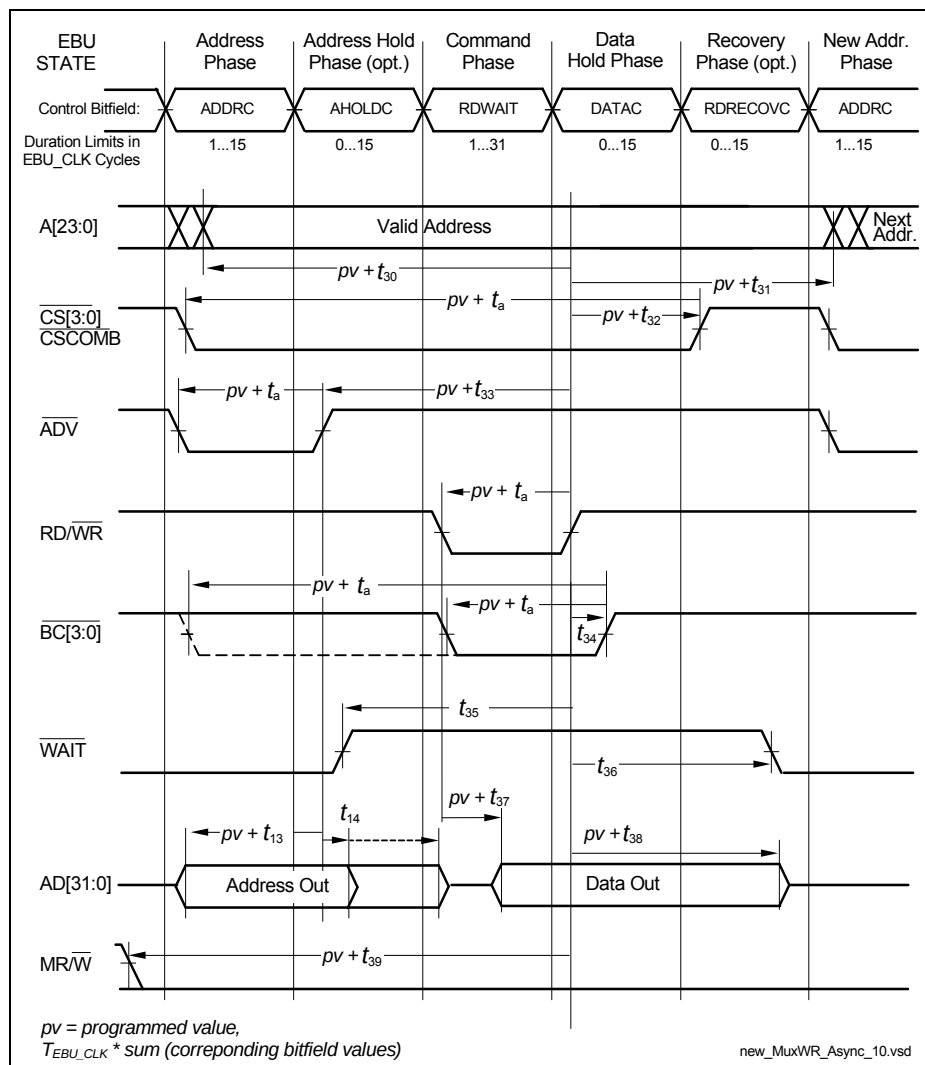


Figure 22 Multiplexed Write Access

Electrical Parameters AC Parameters

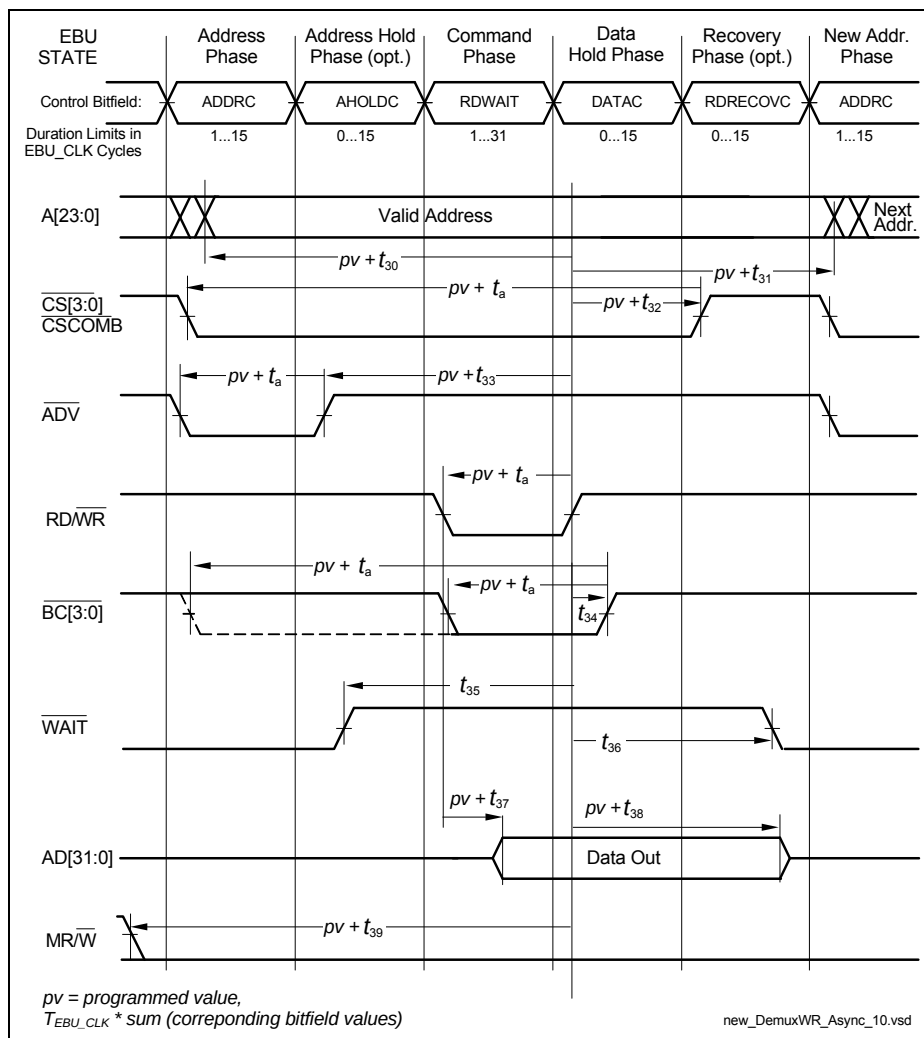


Figure 23 Demultiplexed Write Access

5.4 Package and Reliability

5.4.1 Package Parameters

Table 37 Thermal Characteristics of the Package

Device	Package	$R_{\Theta JCT}^{1)}$	$R_{\Theta JCB}^{1)}$	$R_{\Theta JLead}$	Unit	Note
TC1784	PG-LFBGA-292-6	6,8	4,8	17,0	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT} , R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT} , R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT} , R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

5.4.2 Package Outline

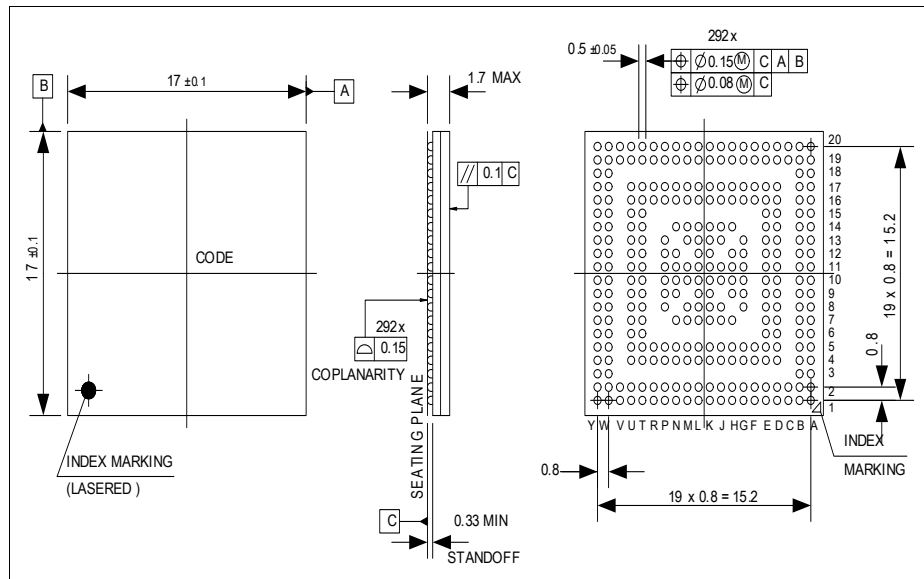


Figure 24 Package Outlines PG-LFBGA-292-6

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: <http://www.infineon.com/products>.

5.4.3 Flash Memory Parameters

The data retention time of the TC1784’s Flash memory depends on the number of times the Flash memory has been erased and programmed.

Table 38 FLASH32 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Sector	t_{ERD} CC	—	—	3 ¹⁾	s	
Program Flash Erase Time per 256 KByte Sector	t_{ERP} CC	—	—	5	s	

Electrical Parameters Package and Reliability

Table 38 FLASH32 Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page ²⁾	t_{PRD} CC	—	—	5.3	ms	without reprogramming
		—	—	15.9	ms	with two reprogramming cycles
Program time program flash per page ³⁾	t_{PRP} CC	—	—	5.3	ms	without reprogramming
		—	—	10.6	ms	with one reprogramming cycle
Data Flash Endurance	N_E CC	60000 ⁴⁾	—	—	cycles	Min. data retention time 5 years
Erase suspend delay	t_{FL_ErSusp} CC	—	—	15	ms	
Wait time after margin change	$t_{FL_MarginDel}$ CC	10	—	—	μs	
Program Flash Retention Time, Physical Sector ⁵⁾⁶⁾	t_{RET} CC	20	—	—	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector ⁵⁾⁶⁾	t_{RETL} CC	20	—	—	years	Max. 100 erase/program cycles
UCB Retention Time ⁵⁾⁶⁾	t_{RTU} CC	20	—	—	years	Max. 4 erase/program cycles per UCB
Wake-Up time	t_{WU} CC	—	—	270	μs	
DFlash wait state configuration	WS_{DF} CC	50 ns x f_{FSI}	—	—		
PFlash wait state configuration	WS_{PF} CC	26 ns x f_{FSI}	—	—		

1) In case of wordline oriented defects (see robust EEPROM emulation in the User's Manual) this erase time can increase by up to 100%.

2) In case the Program Verify feature detects weak bits, these bits will be programmed up to twice more. Each reprogramming takes additional 5 ms.

Electrical Parameters Package and Reliability

- 3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.
- 4) Only valid when a robust EEPROM emulation algorithm is used. For more details see the User's Manual.
- 5) Storage and inactive time included.
- 6) At average weighted junction temperature $T_j = 100^\circ\text{C}$, or the retention time at average weighted temperature of $T_j = 110^\circ\text{C}$ is minimum 10 years, or the retention time at average weighted temperature of $T_j = 150^\circ\text{C}$ is minimum 0.7 years.

5.4.4 Quality Declarations

Table 39 **Quality Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime ¹⁾	t_{OP}	–	–	24000	hours	– ²⁾
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.

2) For worst-case temperature profile equivalent to:

1200 hours at $T_j = 125...150^\circ\text{C}$

3600 hours at $T_j = 110...125^\circ\text{C}$

7200 hours at $T_j = 100...110^\circ\text{C}$

11000 hours at $T_j = 25...100^\circ\text{C}$

1000 hours at $T_j = -40...25^\circ\text{C}$

6 History

The Version 0.7 is the first version of this document:

The following changes were done between Version 0.7 and 0.71 of this document:

- update and correct figure 3-2
- update and correct table 3-1

The following changes were done between Version 0.71 and 1.0 of this document:

- adapt Absolute Maximum Rating
- clarify pad supply levels in Pin Reliability in Overload section
- add note at the end of Pin Reliability in Overload section
- clarify wording for valid operating conditions
- split FADC DNL parameter into two conditions and change value for gain 4 and 8
- add footnote 5 to I_{DDP}
- add footnote for D-Flash currents in power section
- rework first sentence for chapter 5.3
- reduce min value for t_L for both PLLs
- add for MLI and SSC timing parameter: valid strong driver medium edge only
- change MLI parameter t_{17} min value
- update parameter description for SSC parameters t_{52} , t_{53} , t_{56} , t_{57} , t_{58} , and t_{59}
- change SSC parameters from CC to SR Symbol for t_{56} , t_{57} , t_{58} and t_{59}
- add footnote to Flash parameter t_{ERD}

The following changes were done between Version 1.0 and 1.1 of this document:

- remove the following product options:
 - SAK-TC1784N-320F180EL
- add the following product options:
 - SAK-TC1784F-320F180EP
- change t_{48} from 100ns to 200ns in table 42
- change t_{49} from 100ns to 200ns in table 42
- extend K_{OVAN} condition from $I_{OV} \leq 0$ mA; $I_{OV} \geq -1$ mA to $I_{OV} \leq 0$ mA; $I_{OV} \geq -2$ mA
- change parameter EF_{OFF} from +90mV to +120 for condition Calibration = No
- change package version from PG-LFBGA-292-3 to PG-LFBGA-292-6

The following changes were done between Version 1.1 and 1.1.1 of this document:

- change parameter EF_{OFF} from +120mV to +90 for condition Calibration = No

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