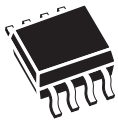
M95256-W M95256-R M95256-DR M95256-DF

256-Kbit serial SPI bus EEPROM with high-speed clock

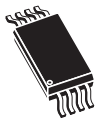
Datasheet – production data

Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 256 Kb (32 Kbytes) of EEPROM
  - Page size: 64 bytes
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Additional Write lockable page (Identification page)
- Write Protect: quarter, half or whole memory array
- High-speed clock: 20 MHz
- Single supply voltage:
  - 2.5 V to 5.5 V for M95256-W
  - 1.8 V to 5.5 V for M95256-R and M95256-DR
  - 1.7 V to 5.5 V for M95256-DF
- Operating temperature range: from -40°C up to +85°C
- Enhanced ESD protection
- More than 4 million Write cycles
- More than 200-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width

UFDFPN8 (MC)
2 x 3 mm (MLP)

WLCSP (CS)
(preliminary data)

Contents

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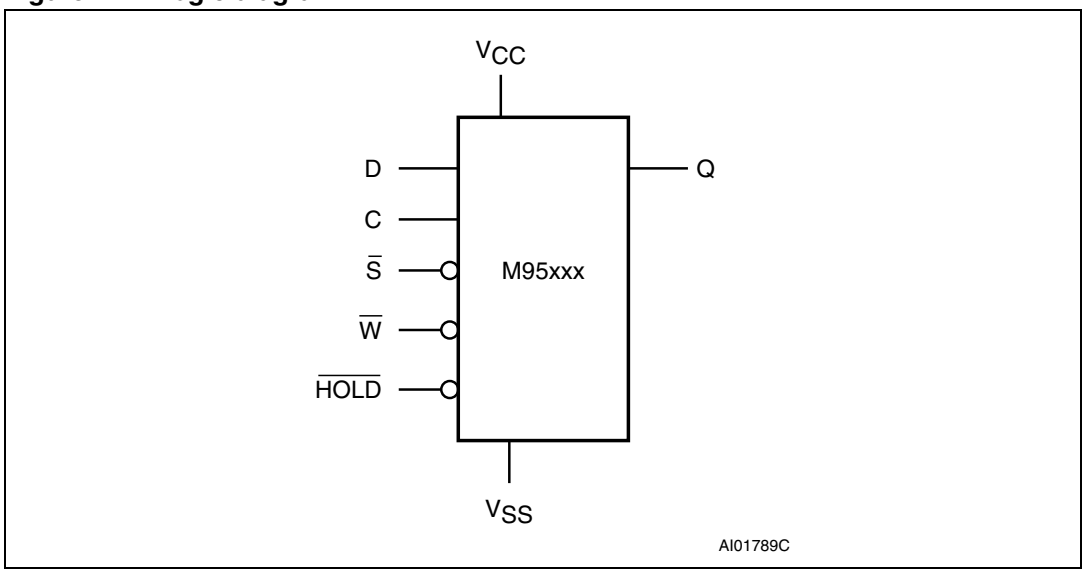
1 Description

The M95256 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 32768 x 8 bits, accessed through the SPI bus.

The M95256-W can operate with a supply voltage from 2.5 V to 5.5 V, the M95256-R and M95256-DR can operate with a supply voltage from 1.8 V to 5.5 V, and the M95256-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

The M95256-Dx offers an additional page, named the Identification Page (64 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

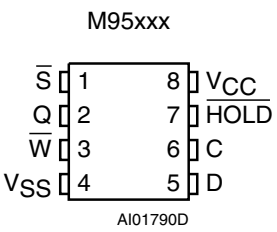


The SPI bus signals are C, D and Q, as shown in *Figure 1* and *Table 1*. The device is selected when Chip Select ($\overline{S}$) is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ is driven low.

Table 1. Signal names

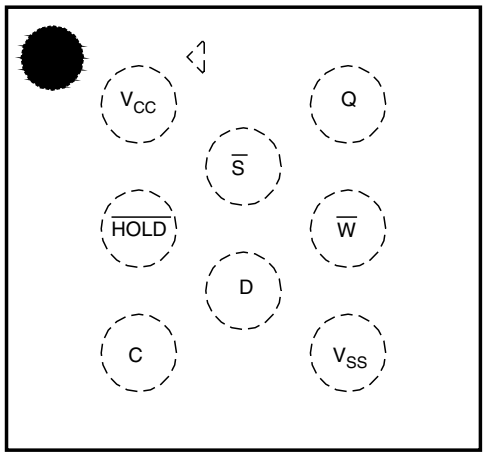
Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections (top view)



1. See *Section 10: Package mechanical data* section for package dimensions, and how to identify pin 1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)

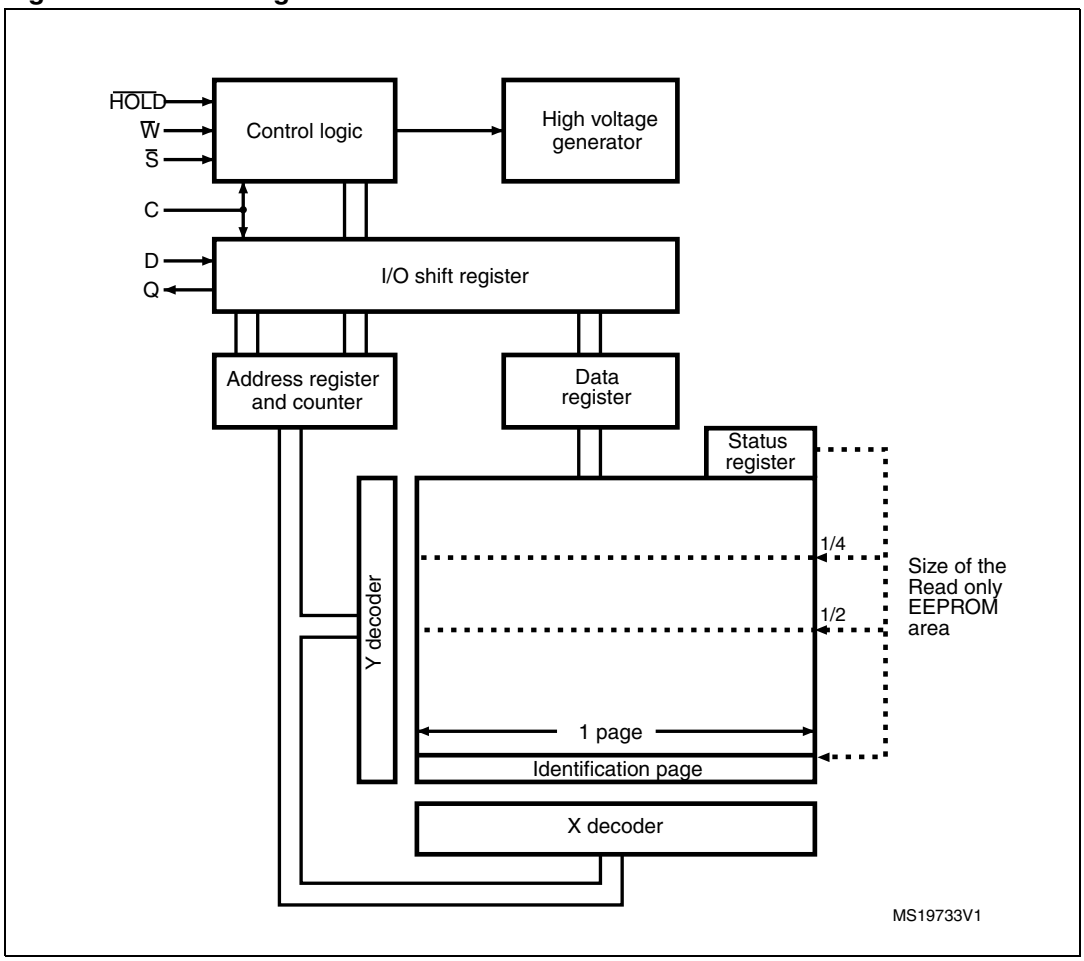


Caution: As EEPROM cells lose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

2 Memory organization

The memory is organized as shown in the following figure.

Figure 4. Block diagram



3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Section 9: DC and AC parameters*). These signals are described next.

3.1 Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

3.2 Serial Data Input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).

3.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby Power mode, unless an internal Write cycle is in progress. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

3.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all Write instructions.

3.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

3.8 V_{SS} ground

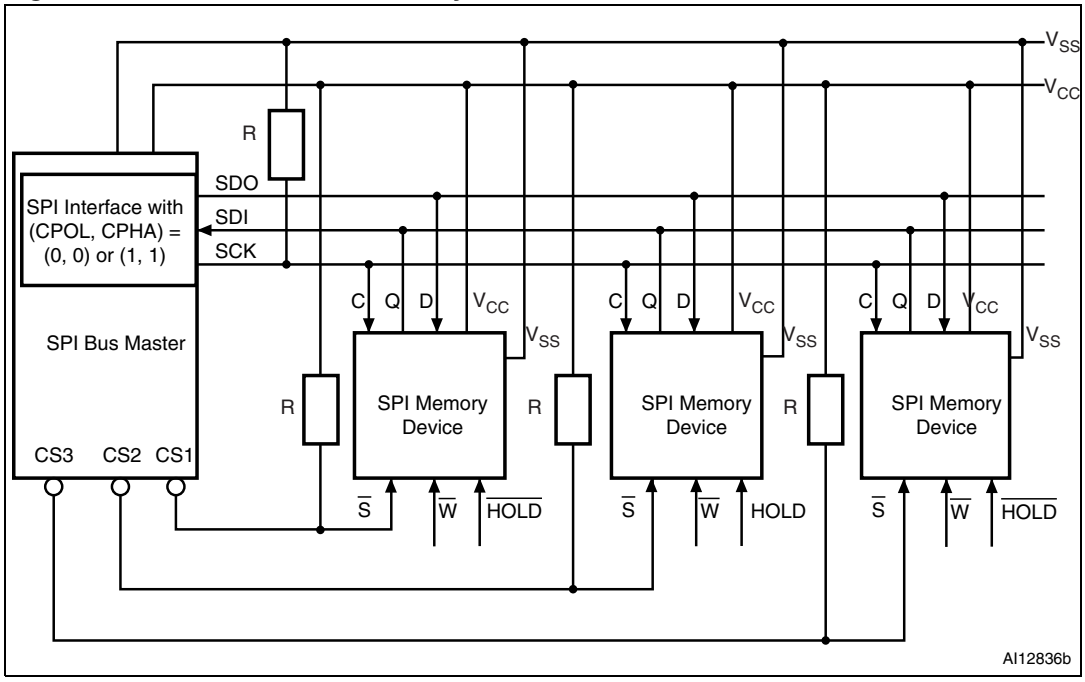
V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

4 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 5. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 5 shows an example of three memory devices connected to an SPI bus master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 5*) ensures that a device is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state.

In applications where the Bus Master may leave all SPI bus lines in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

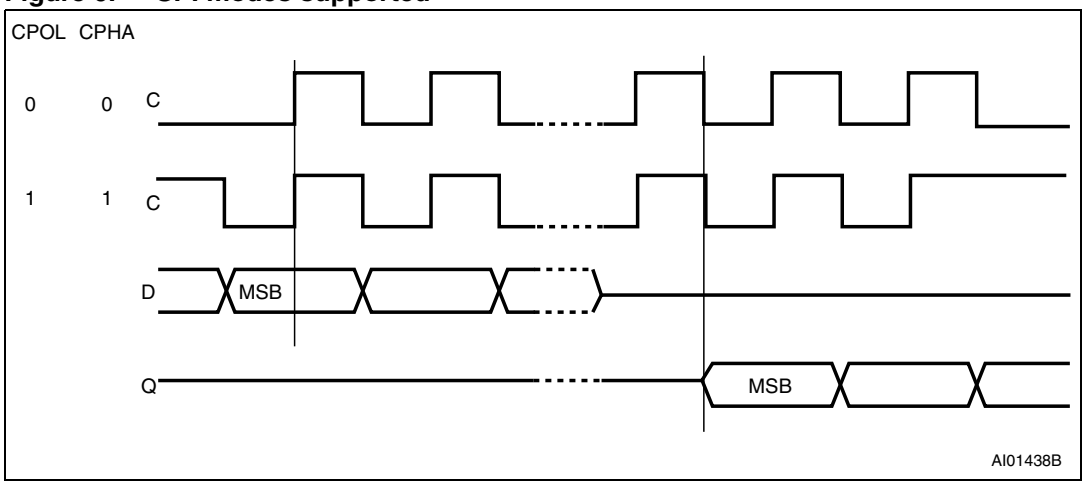
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 6*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 6. SPI modes supported



5 Operating features

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 9: DC and AC parameters*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} device pins.

5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until VCC reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 9: DC and AC parameters*).

At power-up, when V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode,
- deselected,
- Status Register values:
  - The Write Enable Latch (WEL) bit is reset to 0.
  - The Write In Progress (WIP) bit is reset to 0.
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC}(min), V_{CC}(max)] range, as defined under Operating conditions in *Section 9: DC and AC parameters*.

5.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 5*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*, and the rise time must not vary faster than 1 V/µs.

5.1.4 Power-down

During power-down (continuous decrease of the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined under Operating conditions in *Section 9: DC and AC parameters*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC}),
- in Standby Power mode (there should not be any internal write cycle in progress).

5.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1}, as specified in DC characteristics (see *Section 9: DC and AC parameters*).

5.3 Hold condition

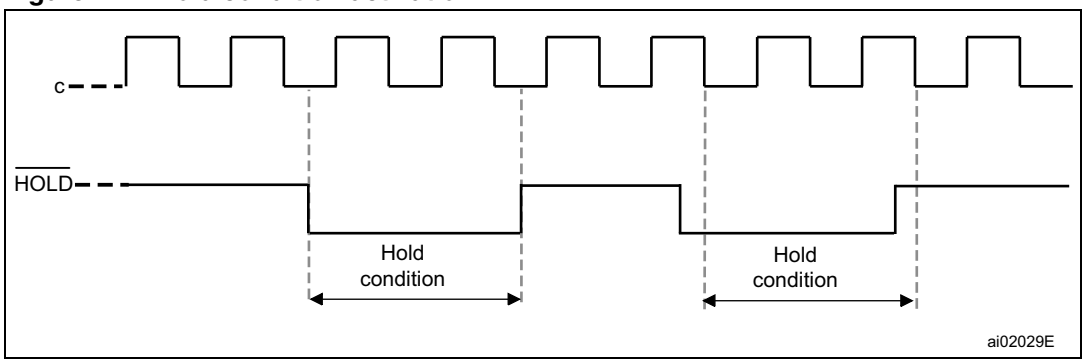
The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if required to reset any processes that had been in progress.[(a)(b)]

Figure 7. Hold condition activation



The Hold condition starts when the Hold (HOLD) signal is driven low when Serial Clock (C) is already low (as shown in *Figure 7*).

a. This resets the internal logic, except the WEL and WIP bits of the Status Register.

b. In the specific case where the device has shifted in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the Write cycle of this decoded command.

The Hold condition ends when the Hold (HOLD) signal is driven high when Serial Clock (C) is already low.

Figure 7 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

5.4 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

5.5 Data protection and protocol control

The device features the following data protection mechanisms:

- Before accepting the execution of the Write and Write Status Register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit.
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points should be noted in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 2. Write-protected block size

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	6000h - 7FFFh
1	0	Upper half	4000h - 7FFFh
1	1	Whole memory	0000h - 7FFFh

6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device automatically deselects itself.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. M95256-D instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
Read Identification Page	Reads the page dedicated to identification.	1000 0011(1)
Write Identification Page	Writes the page dedicated to identification.	1000 0010(1)
Read Lock Status	Reads the lock status of the Identification Page.	1000 0011(2)
Lock ID	Locks the Identification page in read-only mode.	1000 0010(2)

1. Address bit A10 must be 0, all other address bits are Don't Care.
2. Address bit A10 must be 1, all other address bits are Don't Care.

Table 5. Address range bits

Address significant bits	A14-A0(1)

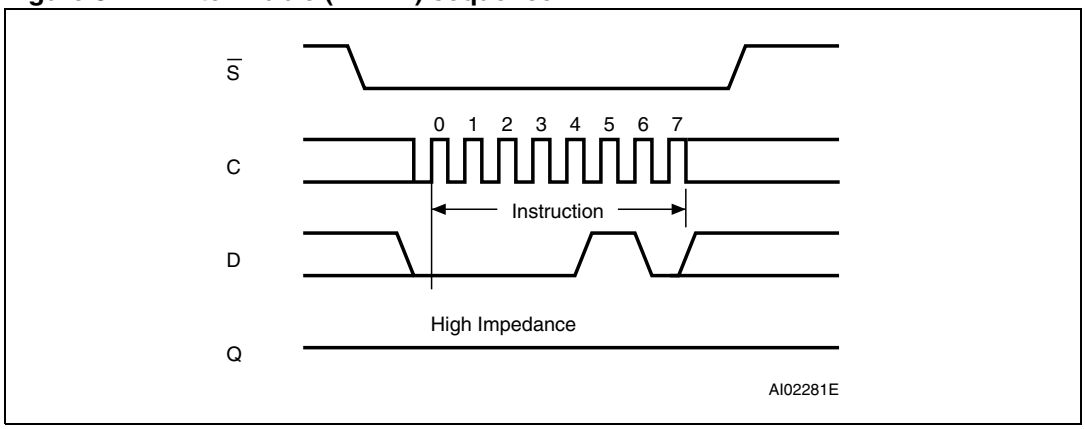
1. Upper MSBs are Don’t Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 8. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

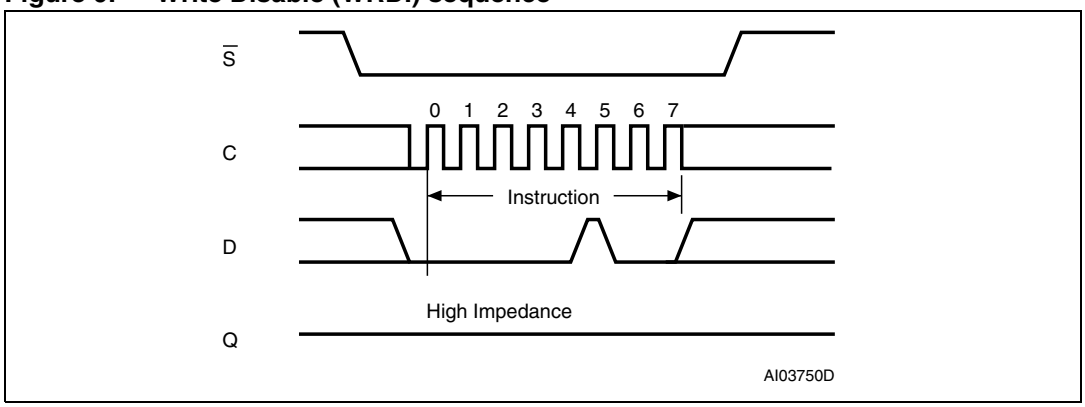
As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

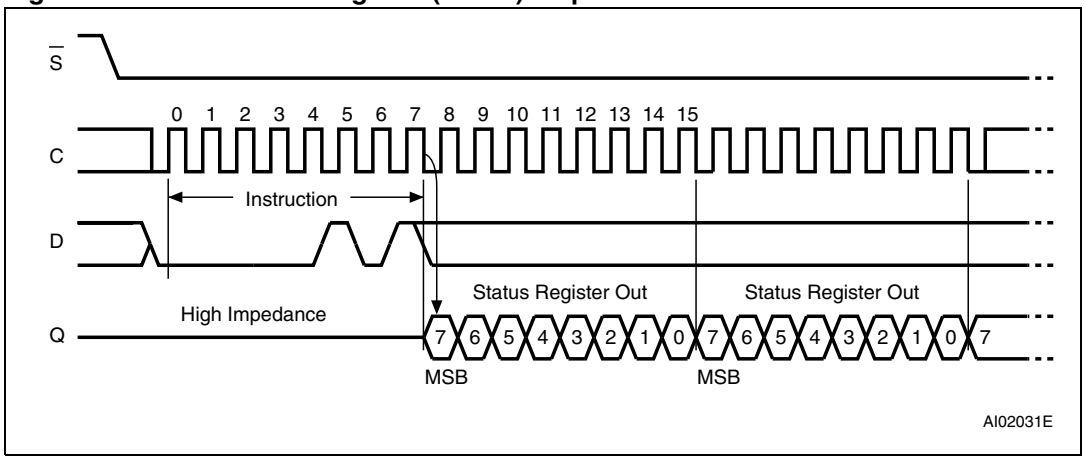
Figure 9. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction is used to read the Status Register. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

Figure 10. Read Status Register (RDSR) sequence



The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset, and no Write or Write Status Register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Write (WRITE) instruction completion

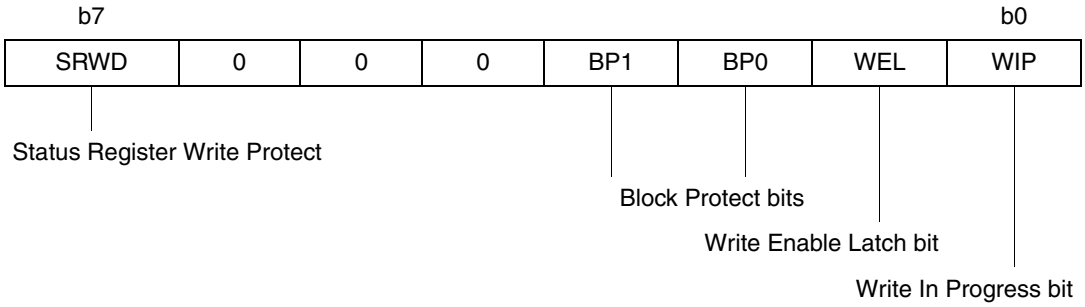
6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non volatile. They define the size of the area to be software-protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 2*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal enable the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 6. Status Register format



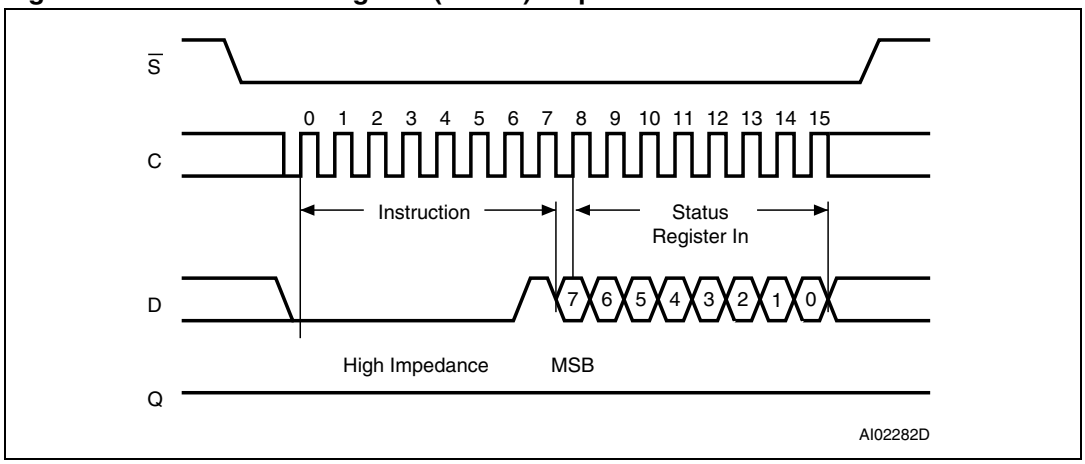
6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction is used to write new values to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in *Figure 11*.

Figure 11. Write Status Register (WRSR) sequence



Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed Write cycle that takes t_W to complete (as specified in AC tables under *Section 9: DC and AC parameters*).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle t_W, and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the Write cycle t_W.

The Write Status Register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in *Table 2*.
- The SRWD (Status Register Write Disable) bit, in accordance with the signal read on the Write Protect pin ($\overline{W}$), enables the user to set or reset the Write protection mode of the Status Register itself, as defined in *Table 7*. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 7. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status Register is writable (if the WREN instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status Register is Hardware write-protected. The values in the BP1 and BP0 bits cannot be changed.	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register. See *Table 2*.

The protection features of the device are summarized in *Table 7*.

When the Status Register Write Disable (SRWD) bit in the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ($\overline{W}$) input pin.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases should be considered, depending on the state of the Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are Software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the Write Protect ($\overline{W}$) input pin low,
- or driving the Write Protect ($\overline{W}$) input pin low after setting the SRWD bit.

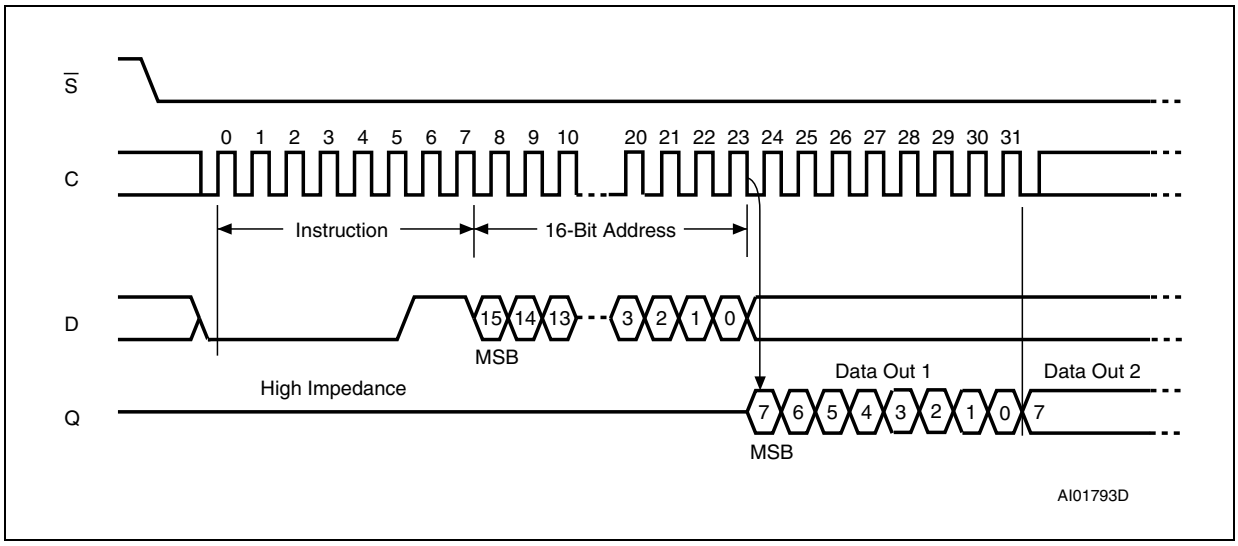
Once the Hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the Write Protect ($\overline{W}$) input pin.

If the Write Protect ($\overline{W}$) input pin is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

6.5 Read from Memory Array (READ)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

Figure 12. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 5*, the most significant address bits are Don't Care.

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is incremented automatically, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

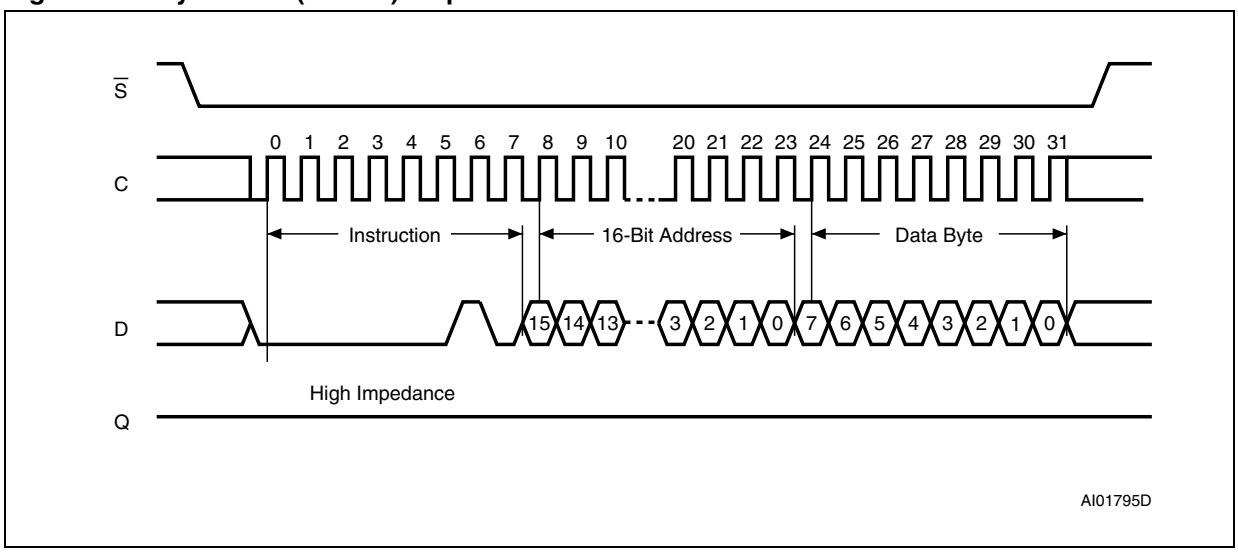
The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 13*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ($\overline{S}$) rising edge, continues for a period t_W (as specified in AC characteristics in *Section 9: DC and AC parameters*), at the end of which the Write in Progress (WIP) bit is reset to 0.

Figure 13. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 5*, the most significant address bits are Don't Care.

In the case of *Figure 13*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 14*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

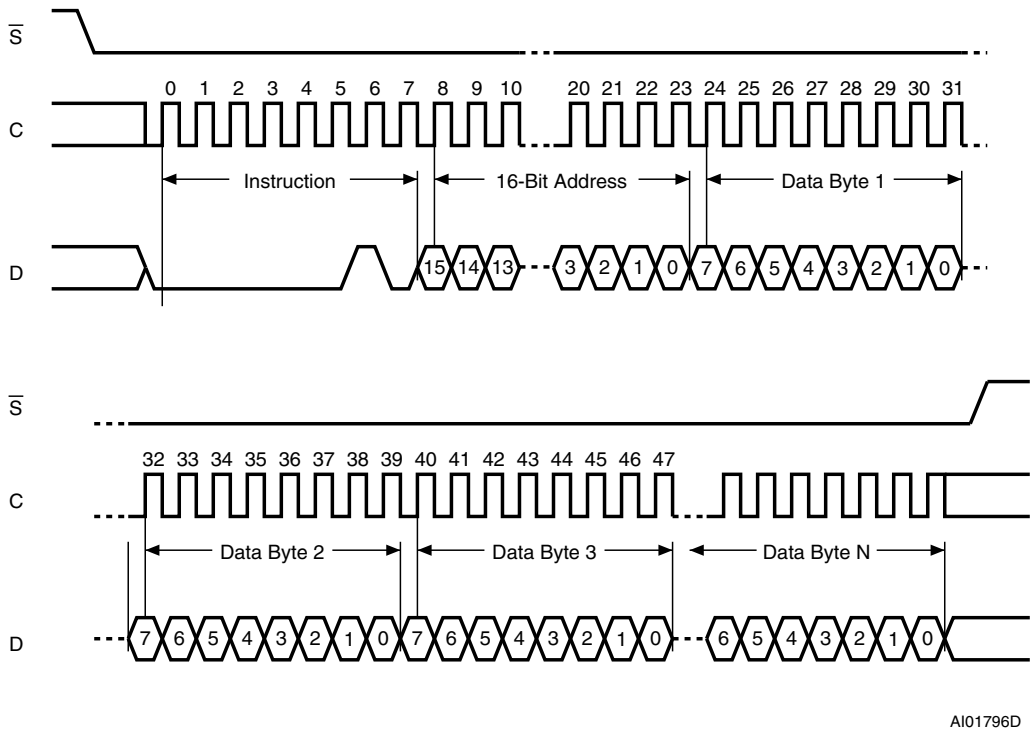
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over" occurs. In case of roll-over, the bytes exceeding the page size are overwritten from location 0 of the same page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before),
- if a Write cycle is already in progress,
- if the device has not been deselected, by driving high Chip Select ($\overline{S}$), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 14. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 5*, the most significant address bits are Don't Care.

6.6.1 Cycling with Error Correction Code (ECC)

M95256 and M95256-D devices offer an Error Correction Code (ECC) logic. The ECC is an internal logic function which is transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[c]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[c]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in *Table 14*.

c. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

6.7 Read Identification Page (available only in M95256-D devices)

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

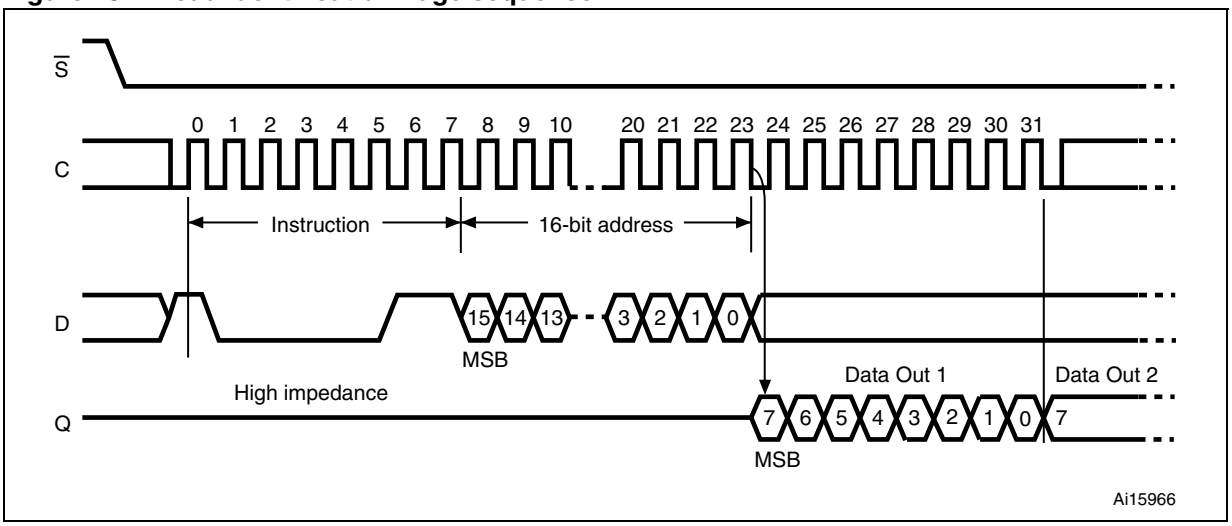
Reading this page is achieved with the Read Identification Page instruction (see *Table 4*). The Chip Select signal ($\overline{S}$) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). Address bit A10 must be 0, upper address bits are Don't Care, and the data byte pointed to by the lower address bits [A5:A0] is shifted out on Serial Data Output (Q). If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

The number of bytes to read in the ID page must not exceed the page boundary, otherwise unexpected data is read (e.g.: when reading the ID page from location 24d, the number of bytes should be less than or equal to 40d, as the ID page boundary is 64 bytes).

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 15. Read Identification Page sequence

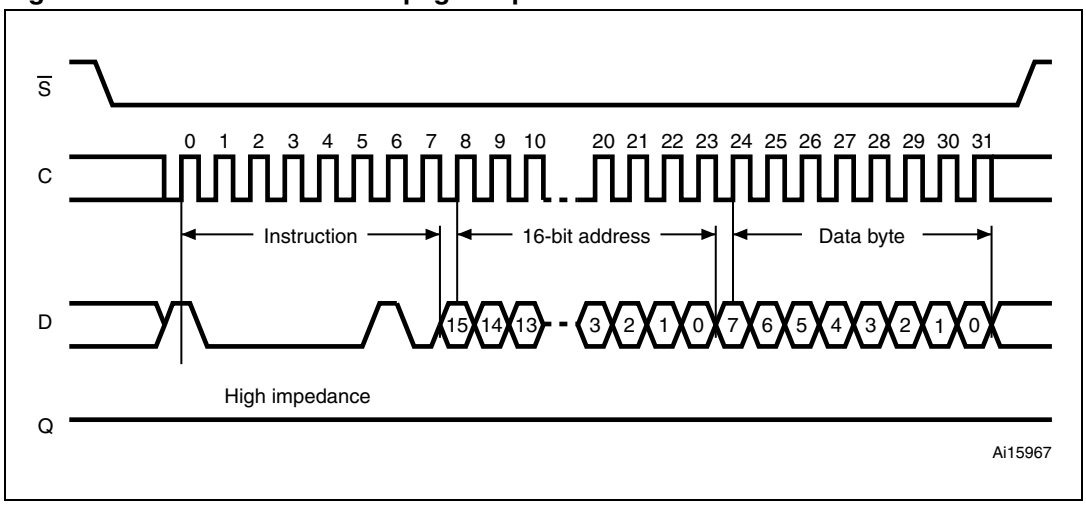


6.8 Write Identification Page (available only in M95256-D devices)

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

Writing this page is achieved with the Write Identification Page instruction (see *Table 4*). The Chip Select signal ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in on Serial Data Input (D). Address bit A10 must be 0, upper address bits are Don't Care, the lower address bits [A5:A0] address bits define the byte address inside the identification page. The instruction sequence is shown in *Figure 16*.

Figure 16. Write identification page sequence

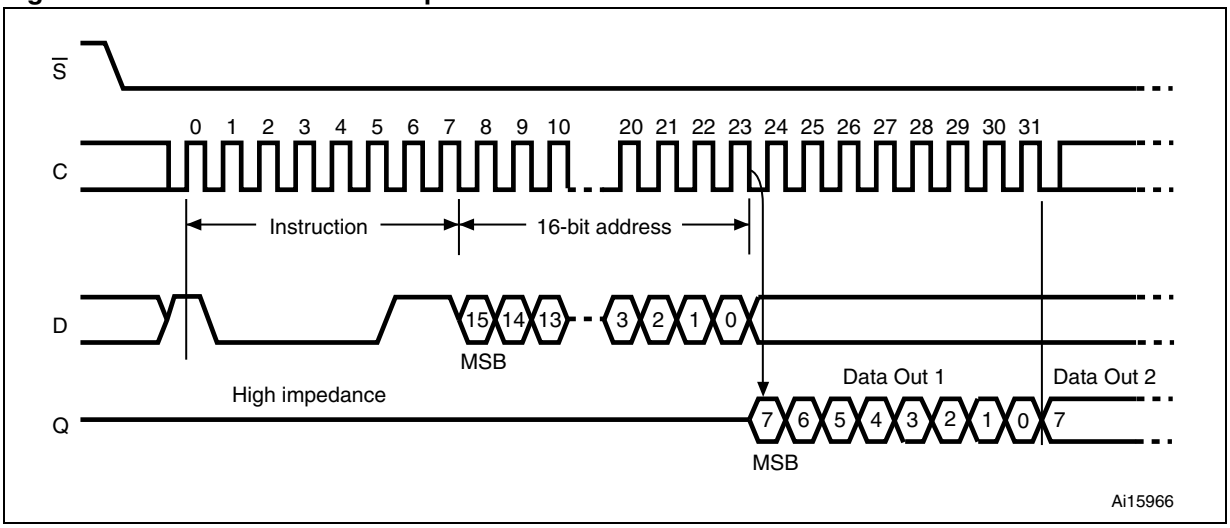


6.9 Read Lock Status (available only in M95256-D devices)

The Read Lock Status instruction (see *Table 4*) is used to check whether the Identification Page is locked or not in Read-only mode. The Read Lock Status sequence is defined with the Chip Select ($\overline{S}$) first driven low. The bits of the instruction byte and address bytes are then shifted in on Serial Data Input (D). Address bit A10 must be 1, all other address bits are Don't Care. The Lock bit is the LSB (least significant bit) of the byte read on Serial Data Output (Q). It is at “1” when the lock is active and at “0” when the lock is not active. If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving Chip Select ($\overline{S}$) high.

The instruction sequence is shown in *Figure 17*.

Figure 17. Read Lock Status sequence



6.10 Lock ID (available only in M95256-D devices)

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed.

The Lock ID instruction is issued by driving Chip Select ($\overline{S}$) low, sending the instruction code, the address and a data byte on Serial Data Input (D), and driving Chip Select ($\overline{S}$) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

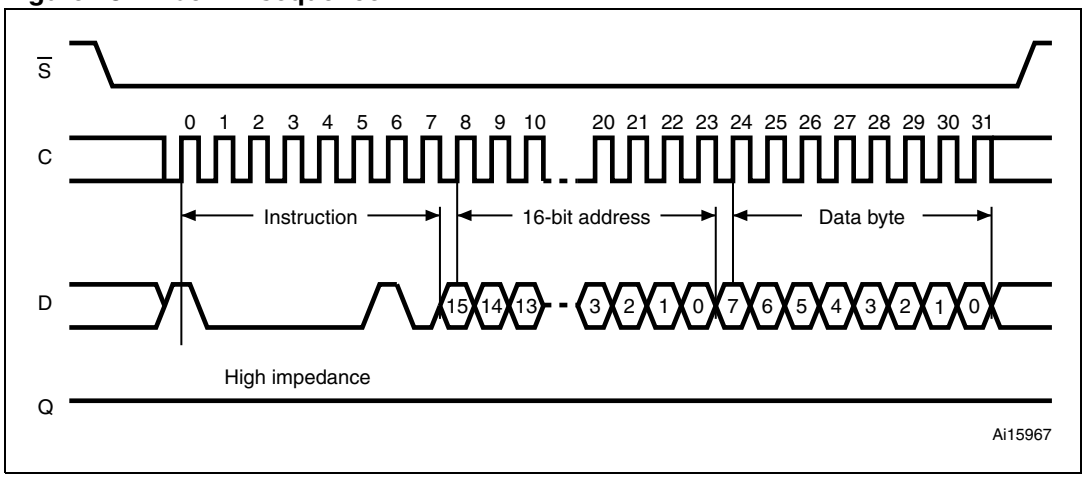
Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Lock ID instruction is not executed.

Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is t_W (as specified in AC characteristics in *Section 9: DC and AC parameters*). The instruction sequence is shown in *Figure 18*.

The instruction is discarded, and is not executed, under the following conditions:

- If a Write cycle is already in progress,
- If the Block Protect bits (BP1,BP0) = (1,1),
- If a rising edge on Chip Select (S) happens outside of a byte boundary.

Figure 18. Lock ID sequence



7 Power-up and delivery state

7.1 Power-up state

After power-up, the device is in the following state:

- Standby power mode,
- deselected (after power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started),
- not in the Hold condition,
- the Write Enable Latch (WEL) is reset to 0,
- Write In Progress (WIP) is reset to 0.

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set to all 1s (each byte = FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 8* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		5	mA
V_{ESD}	Electrostatic discharge voltage (human body model)(2)		4000(3)	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), with the ST ECOPACK® 7191395 specification, and with the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).
3. V_{ESD} is 3000 V (max) for the M95256 identified by process letters KA.

9 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 9. Operating conditions (M95256-W, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Operating conditions (M95256-R and M95256-DR, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. Operating conditions (M95256-DF, device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30 or 100(1)		pF
	Input rise and fall times		25	ns
	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

1. 100 pF when the clock frequency f_C is less than 10 MHz, 30 pF when the clock frequency f_C is equal to or greater than 10 MHz.

Figure 19. AC measurement I/O waveform

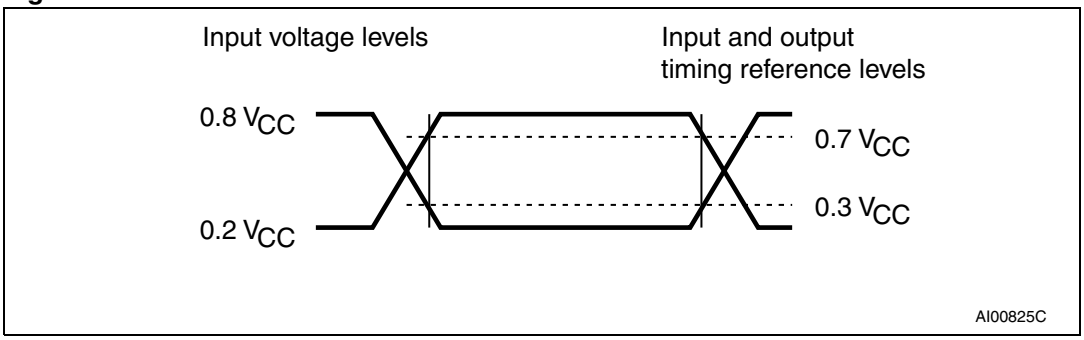


Table 13. Capacitance

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz.

Table 14. Cycling performance by groups of four bytes

Symbol	Parameter(1)	Test conditions	Min.	Max.	Unit
Ncycle	Write cycle endurance(2)	TA ≤ 25 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)		4,000,000	Write cycle(3)
		TA = 85 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)		1,200,000	

1. Cycling performance for products identified by process letters KB.
2. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.
3. A Write cycle is executed when either a Page Write, a Byte Write, a WRSR, a WRID or an LID instruction is decoded. When using the Byte Write, the Page Write or the WRID instruction, refer also to *Section 6.6.1: Cycling with Error Correction Code (ECC)*.

Table 15. Memory cell data retention

Parameter	Test conditions	Min.	Unit
Data retention(1)	TA = 55 °C	200	Year

1. For products identified by process letters KB. The data retention behavior is checked in production. The 200-year limit is defined from characterization and qualification results.

Table 16. DC characteristics (M95256-W, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC}= 2.5 V, C = 0.1 V_{CC}/0.9 V_{CC} at 5 MHz, Q = open		3(1)	mA
		V_{CC}= 2.5 V, C = 0.1 V_{CC}/0.9 V_{CC} at 10 MHz, Q = open		2(2)	
		V_{CC}= 5.5 V, C = 0.1 V_{CC}/0.9 V_{CC} at 5 MHz, Q = open		5(1)	
		V_{CC}= 5.5 V, C = 0.1 V_{CC}/0.9 V_{CC} at 20 MHz, Q = open		5(3)	
I_{CC0}(4)	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$, 2.5 V < V_{CC} < 5.5 V		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5.5 V, $V_{IN} = V_{SS}$ or V_{CC},		3(5)	µA
		$\overline{S} = V_{CC}$, V_{CC} = 2.5 V, $V_{IN} = V_{SS}$ or V_{CC},		2(5)	
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V and I_{OL} = 1.5 mA or V_{CC} = 5 V and I_{OL} = 2 mA		0.4	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V and I_{OH} = –0.4 mA or V_{CC} = 5 V and I_{OH} = –2 mA	0.8 V_{CC}		V

1. For previous products identified with process letter A.
2. 4 mA at 10 MHz and 3 mA at 5 MHz for M95256 previous devices identified by process letter A.
3. For the M95256 devices identified by process letter K.
4. Characterized only, not tested in production.
5. 5 µA for M95256 previous devices identified by process letter A.

Table 17. DC characteristics (M95256-R, M95256-DR, device grade 6)

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1 V_{CC} or 0.9 V_{CC}, at 2 MHz, Q = open		1(2)	mA
		V_{CC} = 1.8 V, C = 0.1 V_{CC} or 0.9 V_{CC}, at 5 MHz, Q = open		2(3)	
I_{CC0}(4)	Supply current (Write)	V_{CC} = 1.8 V, during t_W, $\overline{S} = V_{CC}$		3	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1(5)	µA
V_{IL}	Input low voltage	1.8 V ≤V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage	1.8 V ≤V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

1. If the application uses the M95256-R and M95256-DR devices at 2.5 V ≤V_{CC} ≤5.5 V and –40 °C ≤T_A ≤+85 °C, please refer to *Table 16: DC characteristics (M95256-W, device grade 6)*, rather than to the above table.
2. Value tested only for previous M95256 devices identified by process letter A.
3. Only the M95256 devices identified by process letter K.
4. Characterized only, not tested in production.
5. 3 µA for previous M95256 devices identified by process letter A.

Table 18. DC characteristics (M95256-DF, device grade 6)

Symbol	Parameter	Test conditions(1)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, C = 0.1 V_{CC} or 0.9 V_{CC}, at 5 MHz, Q = open		2	mA
I_{CC0}(2)	Supply current (Write)	V_{CC} = 1.7 V, during t_W, $\overline{S} = V_{CC}$		3	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 1.7 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	µA
V_{IL}	Input low voltage	1.7 V ≤V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage	1.7 V ≤V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.7 V		0.3	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA, V_{CC} = 1.7 V	0.8 V_{CC}		V

1. If the application uses the M95256-DF devices at 2.5 V ≤V_{CC} ≤5.5 V and –40 °C ≤T_A ≤+85 °C, please refer to *Table 16: DC characteristics (M95256-W, device grade 6)*, rather than to the above table.
2. Characterized only, not tested in production.

Table 19. AC characteristics (M95256-W, device grade 6)

Test conditions specified in *Table 9* and *Table 12*			Previous[1] and new products C_L = 100 pF		New products[2] C_L = 30 pF				Unit
					$V_{cc} \geq 2.5V$		$V_{cc} \geq 4.5V$		
Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency	D.C.	5	D.C.	10	D.C.	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		30		15		ns
t_{CH} (3)	t_{CLH}	Clock high time	90		40		20		ns
t_{CL} (3)	t_{CLL}	Clock low time	90		40		20		ns
t_{CLCH} (3)	t_{RC}	Clock rise time		1		2		2	µs
t_{CHCL} (3)	t_{FC}	Clock fall time		1		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	30		10		10		ns
t_{HHCH}		Clock low hold time after HOLD not active	70		30		15		ns
t_{HLCH}		Clock low hold time after HOLD active	40		30		15		ns
t_{CLHL}		Clock low setup time before HOLD active	0		0		0		ns
t_{CLHH}		Clock low setup time before HOLD not active	0		0		0		ns
t_{SHQZ} (4)	t_{DIS}	Output disable time		100		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		60		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		0		ns
t_{QLQH} (4)	t_{RO}	Output rise time		50		20		10	ns
t_{QHQL} (4)	t_{FO}	Output fall time		50		20		10	ns
t_{HHQV}	t_{LZ}	HOLD high to output valid		50		40		20	ns
t_{HLQZ} (4)	t_{HZ}	HOLD low to output High-Z		100		40		20	ns
t_W	t_{WC}	Write time		5		5		5	ms

1. Previous products are identified by process letters AB.
2. New products are M95256 devices identified by process letter K.
3. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$.
4. Characterized only, not tested in production.

Table 20. AC characteristics (M95256-R, M95256-DR device grade 6)

Test conditions specified in *Table 10* and *Table 12*											
Symbol	Alt.	Parameter	Previous products (1)		New products (2)						Unit
					$V_{CC} \geq 1.8V$		$V_{CC} \geq 2.5V$		$V_{CC} \geq 4.5V$		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency		2		5		10		20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	200		60		30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	200		60		30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	200		90		40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	200		60		30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	200		60		30		15		ns
t_{CH} (3)	t_{CLH}	Clock high time	200		80		40		20		ns
t_{CL} (3)	t_{CLL}	Clock low time	200		80		40		20		ns
t_{CLCH} (4)	t_{RC}	Clock rise time		1		2		2		2	µs
t_{CHCL} (4)	t_{FC}	Clock fall time		1		2		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	40		20		10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	50		20		10		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	140		60		30		15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	90		60		30		15		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		0		0		0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		0		0		0		ns
t_{SHQZ} (4)	t_{DIS}	Output disable time		250		80		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		150		80		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		0		0		ns
t_{QLQH} (4)	t_{RO}	Output rise time		100		20		20		10	ns
t_{QHQL} (4)	t_{FO}	Output fall time		100		20		20		10	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		100		80		40		20	ns
t_{HLQZ} (4)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		250		80		40		20	ns
t_W	t_{WC}	Write time		5		5		5		5	ms

1. Previous products are identified by process letters AB.
2. New products are the M95256 devices identified by process letter K.
3. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$.
4. Characterized only, not tested in production.

Table 21. AC characteristics (M95256-DF device grade 6)

Test conditions specified in *Table 10* and *Table 12*[1]									
		Parameter	$V_{CC} \geq 1.7$ V		$V_{CC} \geq 2.5$ V		$V_{CC} \geq 4.5$ V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency		5		10		20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		30		15		ns
t_{CH} (2)	t_{CLH}	Clock high time	80		40		20		ns
t_{CL} (3)	t_{CLL}	Clock low time	80		40		20		ns
t_{CLCH} (3)	t_{RC}	Clock rise time		2		2		2	µs
t_{CHCL} (4)	t_{FC}	Clock fall time		2		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	20		10		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		30		15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		30		15		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		0		0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		0		0		ns
t_{SHQZ} (4)	t_{DIS}	Output disable time		80		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		80		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		0		ns
t_{QLQH} (4)	t_{RO}	Output rise time		20		20		10	ns
t_{QHQL} (4)	t_{FO}	Output fall time		20		20		10	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80		40		20	ns
t_{HLQZ} (4)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		80		40		20	ns
t_W	t_{WC}	Write time		5		5		5	ms

1. Preliminary data.
2. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$.
3. Characterized only, not tested in production.

Figure 20. Serial input timing

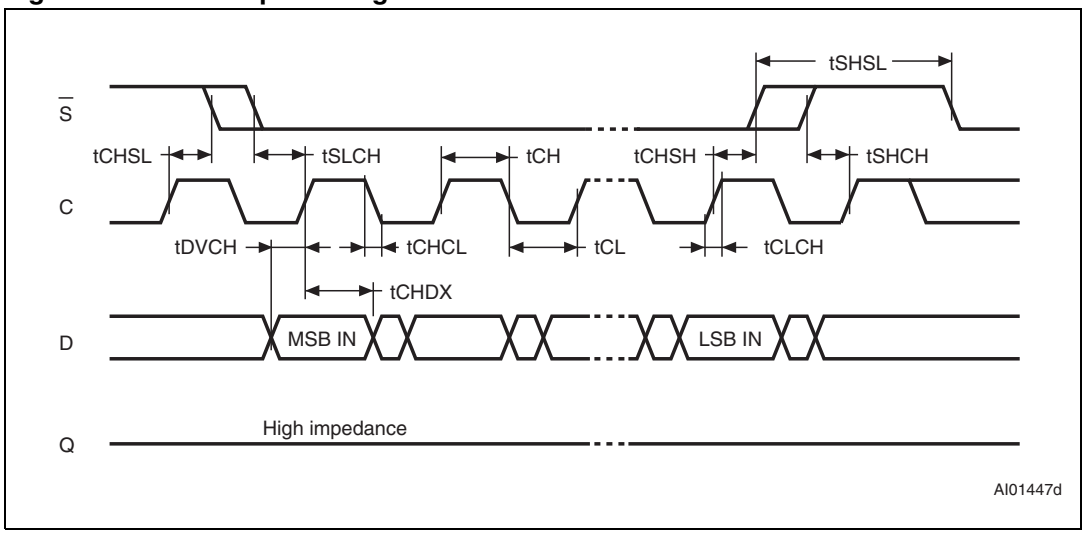


Figure 21. Hold timing

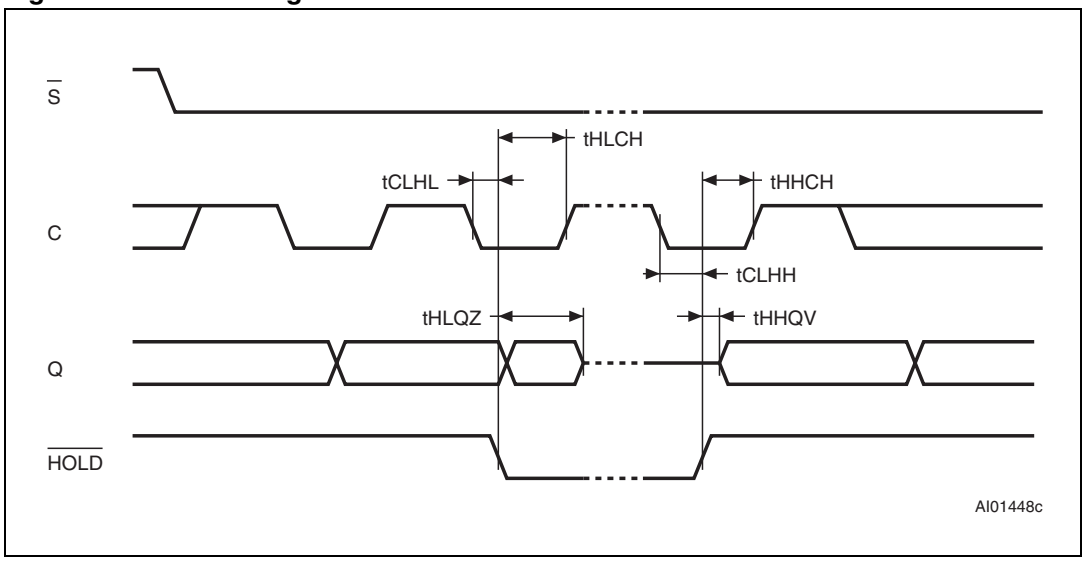
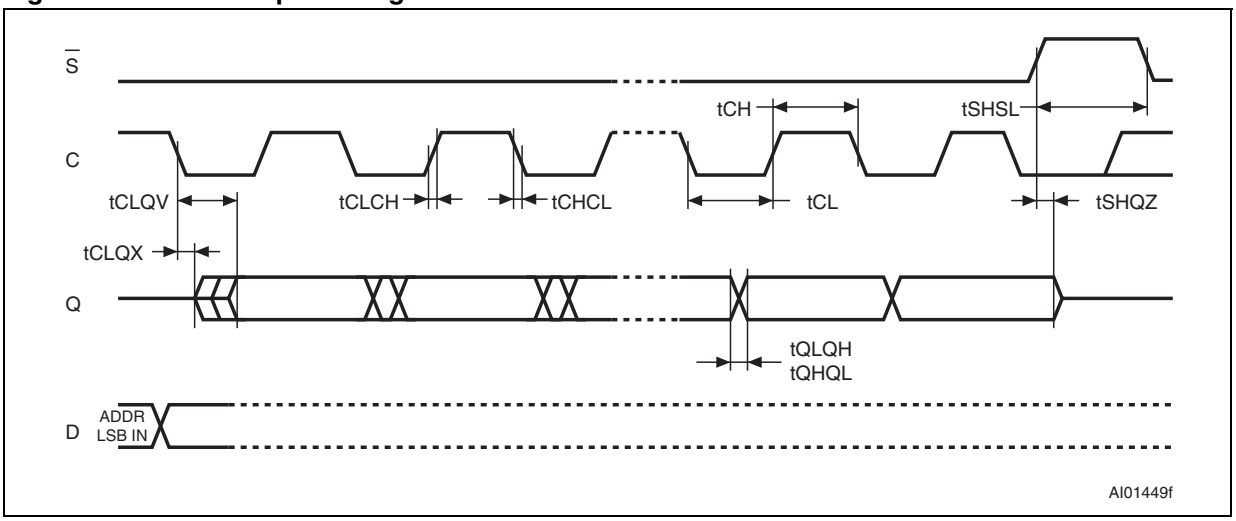


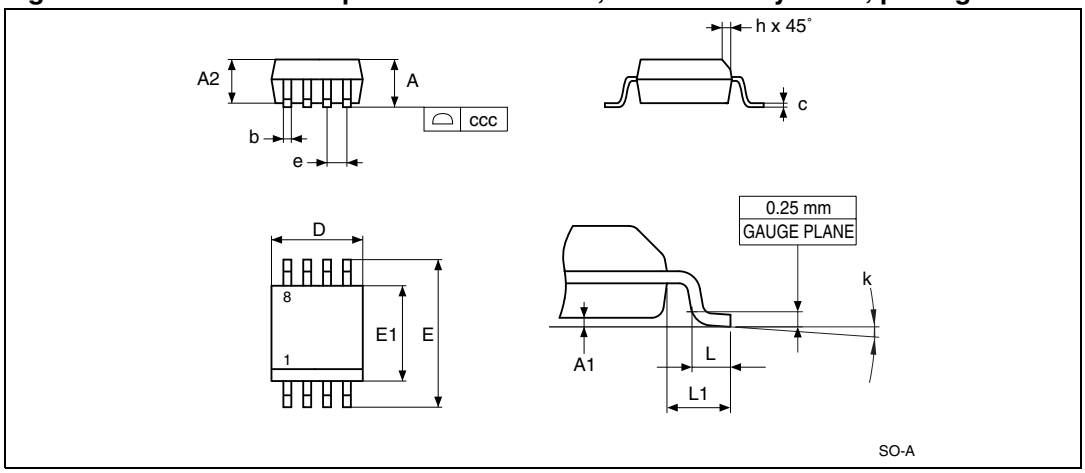
Figure 22. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 23. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



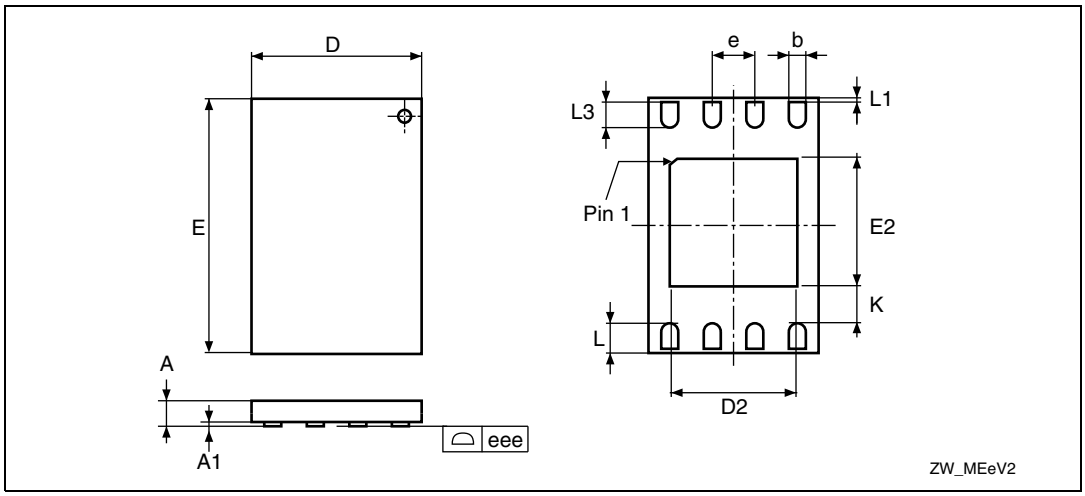
1. Drawing is not to scale.

Table 22. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	-	-	0.0500	-	-
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 24. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



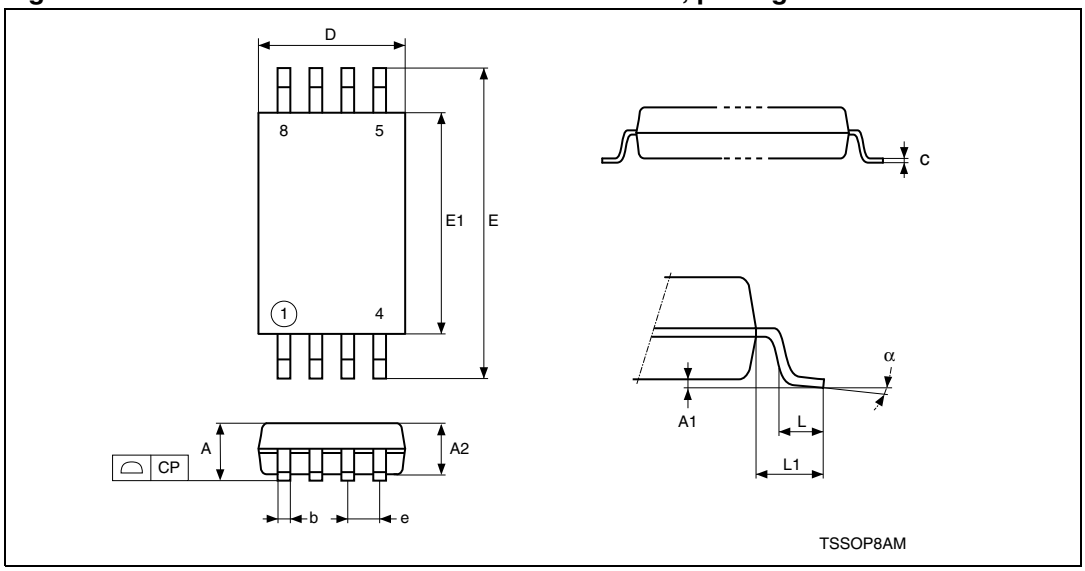
1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 23. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 25. TSSOP8 – 8-lead thin shrink small outline, package outline



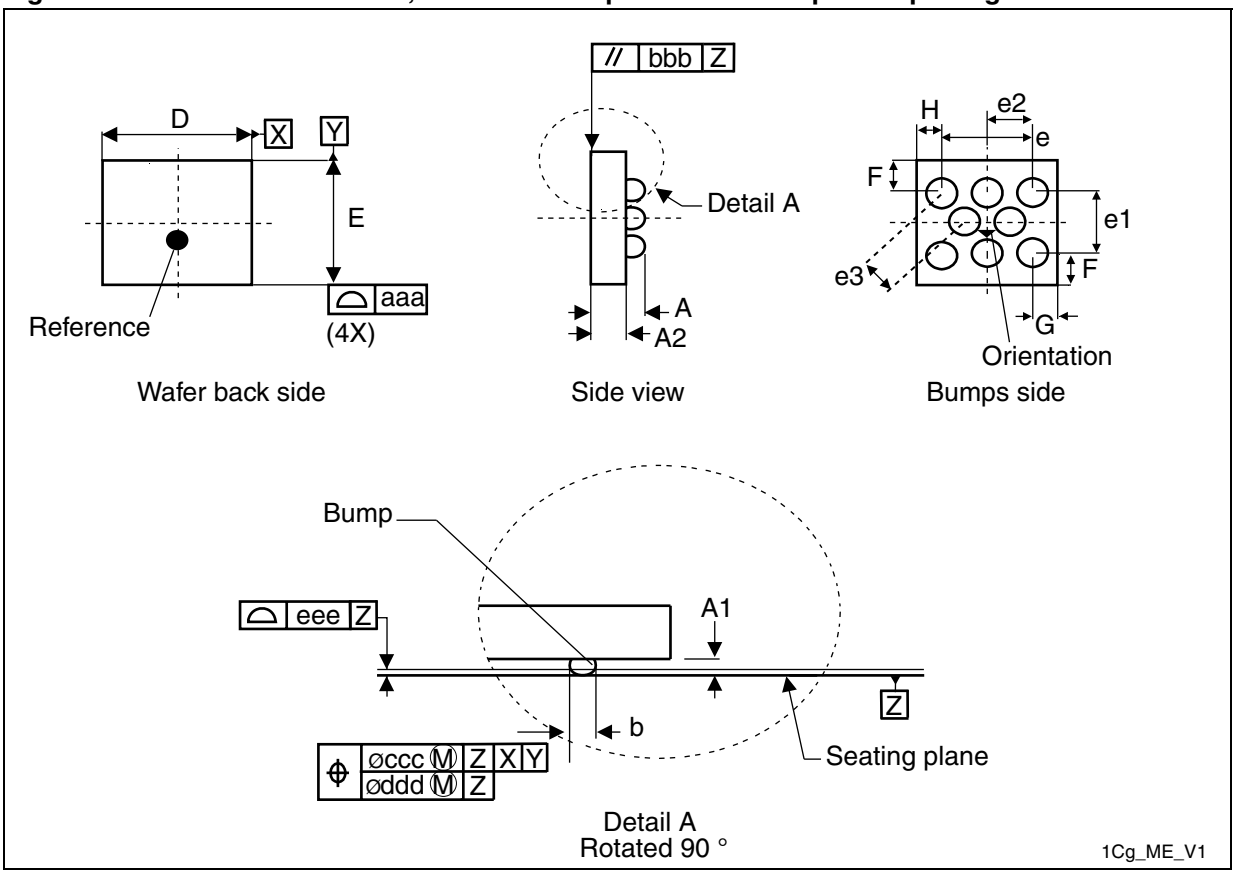
1. Drawing is not to scale.

Table 24. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 26. M95256-DFCS6TP/K, WLCSP 8-bump wafer-level chip scale package outline



1. Drawing is not to scale.

Table 25. M95256-DFCS6TP/K, WLCSP 8-bump wafer-level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.540	0.500	0.580	0.0213	0.0197	0.0228
A1	0.190			0.0075		
A2	0.350			0.0138		
b	0.270			0.0106		
D	1.271		1.291	0.0500		0.0508
E	1.358		1.378	0.0535		0.0543
e	0.800			0.0315		
e1	0.693			0.0273		
e2	0.400			0.0157		
e3	0.400			0.0157		
F	0.333			0.0131		
G	0.235			0.0093		
H	0.236			0.0093		
N (number of terminals)	8			8		
aaa	0.11			0.0043		
bbb	0.11			0.0043		
ccc	0.11			0.0043		
ddd	0.06			0.0024		
eee	0.06			0.0024		

1. Values in inches are converted from mm and rounded to four decimal digits.

11 Part numbering

Table 26. Ordering information scheme

Example: M95256 W MN 6 T P /A

Device type

M95 = SPI serial access EEPROM

Device function

256 = 256 Kbit

256-D = 256 Kbit plus Identification page

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

F = V_{CC} = 1.7 to 5.5 V

Package

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MC = UFDFPN8 (MLP8)

CS = WLCSP

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

G or P = RoHS compliant and halogen-free
(ECOPACK®)

Process(1)

/A, /AB or /K= Manufacturing technology code

1. The process letters apply to WLCSP devices only. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

12 Revision history

Table 27. Document revision history

Date	Revision	Changes
17-Nov-1999	2.1	New -V voltage range added (including the tables for DC characteristics, AC characteristics, and ordering information).
07-Feb-2000	2.2	New -V voltage range extended to M95256 (including AC characteristics, and ordering information).
22-Feb-2000	2.3	tCLCH and tCHCL, for the M95xxx-V, changed from 1µs to 100ns
15-Mar-2000	2.4	-V voltage range changed to 2.7-3.6V
29-Jan-2001	2.5	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Illustrations and Package Mechanical data updated
12-Jun-2001	2.6	Correction to header of Table 12B TSSOP14 Illustrations and Package Mechanical data updated Document promoted from Preliminary Data to Full Data Sheet
08-Feb-2002	2.7	Announcement made of planned upgrade to 10 MHz clock for the 5V, –40 to 85°C, range.
09-Aug-2002	2.8	M95128 split off to its own datasheet. Data added for new and forthcoming products, including availability of the SO8 narrow package.
24-Feb-2003	2.9	Omission of SO8 narrow package mechanical data remedied
26-Jun-2003	2.10	-V voltage range removed
21-Nov-2003	3.0	Table of contents, and Pb-free options added. -S voltage range extended to -R. V_{IL}(min) improved to –0.45V
17-Mar-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified
21-Oct-2004	5.0	M95128 datasheet merged back in. Product List summary table added. AEC-Q100-002 compliance. Device Grade information clarified. tHHQX corrected to tHHQV. 10MHz product becomes standard

Table 27. Document revision history (continued)

Date	Revision	Changes
13-Apr-2006	6	M95128 part numbers removed from document. PDIP8 package removed. *Delivery state* paragraph added. *Section 3.8: Operating supply voltage (VCC)* added and information removed below *Section 4: Operating features*. Power up state removed below *Section 6: Delivery state*. *Figure 18: SPI modes supported* modified and *Note 2* added. *Note 1* added to *Table 8*. I_{CC1} specified over the whole V_{CC} range and I_{CC0} added in *Table 14*, *Table 15* and *Table 16*. I_{CC} specified over the whole V_{CC} range in *Table 14*. *Table 17: AC Characteristics (M95256, Device Grade 6)* added. t_{CHHL} and t_{CHHH} replaced by t_{CLHL} and t_{CLHH}, respectively. *Figure 21: Hold timing* modified. *Process* added to *Table 25: Ordering information scheme*. *Note 1* added to *Table 25*. Note 1 removed from *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*. T_A added to *Table 7: Absolute maximum ratings*. Order of sections modified.
15-Oct-2007	7	M95256 with device grade 6 temperature range removed. *Section 3.7: VSS ground* added, *Section 3.8: Operating supply voltage (VCC)* modified. Small text changes. *Section 5.4: Write Status Register (WRSR)*, *Section 5.5: Read from Memory Array (READ)* and *Section 6: Delivery state* updated. Note 2 below *Figure 17: Bus master and memory devices on the SPI bus* removed, replaced by explanatory paragraph. T_{LEAD} added to *Table 7: Absolute maximum ratings*. Test conditions modified for I_{CC0} and I_{CC1}, and V_{IH} min modified in *Table 17: AC characteristics (M95256, device grade 3)*. t_W modified and “preliminary data” note removed in *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*. Blank option removed below Plating technology, process A modified and process V removed in *Table 25: Ordering information scheme*. *Table 26: Available M95256x products (package, voltage range, temperature grade)* added. SO8N and SO8W package specifications updated (see *Section 10: Package mechanical data*). Package mechanical data: inches calculated from mm and rounded to 3 decimal digits.
27-Mar-2008	8	*Section 3.8: Operating supply voltage (VCC)* modified. Small text changes. Frequency corrected *on page 1*. V_{IL} and V_{IH} modified in *Table 16: DC characteristics (M95256-R, M95256-DR, device grade 6)*. AB Process added to *Table 25: Ordering information scheme*.
15-Jul-2008	9	WLCSP package added (see *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* and *Section 10: Package mechanical data*).

Table 27. Document revision history (continued)

Date	Revision	Changes
24-Jun-2010	10	M95080 part number added. Updated *Section 3.8: Operating supply voltage (VCC)* Updated *Section 4.3: Data protection and protocol control* Updated *Section 5.4: Write Status Register (WRSR)* Added note in *Section 5.6: Write to Memory Array (WRITE)* Updated *Table 7: Absolute maximum ratings* Added *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)* Updated *Table 20: AC characteristics (M95256-DR, M95256-R device grade 6)*
07-Sep-2010	11	Updated *Section 1: Description*. Updated *Section 5.7: Read Identification Page (available only in M95256-DR devices)*. Updated *Section 5.8: Write Identification Page*. Updated *Section 5.9: Read Lock Status (available only in M95256-DR devices)*.
12-Nov-2010	12	Updated *Features*. Updated *Section 5.8: Write Identification Page*. Added *Figure 25: TSSOP8 – 8 lead thin shrink small outline, package outline*. Added *Table 23: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, package mechanical data*. Updated *Section 11: Part numbering*. Updated *Table 26: Available M95256x products (package, voltage range, temperature grade)*. Updated *Figure 25*, *Figure 26*.
22-Mar-2011	13	Deleted: – SO8 (MW) picture under *Features* – SO8 (MW) mechanical dimensions Updated: – UFDFPN8 (MB) with UFDFPN8 (MB, MC) picture under *Features* – *Section 5.6.1: ECC (error correction code) and Write cycling* – *Section 7: Connecting to the SPI bus* – *Table 7: Absolute maximum ratings* Process letter K substituted with only concerned products (M95256-D and M95256 in MLP8 package MC).9 (...)

Table 27. Document revision history (continued)

Date	Revision	Changes
22-Mar-2011	13	(...) – Rephrased “test condition” text in: *Table 14: DC characteristics (M95256, device grade 3)* *Table 20: DC characteristics (current M95080-W products)* *Table 16: DC characteristics (M95256-W, device grade 3)* *Table 23: DC characteristics (current and new M95080-R and M95080-DR products)* *Table 18: AC characteristics (M95256, device grade 3)* *Table 31: AC characteristics, M95080-W, device grade 6* *Table 20: AC characteristics (M95256-W, device grade 3)* *Table 36: AC characteristics (M95080-R, M95080-DR device grade 6)* Added: – Caution under *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* – MC = UFDFPN8 package in *Section 11: Part numbering*
20-May-2011	14	Updated: – UFDFPN8 offered in only one package version Added: *– Table 15: Memory cell characteristics*
19-Jul-2011	15	MC package added (UFDFPN8)
23-Nov-2011	16	Updated: – Footnote 3 below *Table 7: Absolute maximum ratings* – Footnotes 1, 2, 4, 5 below *Table 15: DC characteristics (M95256-W, device grade 6)* – Footnotes 1, 2, 3, 5 below *Table 17: DC characteristics (M95256-R, M95256-DR, device grade 6)* – *Table 19: AC characteristics, M95256-W, device grade 6* headings, T_{QLQH} and T_{QHQL} values. One footnote removed and one added – *Table 21: AC characteristics (M95256-DR, M95256-R device grade 6)*, new columns for new pairs of products. Footnote 2 edited.
17-Jan-2012	17	Updated *Figure 25: UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline*.

Table 27. Document revision history (continued)

Date	Revision	Changes
21-Jun-2012	18	Datasheet split into: – M95256-125 datasheet for automotive products (range 3), – M95256-W, M95256-R, M95256-DR, M95256-DF (this datasheet) for standard products (range 6). Added: – 1.7 V device (M95256-DF) Updated: – *Figure 4: Block diagram* – *Table 25: M95256-DFCS6TP/K, WLCSP 8-bump wafer-level chip scale package mechanical data* and *Figure 26: M95256-DFCS6TP/K, WLCSP 8-bump wafer-level chip scale package outline* – Cycling and data retention values (*Table 14* and *Table 15*) Deleted: – UFDFPN8 package rev MB

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