DATA SHEET

PCA8550

4-bit multiplexed/1-bit latched 5-bit I^2C EEPROM

Product specification
Supersedes data of 2000 Aug 30
ICL03 — PC Motherboard ICs; Logic Products Group

2001 Jan 12

Philips
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4-bit multiplexed/1-bit latched 5-bit I²C EEPROM PCA8550

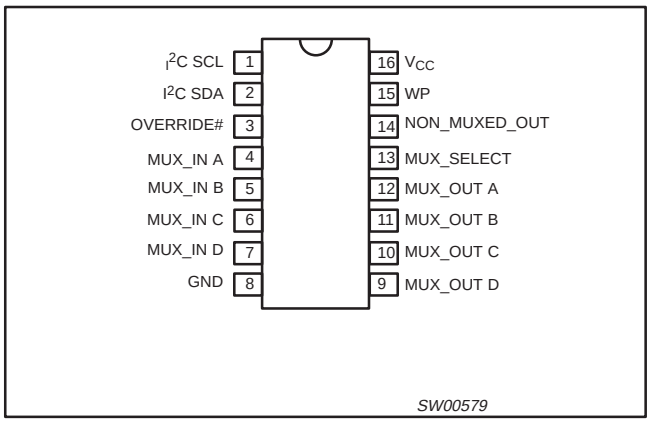
FEATURES

- 4-bit 2-to-1 multiplexer, 1-bit latch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I²C bus
- Write-protect pin enables/disables I²C writes to register
- 2.5 V multiplexed outputs
- 3.3 V non-multiplexed output (latched)
- 5 V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II™ systems

DESCRIPTION

The primary function of the 4-bit 2-to-1 I²C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I²C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An "override" input feature forces all outputs to logic 0.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
16-Pin Plastic SO	0 to +70 °C	PCA8550D	SOT109-1
16-Pin Plastic SSOP	0 to +70 °C	PCA8550DB	SOT338-1
16-Pin Plastic TSSOP	0 to +70 °C	PCA8550PW	SOT403-1

FUNCTIONAL DESCRIPTION

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE# signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I²C bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C bus (described in the next section).

The OVERRIDE#, WP, MUX_IN, and MUX_SELECT signals have internal pullup resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I²C SCL	I²C bus clock
2	I²C SDA	Bi-directional I²C bus data
3	OVERRIDE#	Forces all outputs to logic 0
4	MUX_IN A	External inputs to multiplexer
5	MUX_IN B	
6	MUX_IN C	
7	MUX_IN D	
8	GND	Common ground voltage rail
9	MUX_OUT D	2.5V multiplexed output
10	MUX_OUT C	
11	MUX_OUT B	
12	MUX_OUT A	
13	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
14	NON_MUXED_OUT	TTL-level output from non-volatile memory
15	WP	Non-volatile register write-protect
16	V_{CC}	Positive voltage rail

FUNCTION TABLE

Table 1. Function table

OVERRIDE #	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT[1]
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

NOTE

1. Latched NON_MIXED_OUT state will be the value present on the NON_MUXED_OUT output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

I²C Interface

Communicating with this device is initiated by sending a valid address on the I²C bus. The address format (see FIgure 1) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.

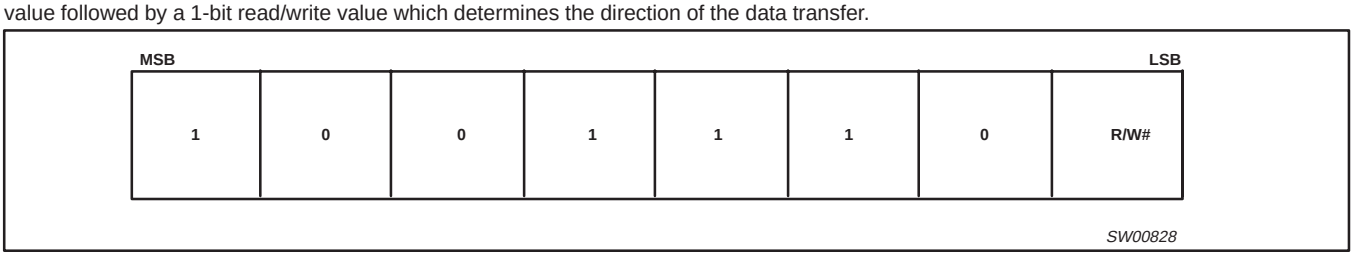


Figure 1. I²C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see FIgure 2) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

NOTE:

1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C bus is powered down or V_{CC} to the component is dropped below normal operating levels.

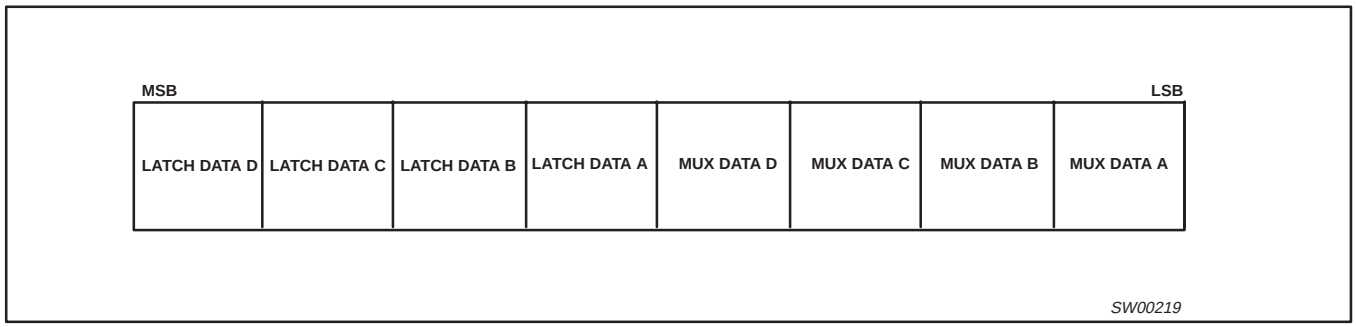
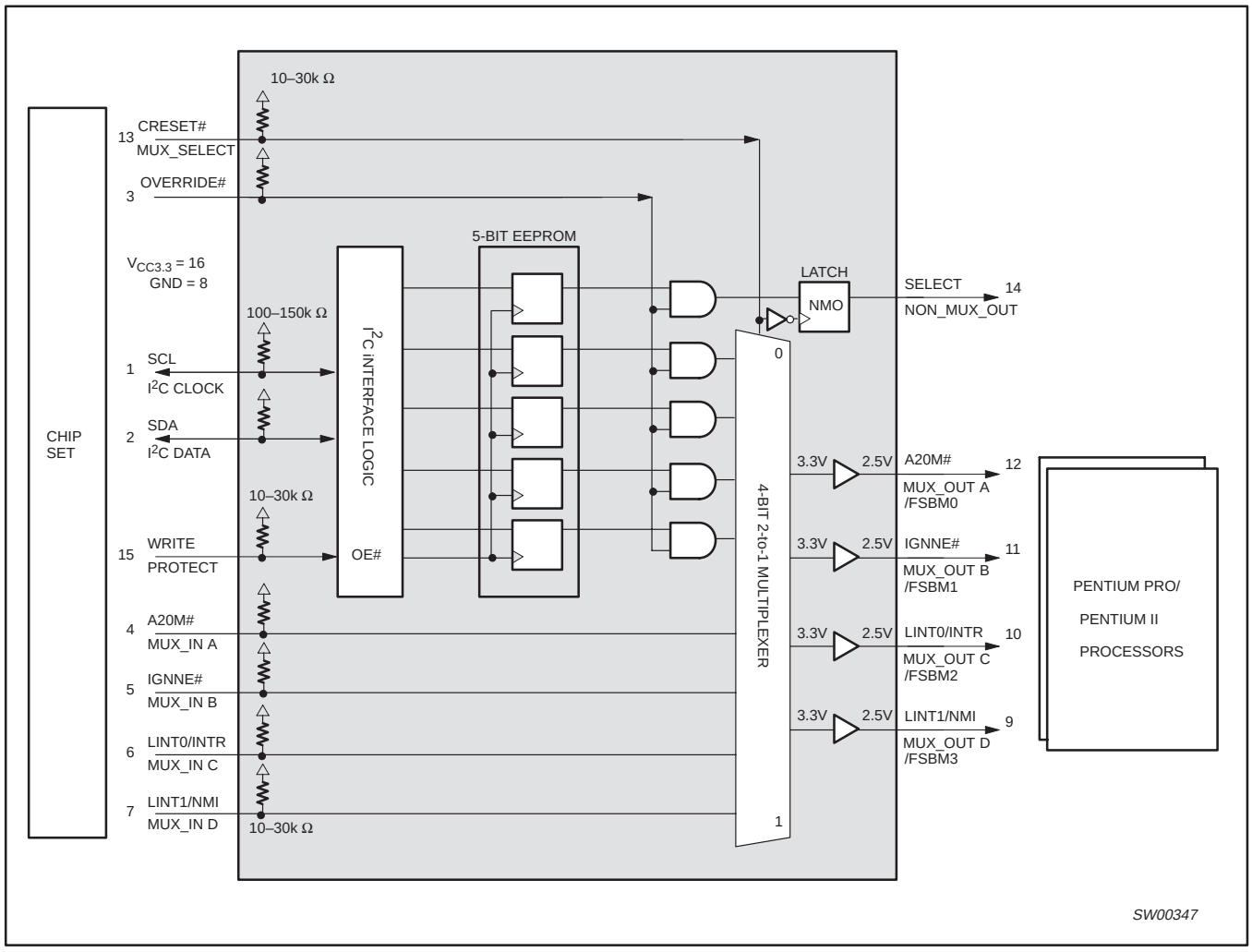


Figure 2. I²C Data Byte

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage	Note 3	–1.5 to V_{CC} +1.5	V
V_{OUT}	DC output voltage	Note 3	–0.5 to V_{CC} +0.5	V
T_{stg}	Storage temperature range		–60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
SCL, SDA	V_{IL} V_{IH} V_{OL}	I_{OL}= 3 mA	–0.5 2.7	0.9 4.0 0.4	V
OVERRIDE#, MUX_IN, MUX_SELECT	V_{IL} V_{IH}		–0.5 2.0	0.8 4.0	V
MUX_OUT, NON_MUXED_OUT	I_{OL} I_{OH}			2.0 –2.0	mA
dt/dv	Input transition rise or fall time		0	10	ns/V
T_A	Operating temperature		0	70	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		Temp = 0°C to +70°C 3.0V < V_{CC} ≤ 3.6V		
		MIN	MAX	
SCL, SDA	V_{OL} I_{OL} (V_{OL} = 0.4 V) I_{OL} (V_{OL} = 0.6 V) I_{IL} (V_{IL} = 0.4 V) I_{IH} (V_{IH} = 2.4 V) V_{HYS}[1]	0 –7 –1.5 0.19	0.6 3.0 6.0 –32 –12	V mA mA µA µA V
OVERRIDE#, WP, MUX_SELECT	I_{IL} I_{IH}	–86 –20	–267 –100	µA
MUX A ⇒ D	I_{IL} (V_{IL} = 0.4 V) I_{IH} (V_{IH} = 2.4 V)	–0.72 –0.166	–2.0 –0.75	mA
MUX_OUT	V_{OL} (I_{OL} = 100 µA) V_{OL} (I_{OL} = 2.0 mA) V_{OH} (I_{OH} = –100 µA) V_{OH} (I_{OH} = –1.0 mA)	–0.3 –0.3 2.0 1.7	0.4 0.7 2.625 2.625	V
NON_MUXED_OUT	V_{OL} (I_{OL} = 100 µA) V_{OL} (I_{OL} = 2.0 mA) V_{OH} (I_{OH} = –100 µA) V_{OH} (I_{OH} = –2.0 mA)	–0.5 –0.5 2.4 2.0	0.4 0.7 3.6 3.6	V
I_{CC}	Quiescent supply current (V_{CC} = 3.3 V) V_I = 0 V to V_{CC}		10	mA
I_{CC}	Quiescent supply current V_I = V_{CC}		500	µA
C_{IN}	All inputs		10	pF
	ESD protection	2.0		KV
	Input diode clamp voltage	–1.5		V

NOTES:
1. V_{HYS} is the hysteresis of Schmitt-Trigger inputs
2. Human body model

NON-VOLATILE STORAGE SPECIFICATIONS

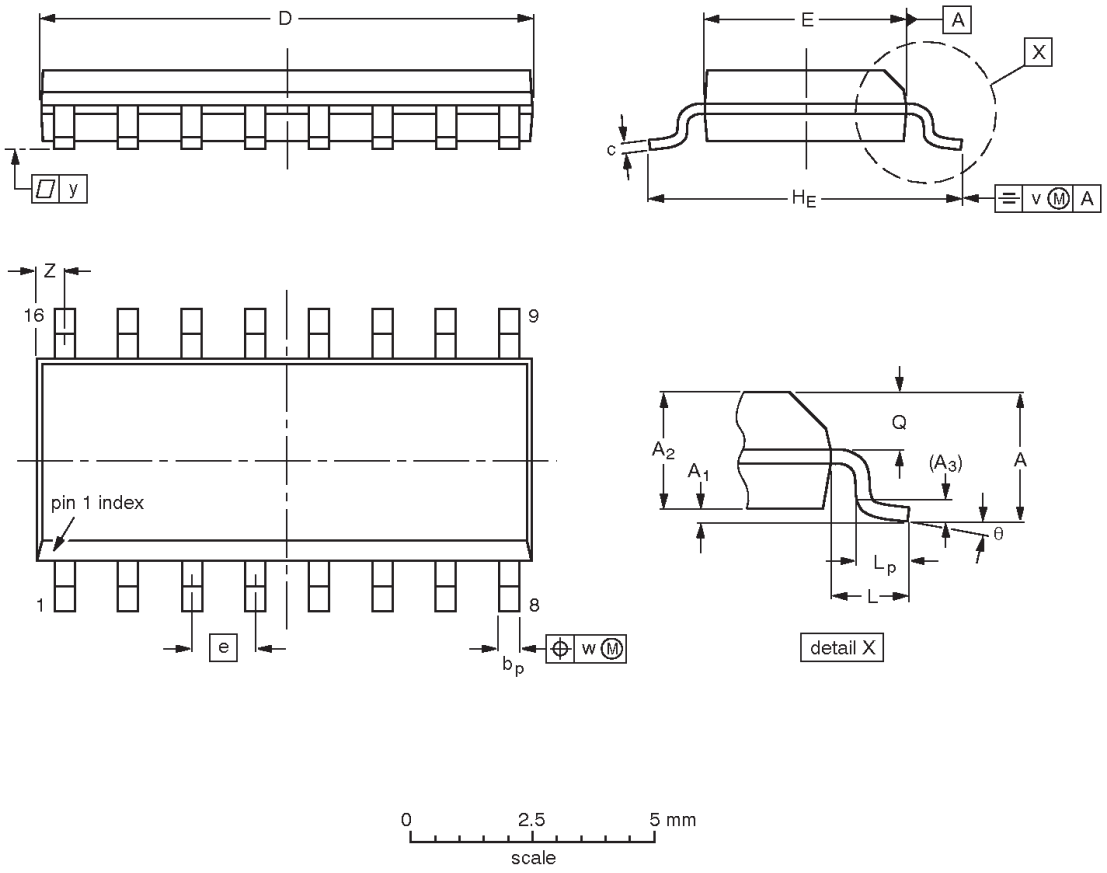
Parameter	Specification
Memory cell data retention	10 years min
Number of memory cell write cycles	3,000 cycles min

AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{MPD}	Mux input to output propagation delay		20.0	ns
T_{SOV}	MUX_SELECT to output valid		22	ns
T_{OVN}	OVERRIDE# to NON_MUX output delay		15.0	ns
T_{OVM}	OVERRIDE# to mux output delay		25.0	ns
T_R	Output rise time	1.0	3.0	ns/V
T_F	Output fall time	1.0	3.0	ns/V
C_L	Test load capacitance on Muxed/Non-Muxed outputs		15	pF
	I²C BUS			
f_{SCL}	I²C clock frequency	10	400	KHz
T_{SCH}	I²C clock high time	600		ns
T_{SCL}	I²C clock low time	1.3		ns
T_{DSP}	I²C data spike time	0	50	ns
T_{SDS}	I²C data setup time	100		ns
T_{SDH}	I²C data hold time	0		ns
T_{ICR}	I²C input rise time (10–400pF bus)	20	300	ns
T_{ICF}	I²C input fall time (10–400pF bus)	20	300	ns
T_{BUF}	I²C bus free time between start and stop	1.3		ns
T_{STS}	I²C repeated start condition setup	600		ns
T_{STH}	I²C repeated start condition hold	600		ns
T_{SPS}	I²C stop condition setup	600		ns
C_B	I²C bus capacitive load		400	pF
T_W	Write cycle time[1]	TYPICAL = 15		ms

NOTE:
1. WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I²C address.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

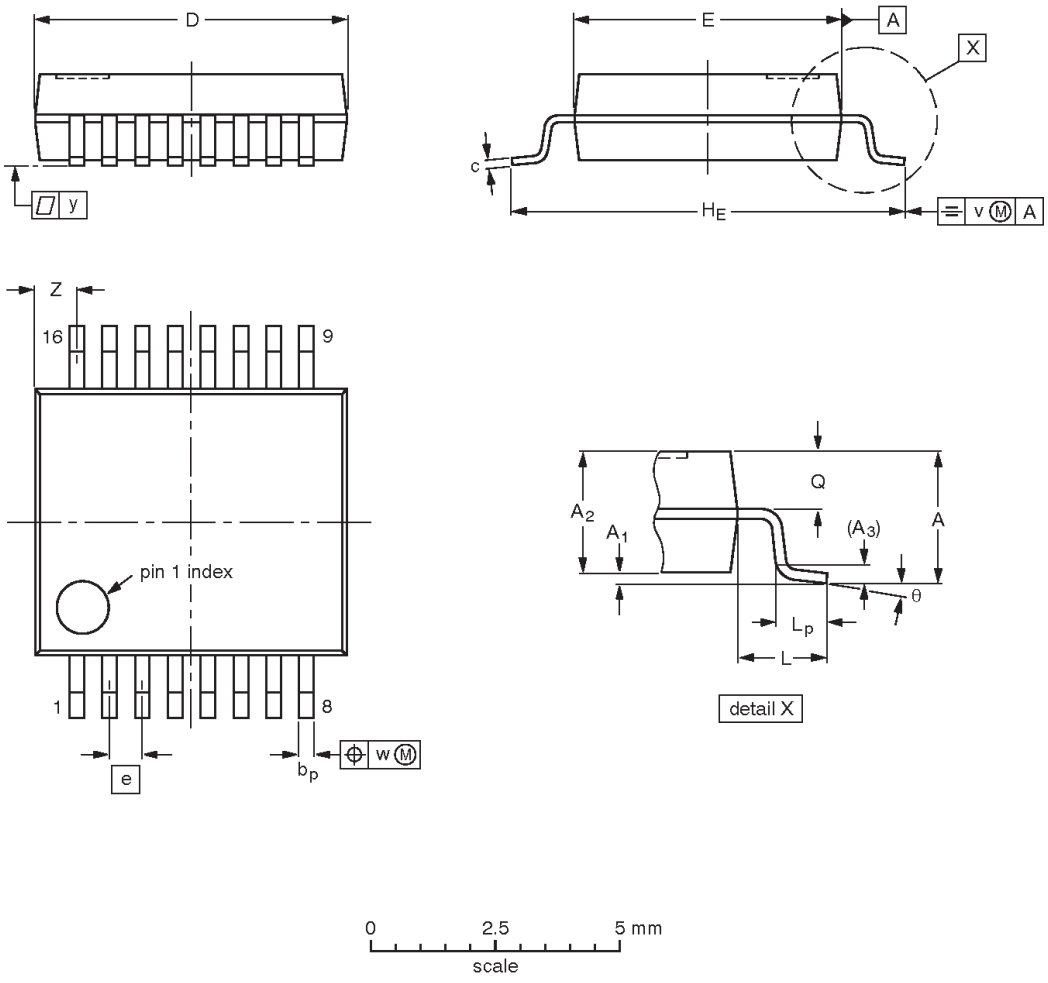
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

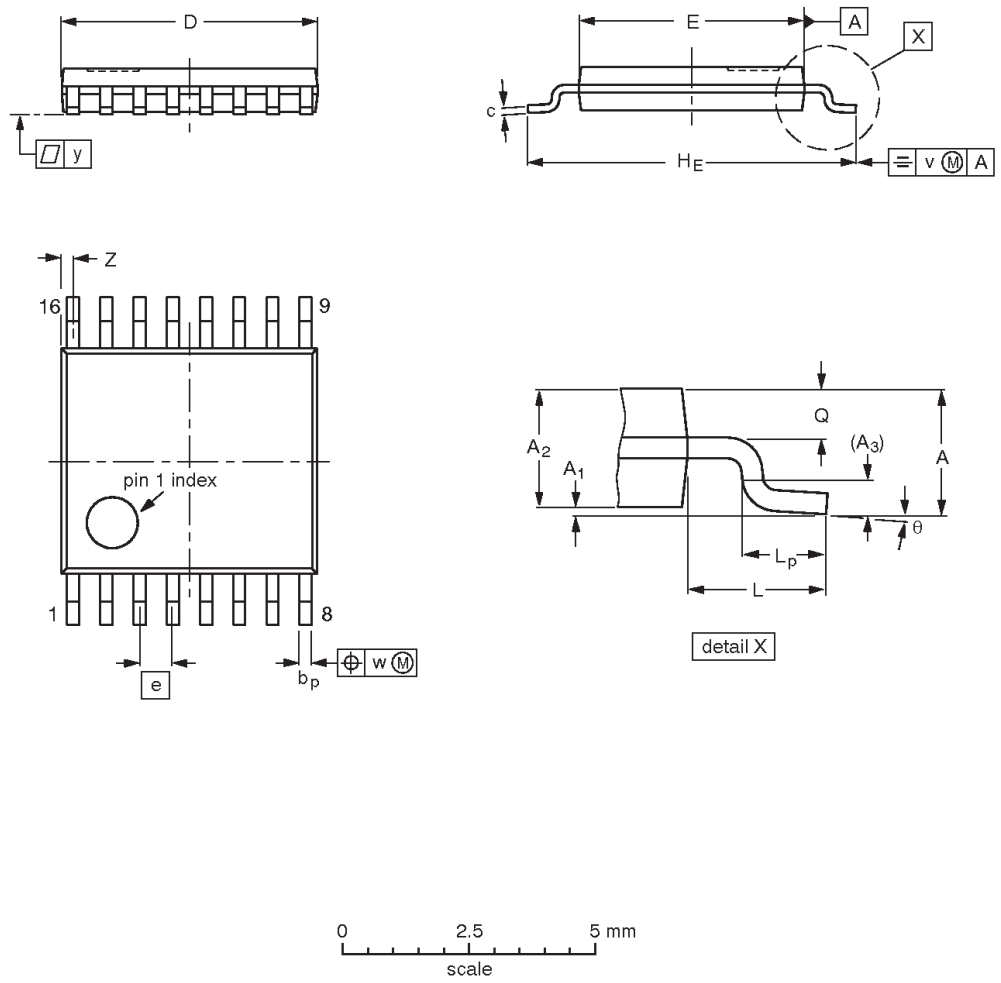
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

NOTES

4-bit multiplexed/1-bit latched 5-bit I²C EEPROM PCA8550

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 01-01

Document order number: 9397 750 07926

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