BR9040
BR9040F

256 × 16 bit serial EEPROM

The BR9040 and BR9040F are CMOS serial input/output-type memory circuits (EEPROMs) that can be programmed electrically. Each can store up to 4096 bits in 256 sixteen bit words. Each word can be accessed separately.

Operational control is performed using four types of 16-bit commands. The commands, addresses, and data are input through the DI pin under the control of the $\overline{CS}$ and $\overline{SK}$ pins.

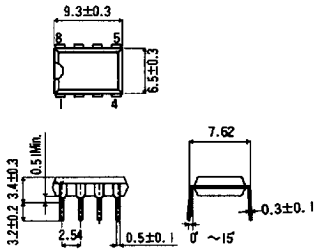
In a write operation, the internal status signal (READY or $\overline{BUSY}$) can be output from the DO pin and R/$\overline{B}$ pins.

Features

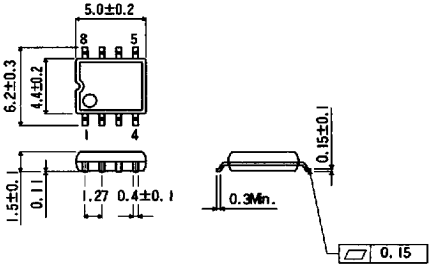
- available in DIP8 and SOP8 packages
- operating voltage is:
  - — during write, 2.7 ~ 5.7 V
  - — during read, 2.0 ~ 5.0 V
- low current consumption
  - — during operation, 1.5 mA at 3 V (max)
  - — while standby, 2 μA at 3 V (max)
- can be rewritten at least 10 000 times
- data can be stored for 10 years without corruption

Dimensions (Units : mm)

BR9040 (DIP8)



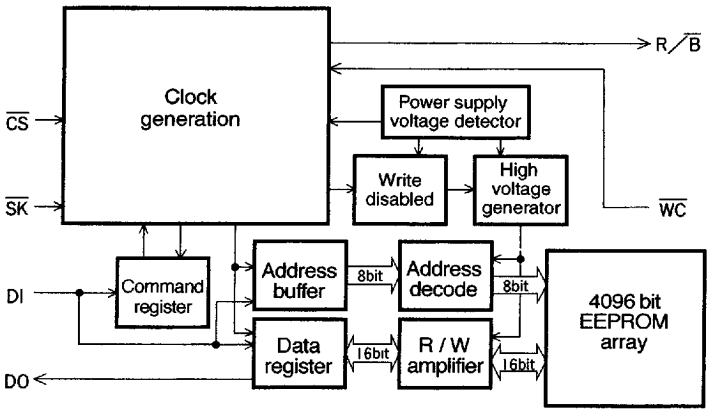
BR9040F (SOP8)



Applications

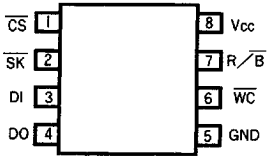
- video tape recorders
- televisions
- facsimile machines
- cameras
- pagers
- printers
- car stereo radio cassette players
- cordless telephones
- programmable DIP switches

Block diagram

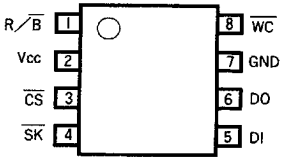


Pin connections

BR9040

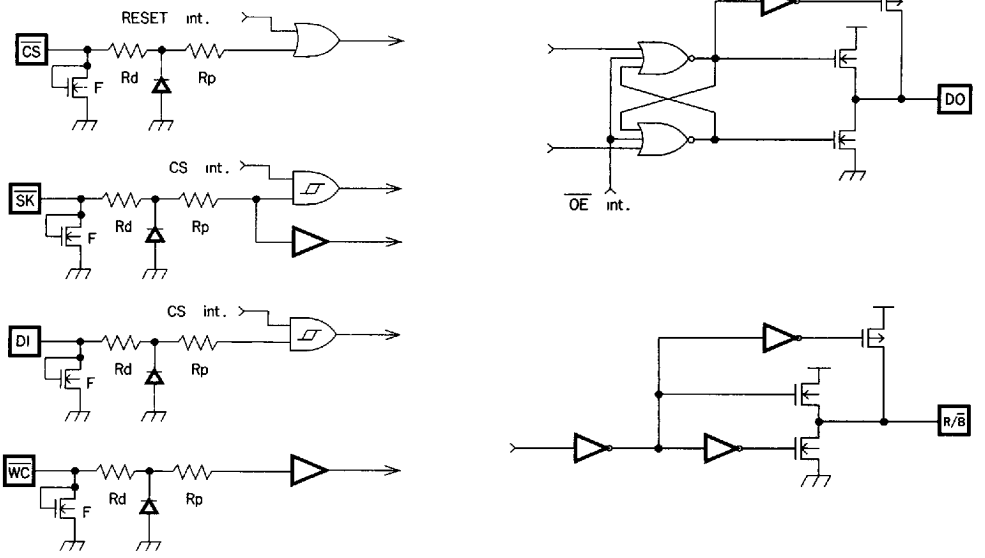


BR9040F



Pin no.		Pin name	Description
BR9040	BR9040F		
1	3	$\overline{CS}$	Chip select input
2	4	$\overline{SK}$	Serial clock input
3	5	DI	Serial data input, operating code, address
4	6	DO	Serial data output
5	7	GND	Ground
6	8	$\overline{WC}$	Write control input
7	1	R/$\overline{B}$	READY, $\overline{BUSY}$ status signal output
8	2	V_{CC}	Power supply

Input and output equivalent circuits



Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Supply voltage		V_{CC}	–0.3 ~ +7.0	V	
Power dissipation	BR9040	P_d	500	mW	Reduce power by 5.0 mW/°C for each degree above 25°C.
	BR9040F		350		Reduce power by 3.5 mW/°C for each degree above 25°C.
Voltage per pin			–0.3 ~ V_{CC} + 0.3	V	
Storage temperature		T_{stg}	–65 ~ +125	°C	
Operating temperature		T_{opr}	–40 ~ +85	°C	

Recommended operating conditions (T_a = 25°C)

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage	WRITE	V_{CC}	2.7		5.5	V
	READ		2.0		5.5	V
Input voltage		V_{IN}	0		V_{CC}	V

Electrical characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Input voltage low 1	V_{IL1}			$0.3 \times V_{CC}$	V	DI pin
Input voltage high 1	V_{IH1}	$0.7 \times V_{CC}$			V	DI pin
Input voltage low 2	V_{IL2}			$0.2 \times V_{CC}$	V	$\overline{CS}$, $\overline{SK}$, and $\overline{WC}$ pins
Input voltage high 2	V_{IH2}	$0.8 \times V_{CC}$			V	$\overline{CS}$, $\overline{SK}$, and $\overline{WC}$ pins
Output voltage low	V_{OL}	0		0.4	V	I_{OL} = 2.1 mA
Output voltage high	V_{OH2}	V_{CC} – 0.4		V_{CC}	V	I_{OH} = –0.4 mA
Input leak current	I_{LI}	–1		+1	µA	V_{IN} = 0 V ~ V_{CC}
Output leak current	I_{LO}	–1		+1	µA	V_{OUT} = 0 V ~ V_{CC}, $\overline{CS}$ = V_{CC}
Operating current 1	I_{CC1}			2	mA	f = 1 MHz, $t_{E/W}$ = 15 ms (WRITE)
Operating current 2	I_{CC2}			1	µA	f = 1 MHz (READ)
Standby current	I_{SB}			3	µA	$\overline{CS}$ = $\overline{SK}$ = DI = $\overline{WC}$ = V_{CC}, DO and R/$\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}			1	MHz	

Electrical characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 3V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Input voltage low 1	V_{IL1}			$0.3 \times V_{CC}$	V	DI pin
Input voltage high 1	V_{IH1}	$0.7 \times V_{CC}$			V	DI pin
Input voltage low 2	V_{IL2}			$0.2 \times V_{CC}$	V	$\overline{CS}$, $\overline{SK}$, and $\overline{WC}$ pins
Input voltage high 2	V_{IH2}	$0.8 \times V_{CC}$			V	$\overline{CS}$, $\overline{SK}$, and $\overline{WC}$ pins
Output voltage low	V_{OL}	0		0.4	V	I_{OL} = 100 µA
Output voltage high	V_{OH2}	V_{CC} – 0.4		V_{CC}	V	I_{OH} = –100 µA
Input leak current	I_{LI}	–1		+1	µA	V_{IN} = 0 V ~ V_{CC}
Output leak current	I_{LO}	–1		+1	µA	V_{OUT} = 0 V ~ V_{CC}, $\overline{CS}$ = V_{CC}
Operating current 1	I_{CC1}			1.5	mA	f = 1 MHz, $t_{E/W}$ = 15 ms (WRITE)
Operating current 2	I_{CC2}			500	mA	f = 1 MHz (READ)
Stand-by current	I_{SB}			2	µA	$\overline{CS}$ = $\overline{SK}$ = DI = $\overline{WC}$ = V_{CC}, DO and R/$\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}			1	MHz	V_{CC} = 3.0 ~ 3.3 V
				750	kHz	V_{CC} = 2.7 ~ 3.0 V

Operating timing characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit
$\overline{CS}$ set up time	t_{CSS}	200			ns
$\overline{CS}$ hold time	t_{CSH}	0			ns
Data set up time	t_{DIS}	150			ns
Data hold time	t_{DIH}	150			ns
DO rise delay time	t_{PD1}			350	ns
DO fall delay time	t_{PD0}			350	ns
Self-timing programming cycle	$t_{E/W}$			10	ms
$\overline{CS}$ minimum HIGH time	t_{CS}	1			µs
Time for READY / $\overline{BUSY}$ display to become valid	t_{SV}			1	µs
Time for DO to become high impedance (from $\overline{CS}$)	t_{OH}	0		400	ns
Data clock time HIGH	t_{WH}	500			ns
Data clock time LOW	t_{WL}	500			ns
Write control set up time	t_{WCS}	0			ns
Write control hold time	t_{WCH}	0			ns

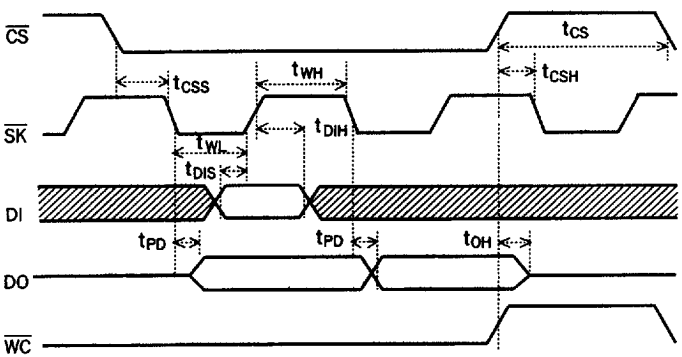
Operating timing characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 3 V ±10%) (Sheet 1 of 2)

Parameter	Symbol	Min	Typical	Max	Unit
$\overline{CS}$ set up time	t_{CSS}	200			ns
$\overline{CS}$ hold time	t_{CSH}	0			ns
Data set up time	t_{DIS}	150			ns
Data hold time	t_{DIH}	150			ns
DO rise delay time V_{CC} = 3.0 ~ 3.3 V	t_{PD1}			350	ns
DO fall delay time V_{CC} = 3.0 ~ 3.3 V	t_{PD0}			350	ns
DO rise delay time V_{CC} = 2.7 ~ 3.0 V	t_{PD1}			500	ns
DO fall delay time V_{CC} = 2.7 ~ 3.0 V	t_{PD0}			500	ns
Self-timing programming cycle	$t_{E/W}$			15	ms
$\overline{CS}$ minimum time HIGH	t_{CS}	1			µs

Operating timing characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 3 V ±10%) (Sheet 2 of 2)

Parameter	Symbol	Min	Typical	Max	Unit
Time for READY / $\overline{BUSY}$ display to become valid	t_{SV}			1	µs
Time for DO to become high impedance (from $\overline{CS}$)	t_{OH}	0		400	ns
Data clock time HIGH	t_{WH}	450			ns
Data clock time LOW	t_{WL}	450			ns
Write control set up time	t_{WCS}	0			ns
Write control hold time	t_{WCH}	0			ns

Figure 1 Timing chart



Data is read in on the rising edge of $\overline{SK}$. Data is output in synchronism with the $\overline{SK}$ falling edge.

During a READ operation, data is output from DO in synchronization with the $\overline{SK}$ rise.

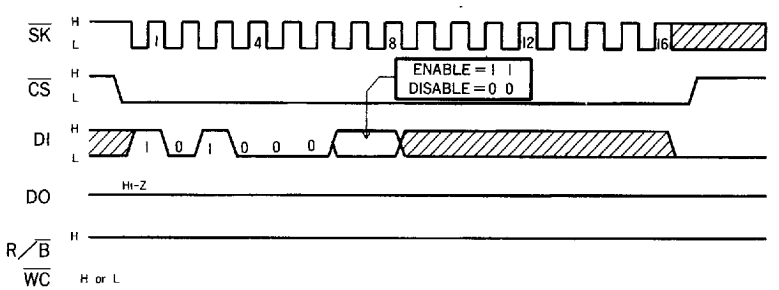
$\overline{WC}$ is related to the write command only. Read, erase/write enable, erase/write disable commands can be executed irrespective of the state of $\overline{WC}$.

Circuit operation

Command	Start bit	Operating code	Address	Data
Read (READ)	1010	1000	A0 A1 A2 A3 A4 A5 A6 A7	
Write (WRITE)	1010	0100	A0 A1 A2 A3 A4 A5 A6 A7	D0 D1 – D14 D15
Erase/write enabled (EWEN)	1010	0011	* * * * * * * *	
Erase/write disabled (EWDS)	1010	0000	* * * * * * * *	
where * = V_{IH} or V_{IL}				

Write Enabled (EWEN) and Write Disabled (EWDS)

Figure 2 Write enabled and write disabled timing diagram

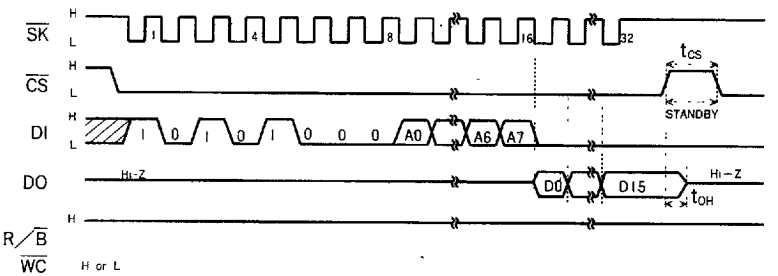


When the power supply is ON, if $\overline{CS}$ is HIGH, the write disabled state is active. Before trying to enter the Write mode, make sure to go to the Write Enabled state first. When set, the Write Enabled state remains valid until the Write Disabled command is entered or the power is cut.

There is no requirement to keep the clock connected after the first 16 clock pulses have been received.

Read command (READ)

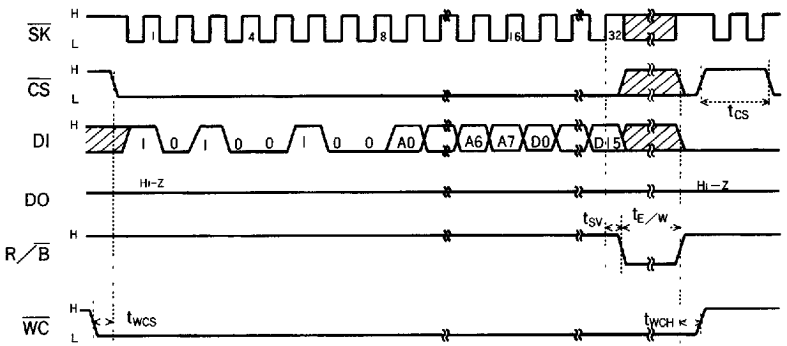
Figure 3 Read cycle timing (READ)



Note: Data is read from the DO pin after the fall of the 16th clock pulse.

Write command (WRITE)

Figure 4 Write cycle timing (WRITE)



After the 32nd clock pulse rise, the R/$\overline{B}$ pin after the TSV process is LOW.

During the execution of a write, the R/$\overline{B}$ is LOW. When the write ends according to the internal timer, the R/$\overline{B}$ pin automatically becomes HIGH.

During input of the write command, $\overline{CS}$ must be LOW. However, when the write begins, $\overline{CS}$ may be either HIGH or LOW. $\overline{SK}$ may be used for other tasks.

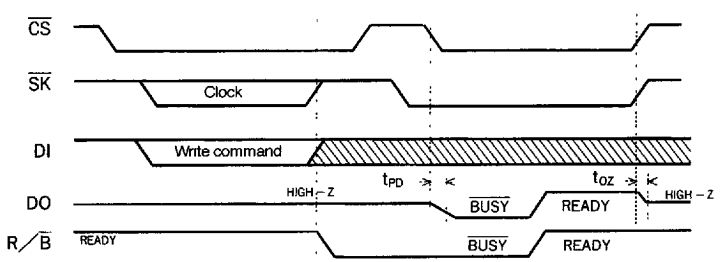
Setting the $\overline{WC}$ pin HIGH when executing a write will force the write to stop instantly. The address data may be lost. ROHM recommends rewriting the data if this occurs.

READY/$\overline{BUSY}$ display (R/$\overline{B}$Pin, DO Pin)

When in the write state, when actually writing to a memory cell, the READY/ $\overline{BUSY}$ indication is output from the R/$\overline{B}$ pin.

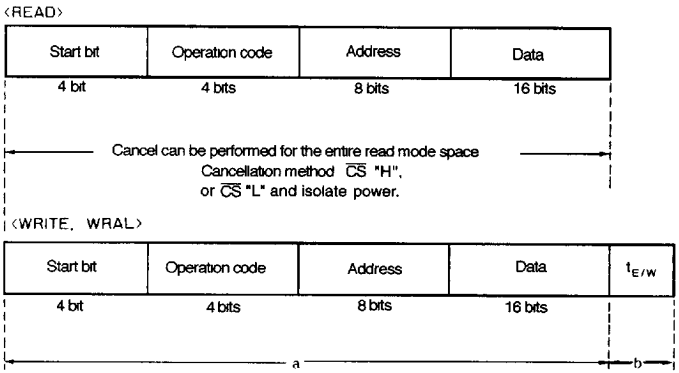
After issuing the write command, when $\overline{SK}$ = LOW, if $\overline{CS}$ falls, the READY/ $\overline{BUSY}$ indication is output from the DO pin.

Figure 5 R/$\overline{B}$ status output timing



Precautions for use

Figure 6 CANCELING MODES



In time a, modes can be cancelled by setting $\overline{CS}$ to HIGH.

In time b, modes can be cancelled by setting $\overline{WC}$ to HIGH, but note that if this is done, the data in the designated addresses cannot be guaranteed.

Power up or power down of the IC

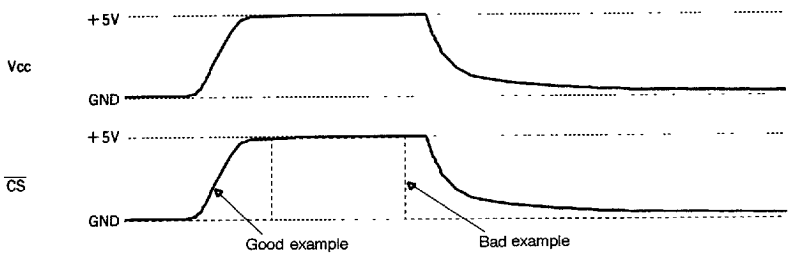
Make sure $\overline{CS}$ is HIGH before isolating or turning on the power supply (V_{CC}) to the IC.

When $\overline{CS}$ is LOW, the EEPROM enters the active state. Turning on the power supply in this situation can result in erroneous operations and erroneous writes due to the influence of noise. To avoid this, set $\overline{CS}$ to HIGH (disable mode) when connecting the power supply. (When $\overline{CS}$ is HIGH, all input is canceled.)

When the power supply is isolated, the IC can be in a low power state for a long time because of the capacity of the power supply line. Erroneous operations and erroneous writes can occur at such times for the same reasons as described above. Therefore, make sure to set $\overline{CS}$ to LOW when turning the power supply off.

To avoid erroneous writes during low voltage operation, a circuit which resets the write command when V_{CC} is less than 2.0 V is installed. (V_{CC}-lockout circuit)

Figure 7 Relationship between V_{CC} and $\overline{CS}$



In the bad example shown in Figure 7, the $\overline{CS}$ pin is pulled down to Ground. In this situation, $\overline{CS}$ is LOW (active state). The EEPROM may perform erroneous operations or erroneous writes due to the influence of noise.

Caution is required because such problems can occur even when the $\overline{CS}$ input is HIGH-Z.

In the good example, $\overline{CS}$ is HIGH until the IC reaches V_{CC} and is set to LOW well before the voltage starts to fall when the EEPROM is de-energized.

Clock ($\overline{SK}$) rise conditions

If the clock pin ($\overline{SK}$) signal has a long rise time (t_R), and there is excessive noise on the signal line, erroneous operations can occur due to erroneous counts in the clock. To avoid this, a Schmitt trigger is built into the $\overline{SK}$ input.

Furthermore, the hysteresis width of this circuit is set at about 0.2 V. Therefore, if the noise exceeds the $\overline{SK}$ input, make sure to set the noise amplitude to below 0.2 $V_{pk\text{-}pk}$. Also, make sure to accelerate rises and falls in the clock as much as possible.

Connecting DI and DO directly

The BR9040 and BR9040F have independent input pins (DI) and output pins (DO). These are treated as individual signals on the timing chart but can be controlled through one control line.

Data collision between the μ-COM output and the DO output

When considering the input and output timing, the timing that causes the most problems is when a signal is simultaneously emitted from the μ-COM output to the DI input and from the DO output as per the following:

Read data is output to the DO pin on the falling edge of the clock and acquires the A7 address during the read command.

In particular, when the read data is different from the A0 data, feedthrough current paths can occur.

After the write, if $\overline{CS}$ falls when $\overline{SK}$ = LOW, the READY/$\overline{BUSY}$ function is output to the DO pin. When the next start bit is input, it becomes HIGH-Z.

In particular, when entering a command after a write, when the $\overline{CS}$ input falls ($\overline{SK}$ = LOW) while the μ-COM output remains LOW, the READY output HIGH is output from the DO pin and feedthrough current paths can occur.

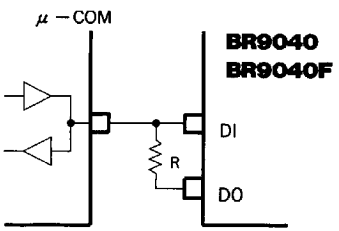
When the μ-COM Port is the CMOS Port

The μ-COM port can be controlled by the 1 control line by connecting a resistor R between the DI and DO pins during CMOS input and output (see Figure 8).

The value of R needs to satisfy the positive portion of the μ-COM input level for the voltage drop at R resulting from the leak current of the μ-COM input and the DI pin.

It must be as small as possible so that it does not influence the DO output noise but large enough to keep the feedthrough current to a minimum. A value in the range 1 k – 200 kΩ is usually sufficient. Make sure to confirm this through experiment. In this case, a dummy bit cannot be detected.

Figure 8 CMOS port equivalent circuit



Feedback to the DI input from the DO output

Data is output from the DO pin and feeds back into the DI input through the resistor R. This happens when

- DO data is output during a READ operation
- READY or $\overline{BUSY}$ signal is output during a WRITE operation

Such feedback input does not cause problems in the basic operations