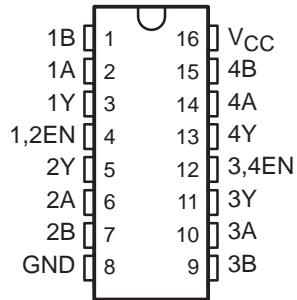


- Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485
- Meets ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirement 27 mA Max
- Common-Mode Input Voltage Range of -12 V to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operates From Single 5-V Supply

N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-ended taped and reeled (order device SN75ALS175NSLE).

description

The SN75ALS175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, and RS-485 and several ITU recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. Each of the two pairs of receivers has a common active-high enable. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of -12 V to 12 V.

The SN75ALS175 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2 < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open Circuit	H	H

H = high level, L = low level, ? = indeterminate,

X = irrelevant, Z = high impedance (off)

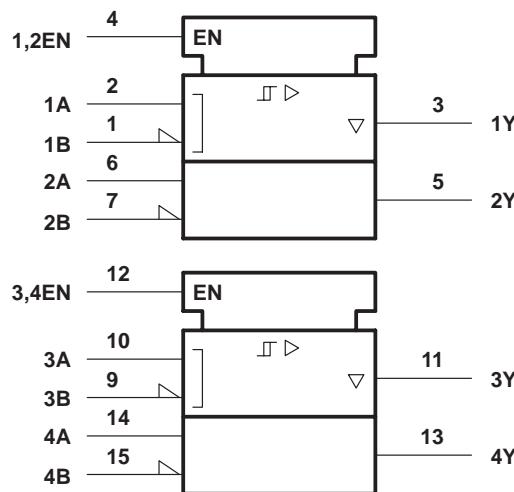


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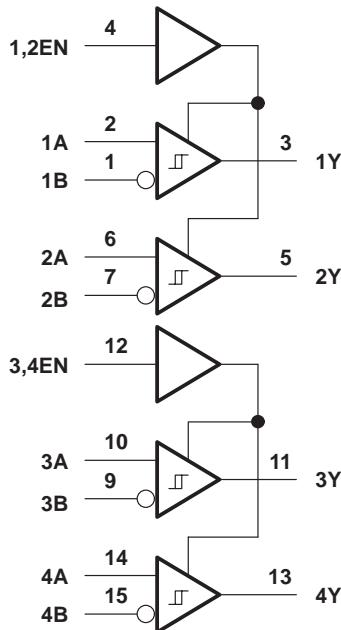
SN75ALS175 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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logic symbol†

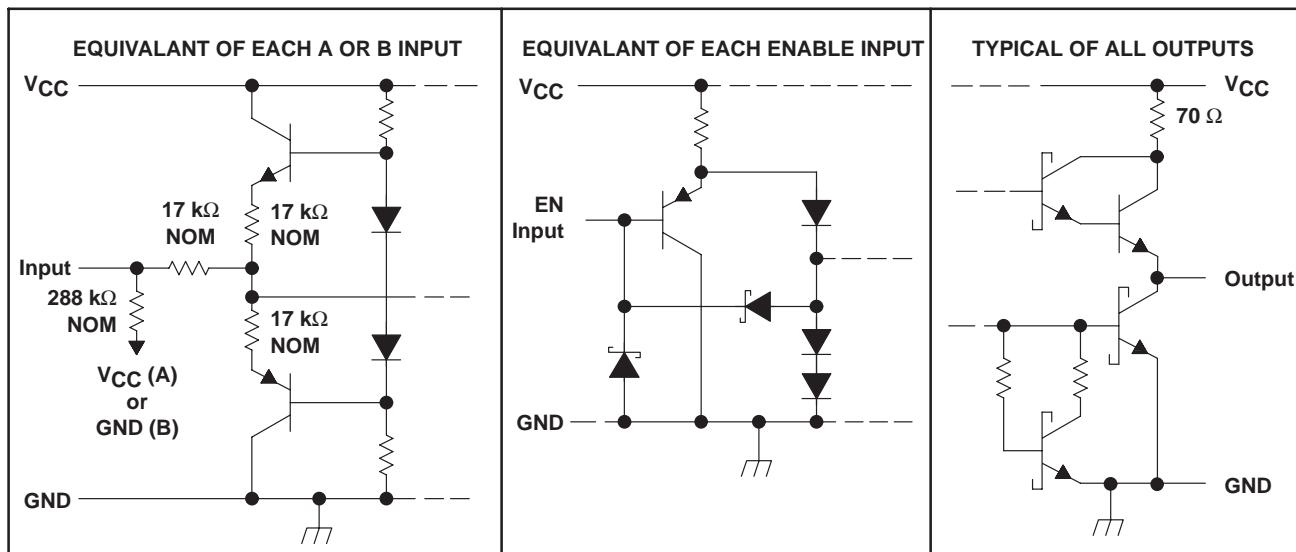


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (A or B inputs)	± 14 V
Differential input voltage, V_{ID} (see Note 2)	± 14 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 12	V
Differential input voltage, V_{ID}			± 12	V
High-level enable-input voltage, V_{IH}		2		V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	$^\circ\text{C}$

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QUADRUPLE DIFFERENTIAL LINE RECEIVER

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electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
V_{IT+} Positive-going input threshold voltage			200		mV			
V_{IT-} Negative-going input threshold voltage			-200‡		mV			
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV			
V_{IK} Enable-input clamp voltage	$I_I = -18 \text{ mA}$		-1.5		V			
V_{OH} High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -400 \mu\text{A}$, See Figure 1		2.7		V			
V_{OL} Low-level output voltage	$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$, See Figure 1		0.45		V			
I_{OZ} High-impedance-state output current	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$		±20		μA			
I_I Line input current	Other input at 0 V, See Note 3		$V_I = 12 \text{ V}$		1	mA		
I_{IH} High-level enable-input current			$V_I = -7 \text{ V}$		-0.8			
I_{IL} Low-level enable-input current	$V_{IL(E)} = 0.4 \text{ V}$		20		μA			
r_I Input resistance			12		$\text{k}\Omega$			
I_{OS} Short-circuit output current	$V_O = 0$		-15		-85			
I_{CC} Suply current (total package)	No load, Outputs enabled		16		24	mA		
	No load, Outputs disabled		18		27			

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

NOTE 3: Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL} Propagation delay time, high- to low-level output	$V_{ID} = -2.5 \text{ V to } 2.5 \text{ V}$,	9	18	27	ns
t_{PLH} Propagation delay time, low- to high-level output	$C_L = 15 \text{ pF}$, See Figure 2	9	18	27	ns
t_{PZH} Output enable time to high level	$C_L = 15 \text{ pF}$, See Figure 3	4	12	18	ns
t_{PZL} Output enable time to low level	$C_L = 15 \text{ pF}$, See Figure 3	6	13	21	ns
t_{PHZ} Output disable time from high level	$C_L = 15 \text{ pF}$, See Figure 3	10	21	27	ns
t_{PLZ} Output disable time from low level		8	15	25	ns

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.



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PARAMETER MEASUREMENT INFORMATION

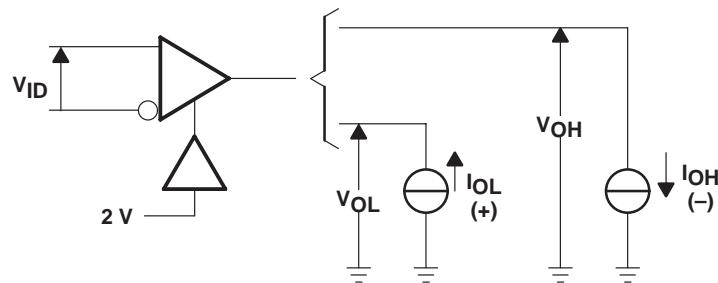
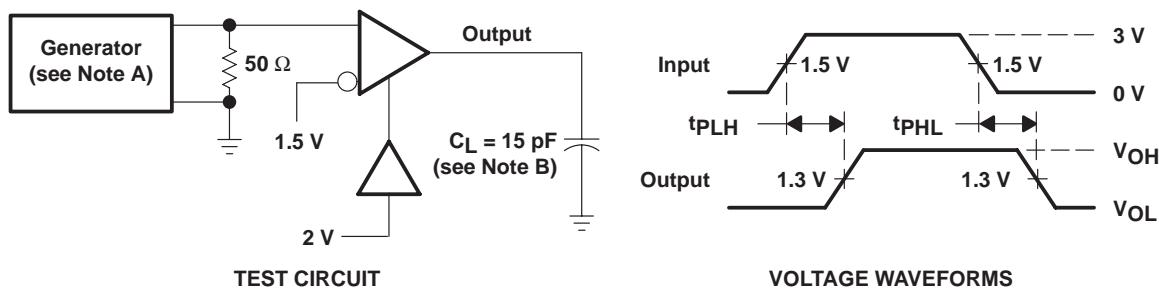


Figure 1. V_{OH} , V_{OL}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6\text{ ns}$.
B. C_L includes probe and jig capacitance.

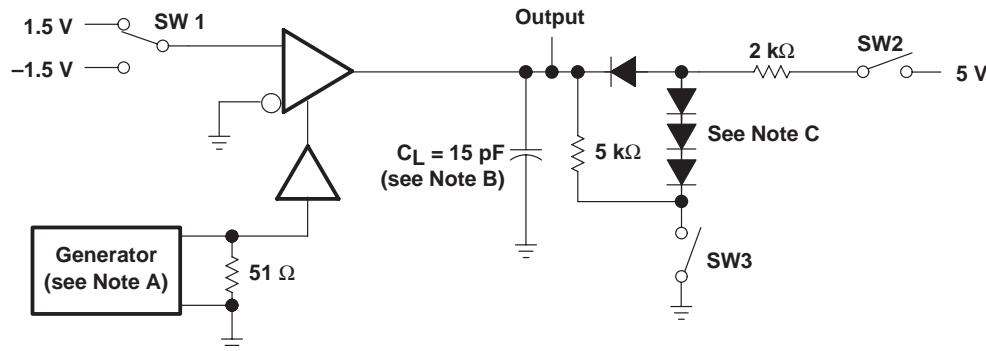
Figure 2. Propagation Delay Times

SN75ALS175

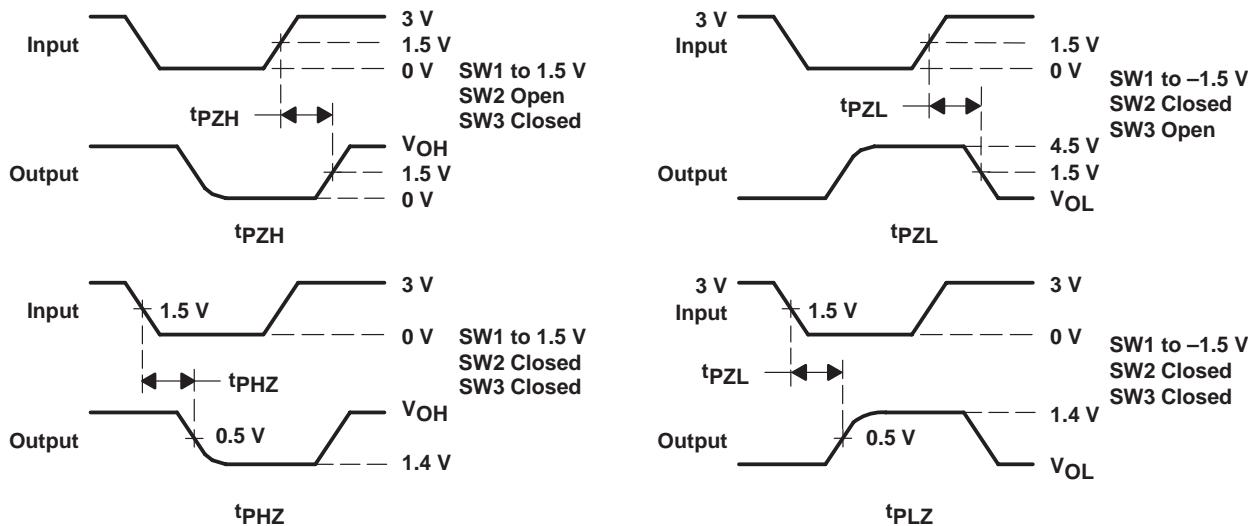
QUADRUPLE DIFFERENTIAL LINE RECEIVER

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or equivalent.

Figure 3. Enable and Disable Times

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75ALS175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS175NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS175NSLE	OBsolete	SO	NS	16		TBD	Call TI	Call TI
SN75ALS175NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS175NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

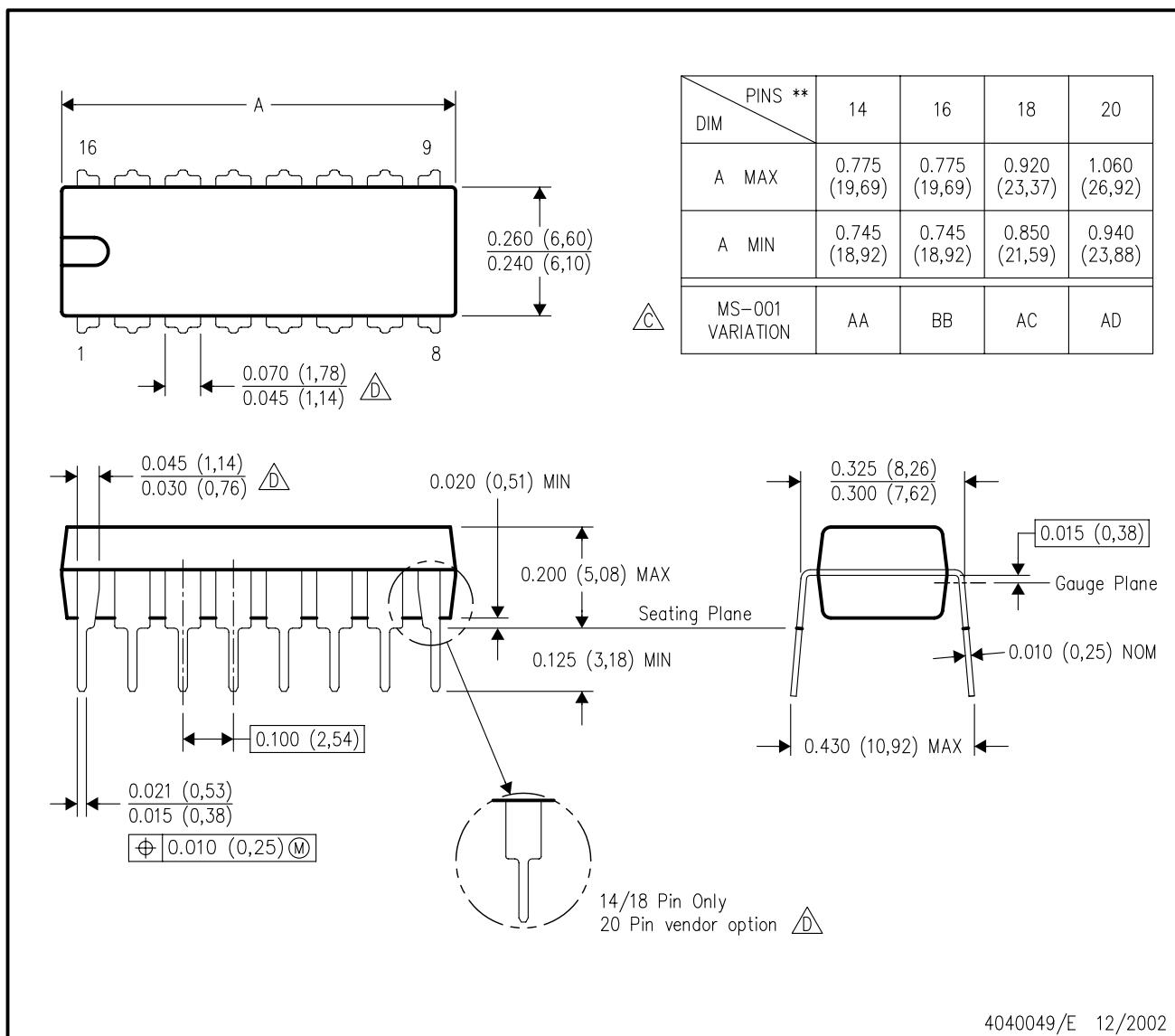
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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

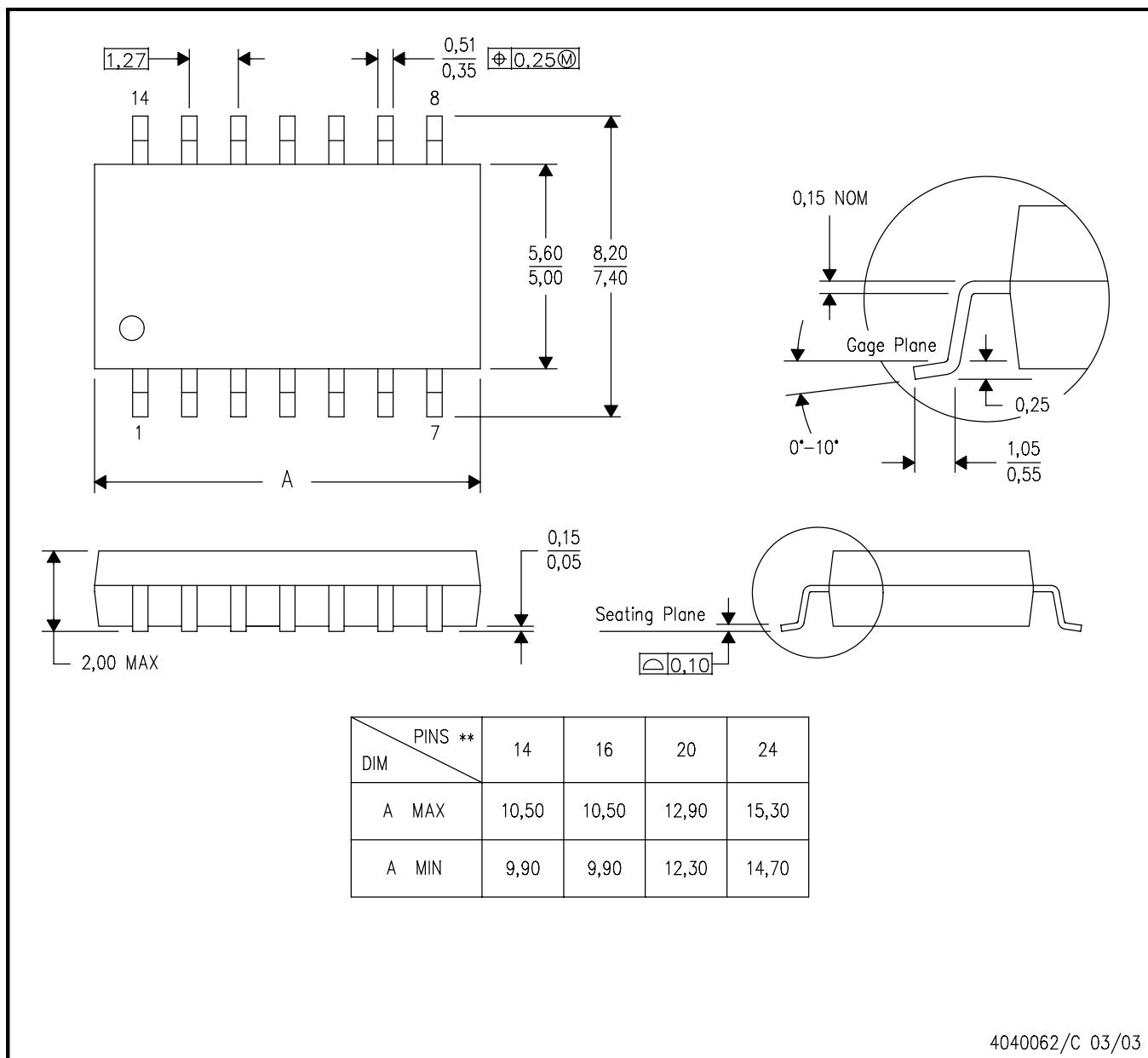
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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