

TJA1145

High-speed CAN transceiver for partial networking

Rev. 1 — 27 September 2013

Product data sheet

1. General description

The TJA1145 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1145 features very low power consumption in Standby and Sleep modes and supports ISO 11898-6 compliant CAN Partial Networking by means of a selective wake-up function.

A dedicated implementation of the partial networking function has been embedded into the TJA1145/FD variants TJA1145T/FD and TJA1145TK/FD (see [Section 6.3.1](#) for further details on CAN FD). This function is called 'FD-passive' and is the ability to ignore CAN FD frames while waiting for a valid wake-up frame in Sleep/Standby mode. This additional feature of partial networking is the perfect fit for networks that support both CAN FD and standard CAN 2.0 communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

Advanced power management regulates the supply throughout the node and supports local and remote wake-up functionality. I/O levels are automatically adjusted to the I/O levels of the controller, allowing the TJA1145 to interface directly with 3.3 V to 5 V microcontrollers. An SPI interface is provided for transceiver control and for retrieving status information. Bus connections are truly floating when power is off.

These features make the TJA1145 the ideal choice for high-speed CAN networks containing nodes that are always connected to the battery supply line but, in order to minimize current consumption, are only active when required by the application.

2. Features and benefits

2.1 General

- Fully compliant with the ISO 11898-2, ISO 11898-5 and ISO 11898-6 standards
- Autonomous bus biasing according to ISO 11898-6
- Optimized for in-vehicle high-speed CAN communication
- No 'false' wake-ups due to CAN FD frame detection in TJA1145/FD variants

2.2 Designed for automotive applications

- ± 8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins



- ± 6 kV ESD protection, according to IEC 61000-4-2 on pins BAT and WAKE and on the CAN bus pins
- CAN bus pins short-circuit proof to ± 58 V
- Battery and CAN bus pins protected against transients according to ISO 7637-3, test pulses 1, 2a, 3a and 3b.
- Suitable for use in 12 V and 24 V systems
- Available in SO14 and leadless HVSON14 package (3 mm \times 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Advanced ECU power management system

- Very low-current Standby and Sleep modes, with full wake-up capability
- Entire node can be powered down via the inhibit output
- Remote wake-up capability via standard CAN wake-up pattern or via ISO 11898-6 compliant selective wake-up frame detection
- Local wake-up via the WAKE pin
- Wake-up source recognition
- Local and/or remote wake-up can be disabled to reduce current consumption
- Transceiver disengages from the bus when the battery supply is removed
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers

2.4 Protection and diagnosis

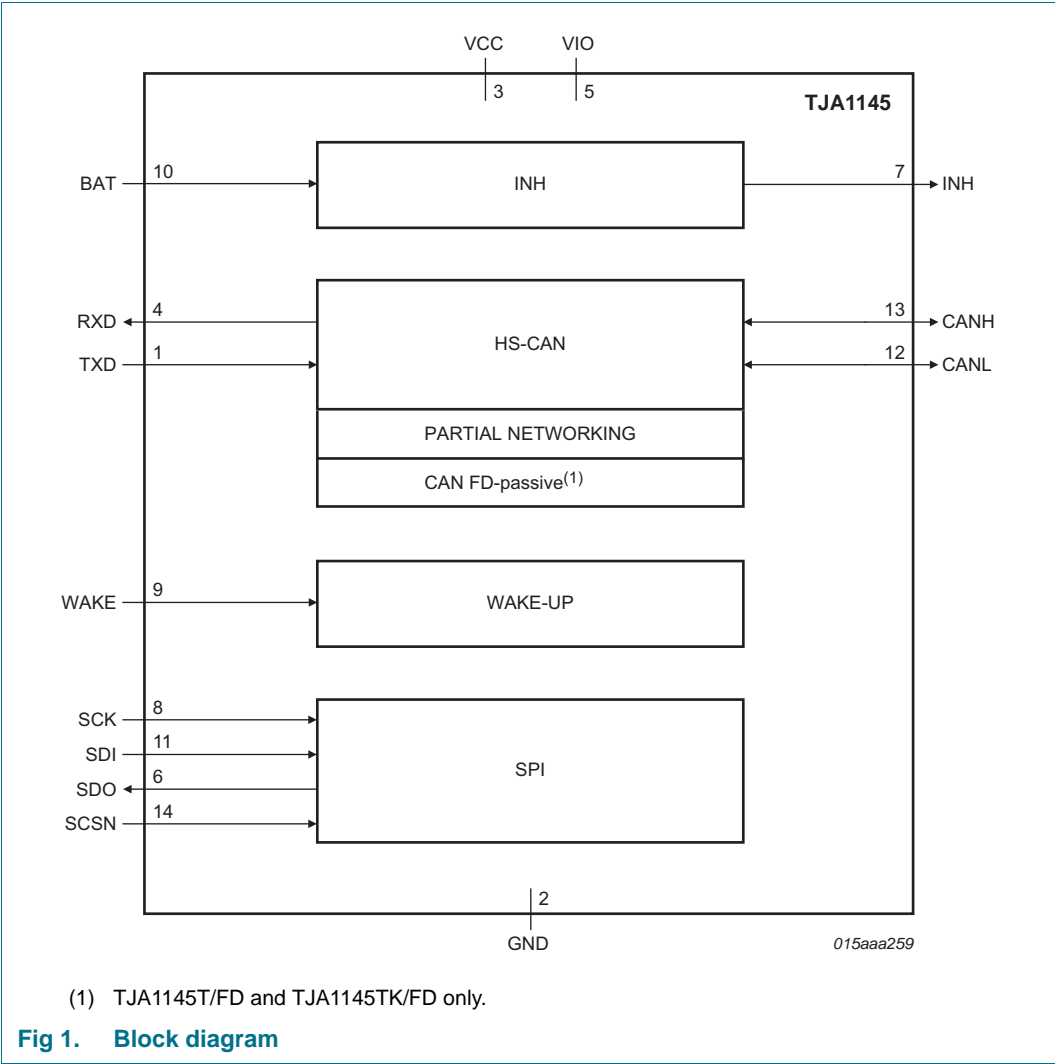
- 16-, 24- or 32-bit SPI for configuration, control and diagnosis
- Transmit Data (TXD) dominant time-out function with diagnosis
- Overtemperature warning and shut-down
- Undervoltage detection and recovery on pins VCC, VIO and BAT
- Cold start diagnosis (via bits PO and NMS)
- Advanced system and transceiver interrupt handling

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1145T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145T/FD	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145TK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
TJA1145TK/FD	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

4. Block diagram



5. Pinning information

5.1 Pinning

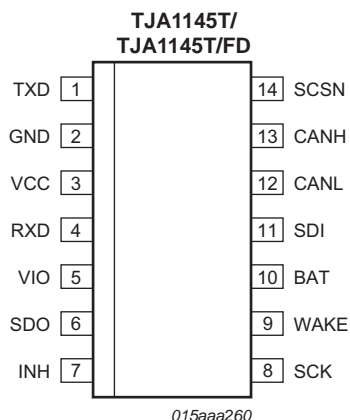


Fig 2. Pin configuration diagram: SO14

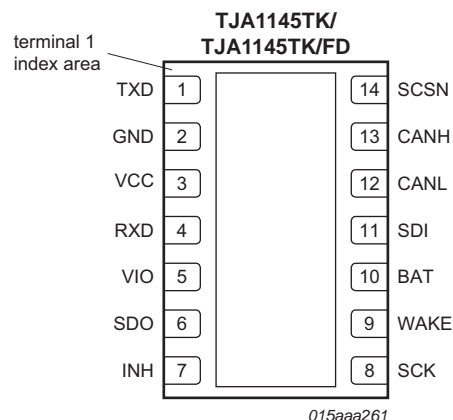


Fig 3. Pin configuration diagram: HVSON14 Transparent top view

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2 ^[1]	ground
VCC	3	5 V CAN transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
VIO	5	supply voltage for I/O level adaptor
SDO	6	SPI data output
INH	7	inhibit output for switching external voltage regulators
SCK	8	SPI clock input
WAKE	9	local wake-up input
BAT	10	battery supply voltage
SDI	11	SPI data input
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
SCSN	14	SPI chip select input

[1] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended to solder the exposed center pad to board ground.

6. Functional description

The TJA1145 is a stand-alone high-speed CAN transceiver containing a variety of fail-safe and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver combines the functionality of the TJA1043 with ISO 11898-6 compliant CAN partial networking and autonomous bus biasing.

6.1 System controller

The system controller manages register configuration and controls the internal functions of the TJA1145. Detailed device status information is collected and made available to the microcontroller.

6.1.1 Operating modes

The system controller contains a state machine that supports five operating modes: Normal, Standby, Sleep, Overtemp and Off. The state transitions are illustrated in [Figure 4](#).

6.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, the TJA1145 is fully operational. All device hardware is available and can be activated (see [Table 3](#)).

Normal mode can be selected from Standby or Sleep mode via an SPI command (MC = 111).

6.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the TJA1145, featuring low current consumption. The transceiver is unable to transmit or receive data in Standby mode, but the INH pin remains active so voltage regulators controlled by this pin will be active.

If remote CAN wake-up is enabled (CWE = 1; see [Table 27](#)), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1; otherwise standard wake-up is enabled).

Pin RXD is forced LOW when any enabled wake-up or interrupt event is detected (see [Section 6.6](#)).

The TJA1145 switches to Standby mode:

- from Off mode if the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$.
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$.
- from Sleep mode on the occurrence of a wake-up or interrupt event (see [Section 6.6](#))
- from Normal or Sleep mode via an SPI command (MC = 100)
- from Normal mode if Sleep mode is selected via an SPI command (MC = 001) while a wake-up event is pending or all wake-up sources are disabled

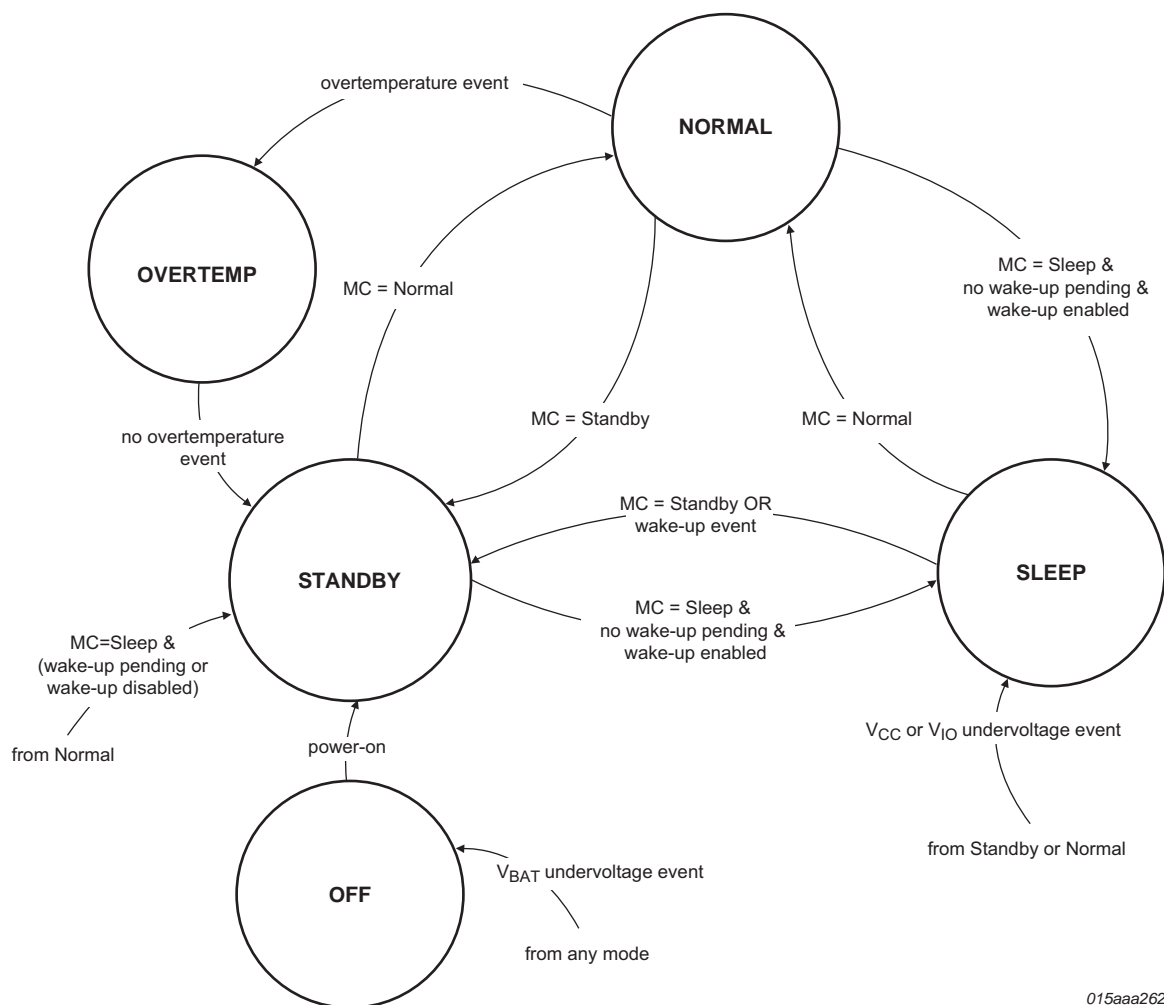


Fig 4. TJA1145 system controller state diagram

6.1.1.3 Sleep mode

Sleep mode is the second-level power saving mode of the TJA1145. In Sleep mode, the transceiver behaves as in Standby Mode with the exception that pin INH is set to a high-ohmic state. Voltage regulators controlled by this pin will be switched off, and the current into pin BAT will be reduced to a minimum.

Any enabled wake-up or interrupt event, or an SPI command (provided a valid V_{IO} voltage is connected), will wake up the transceiver from Sleep mode.

Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001). The TJA1145 will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source (CAN bus or WAKE pin; see [Section 6.6](#)) is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the TJA1145 to switch to Standby mode; if SPI failure detection is enabled (SPIFE = 1), pin RXD will be forced LOW to signal a wake-up event.

The TJA1145 will also be forced to switch to Sleep mode if a V_{CC} or V_{IO} undervoltage event is detected ($V_{CC}/V_{IO} < V_{UVD}(V_{CC})/V_{UVD}(V_{IO})$ for longer than $t_{det(uv)}(V_{CC})/t_{det(uv)}(V_{IO})$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock (see [Section 6.11](#)) and selective wake-up is disabled (CPNC = 0).

Status bit FSMS in the Main status register ([Table 5](#)) indicates whether a transition to Sleep mode was selected via an SPI command (FSMS = 0) or was forced by an undervoltage event on VCC or VIO (FSMS = 1). This bit can be sampled after the TJA1145 wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

6.1.1.4 Off mode

The TJA1145 will be in Off mode when the battery voltage is too low to supply the IC. This is the default mode when the battery is first connected. The TJA1145 will switch to Off mode from any mode if the battery voltage drops below the power-off threshold ($V_{th(det)poff}$). In Off mode, the CAN pins and pin INH are in a high-ohmic state.

When the battery supply voltage rises above the power-on threshold ($V_{th(det)pon}$), the TJA1145 starts to boot up, triggering an initialization procedure. The TJA1145 will switch to Standby mode after $t_{startup}$.

6.1.1.5 Overtemp mode

Overtemp mode is provided to prevent TJA1145 being damaged by excessive temperatures. The TJA1145 switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the TJA1145 issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, status bit OTWS is set and an overtemperature interrupt is generated (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD.

The TJA1145 exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

6.1.1.6 Hardware characterization for the TJA1145 operating modes

Table 3. Hardware characterization by functional block

Block	Operating mode				
	Off	Standby	Normal	Sleep	Overtemp
SPI	disabled	active	active	active if V _{IO} supplied ^[1]	disabled
INH	high-ohmic	V _{BAT} level	V _{BAT} level	high-ohmic	V _{BAT} level
CAN	floating	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 6)	Offline	floating
RXD	V _{IO} level	V _{IO} level/LOW if wake-up event detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V _{IO} level/LOW if wake-up event detected	V _{IO} level/LOW if wake-up pending

[1] SPI speed is limited in Sleep mode (see Table 40).

6.1.2 System control registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 6.12).

Table 4. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the TJA1145 has entered Normal mode after initial power-up. Bit FSMS indicates whether the most recent transition to Sleep mode was triggered by an undervoltage event or by an SPI command.

Table 5. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	FSMS	R		Sleep mode transition status:
			0	transition to Sleep mode triggered by an SPI command
			1	an undervoltage on VCC and/or VIO forced a transition to Sleep mode
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	TJA1145 has entered Normal mode (after power-up)
			1	TJA1145 has powered up but has not yet switched to Normal mode
4:0	reserved	R	-	

6.2 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2, ISO 11898-5 and ISO 11898-6 compliant (defining high-speed CAN with selective wake-up functionality and autonomous bus biasing).

The CAN transmitter is supplied via pin VCC while the CAN receiver is supplied via pin BAT.

The CAN transceiver supports autonomous CAN biasing as defined in ISO 11898-6, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11).

Autonomous biasing is active in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{\text{to(silence)}}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller or when CAN partial networking is enabled. The TJA1145 ensures that the CAN bus is correctly biased to avoid disturbances to communications. The autonomous CAN bias voltage is derived directly from V_{BAT} .

6.2.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see [Figure 5](#)). The CAN transceiver operating mode depends on the TJA1145 operating mode and on the setting of bits CMC in the CAN control register ([Table 6](#)).

When the TJA1145 is in Normal mode, the CAN transceiver operating mode (Offline, Active or Listen-only) can be selected via bits CMC in the CAN control register ([Table 6](#)). When the TJA1145 is in Standby or Sleep modes, the transceiver is forced to Offline mode.

6.2.1.1 CAN Active mode

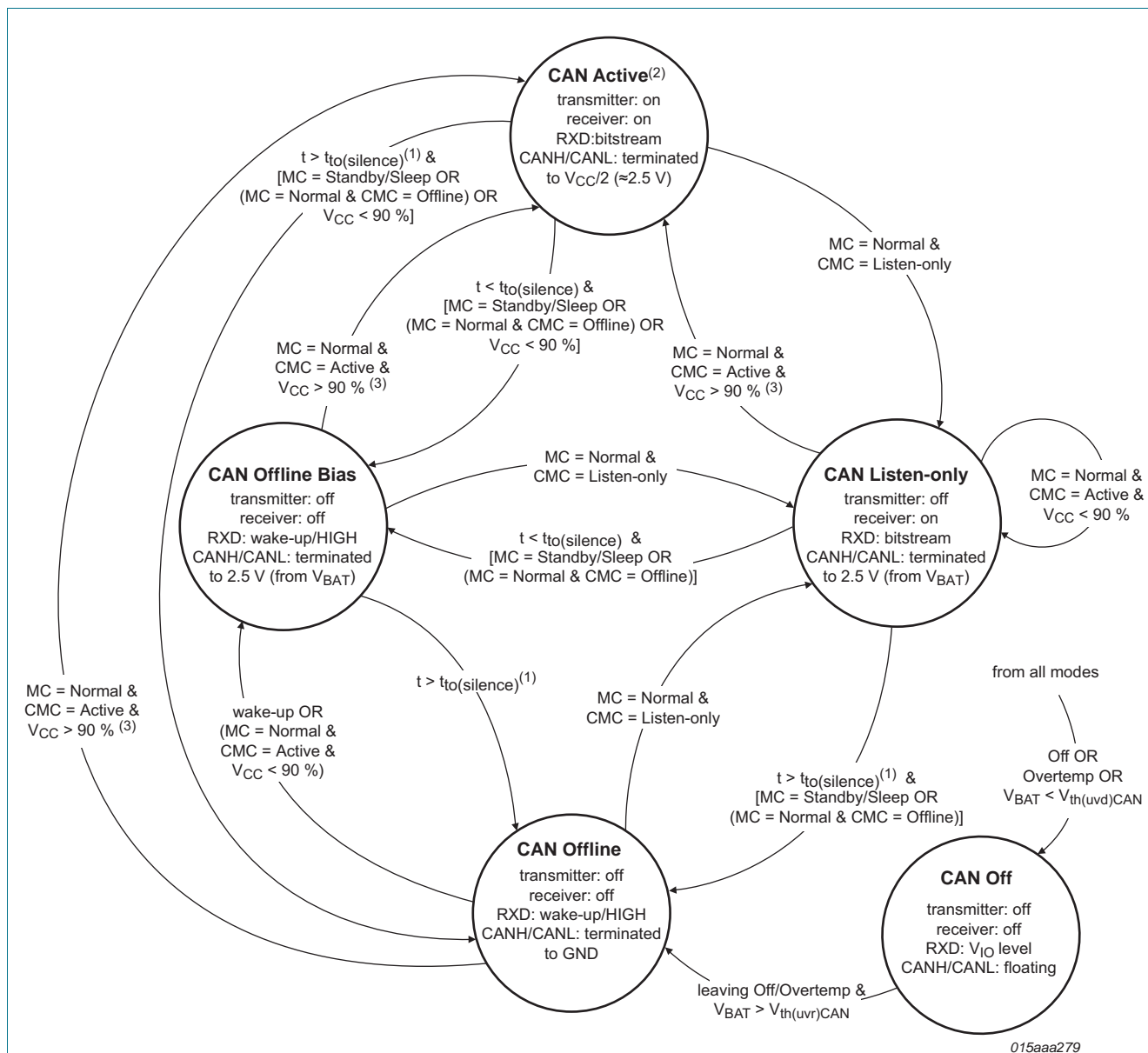
In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

The CAN transceiver is in Active mode when:

- the TJA1145 is in Normal mode (MC = 111) AND
- the CAN transceiver has been enabled by setting bits CMC in the CAN mode control register to 01 or 10 (see [Table 6](#)) AND
- the voltage on pin VCC is above the V_{CC} undervoltage detection threshold ($V_{\text{uvd(VCC)}}$)

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from V_{CC} . If V_{CC} falls below $V_{uvd}(V_{CC})$, the TJA1145 exits CAN Active mode and enters CAN Offline mode with autonomous CAN voltage biasing active.



(1) No activity detected on the CAN bus for $t_{to(silence)}$.

(2) When CMC = 01, a V_{CC} undervoltage event ($V_{CC} < 90\%$) will cause the transceiver to exit Active mode and the transmitter will be switched off. When CMC = 10, the transceiver will not immediately leave Active mode in response to a V_{CC} undervoltage event; the transmitter will remain active until the TJA1145 is forced into Sleep mode by the V_{CC} undervoltage event; the transceiver will then switch to CAN Offline or CAN Offline Bias mode.

(3) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 5. CAN transceiver state machine

The application can determine whether the CAN transceiver is ready to transmit data or is disabled by reading the CAN Transmitter Status (CTS) bit in the Transceiver Status Register ([Table 7](#)).

6.2.1.2 CAN Listen-only mode

CAN Listen-only mode allows the TJA1145 to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active.

The CAN transceiver is in Listen-only mode when:

- the TJA1145 is in Normal mode and CMC = 11

and will remain in Listen-only mode if $V_{CC} < 90\%$ of nominal value, even if CAN Active mode is selected in Normal mode.

6.2.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver is in CAN Offline Bias mode when:

- the TJA1145 is in Standby or Sleep mode OR
- the TJA1145 is in Normal mode and CMC = 00 OR
- the TJA1145 is in Normal mode and CMC = 01, but $V_{CC} < 90\%$ of nominal value OR
- a wake-up event was detected on the CAN bus

The CAN transceiver is in CAN Offline mode when:

- any of the conditions for CAN Offline Bias mode are valid for longer than $t_{to(silence)}$ OR
- the TJA1145 exits Off or Overtemp mode

6.2.1.4 CAN off

The CAN transceiver is switched off completely with the bus lines floating when:

- the TJA1145 switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage release threshold and the TJA1145 is no longer in Off/Overtemp mode.

6.2.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the TJA1145 will monitor the bus for a standard wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up time-out time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 6; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 24) and pin RXD is driven LOW. If the TJA1145 was in Sleep mode when the wake-up event was detected, it will switch pin INH to V_{BAT} to activate external voltage regulators (e.g. for supplying V_{CC} and V_{IO}) and enter Standby mode.

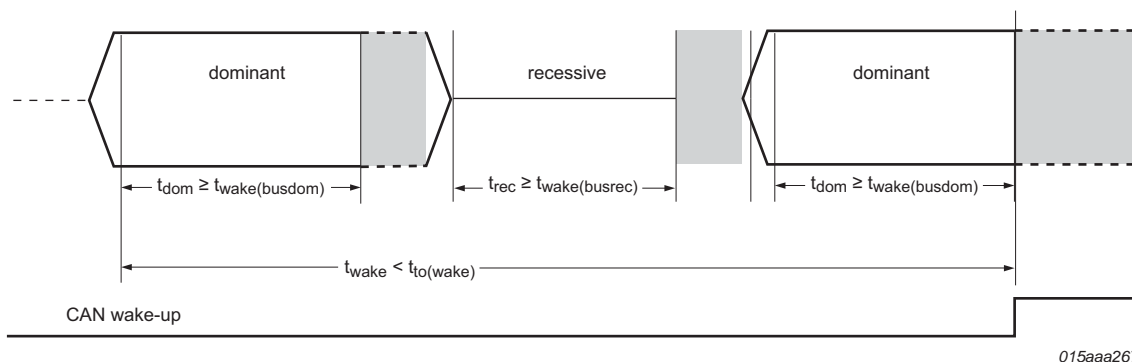


Fig 6. CAN wake-up timing

6.2.3 CAN control and Transceiver status registers

Table 6. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	CFDC	R/W		CAN FD tolerance (TJA1145T/FD and TJA1145TK/FD only; otherwise ignored)
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration registers:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up

Table 6. CAN control register (address 20h) ...continued

Bit	Symbol	Access	Value	Description
3:2	reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection (available when TJA1145 is in Normal mode; MC = 111):
			00	Offline mode
			01	Active mode (V_{CC} undervoltage detection active for CAN state machine)
			10	Active mode (V_{CC} undervoltage detection not active for CAN state machine)
			11	Listen-only mode

Table 7. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R	0	CAN transmitter disabled
			1	CAN transmitter ready to transmit data
6	CPNERR	R	0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0)
5	CPNS	R	0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration OK (PNCOK = 1)
4	COSCS	R	0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R	0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$)
2	reserved	R	-	
1	VCS	R	0	V_{CC} is above the undervoltage detection threshold ($V_{uvd(VCC)}$)
			1	V_{CC} is below the undervoltage detection threshold ($V_{uvd(VCC)}$)
0	CFS	R	0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

6.3 CAN partial networking

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

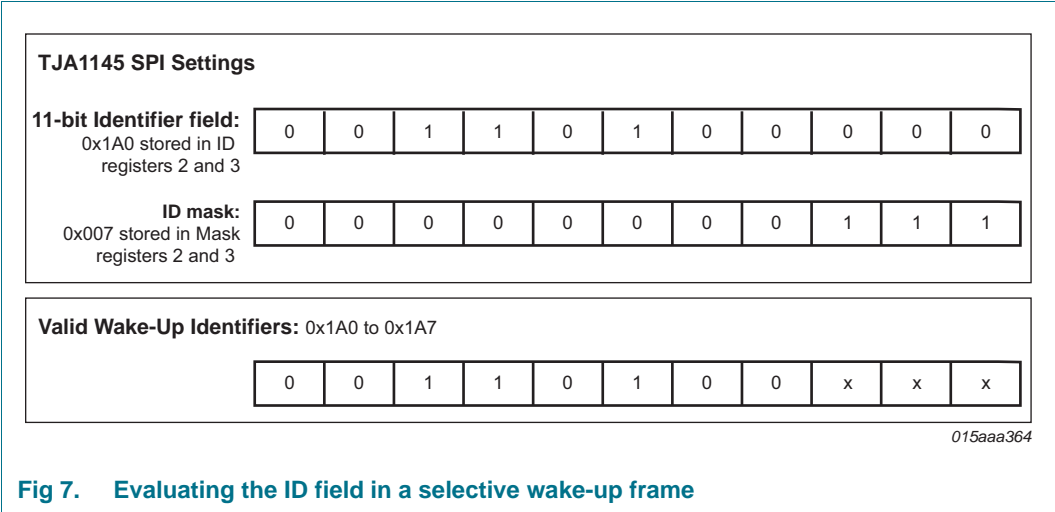
If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

A wake-up frame is a CAN frame according to ISO11898-1, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 17).

A valid WUF identifier is defined and stored in the ID registers (Table 9 to Table 12). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the mask registers (Table 13 to Table 16), where a 1 means ‘don’t care’.

In the example illustrated in Figure 7, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 and 3 (Table 11 and Table 12). The three least significant bits of the ID mask (bits 2 to 4 of Mask register 2; Table 15) are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).



The data field indicates which nodes are to be woken up. Groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up by a single wake-up message.

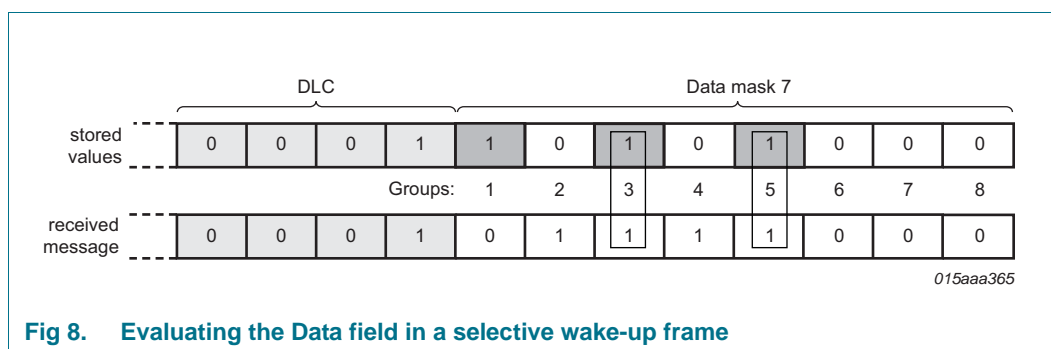
The data length code (bits DLC in the Frame control register; Table 17) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 18) must also be set to 1 for a

successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see [Table 36](#)). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

In the example illustrated in [Figure 8](#), the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see [Table 18](#) and [Figure 9](#)). Data mask 7 is defined as 10101000 in the example. This means that up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1.

The received message shown in [Figure 8](#) could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).



Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included as part of the wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received message matches the configured data length code (bits DLC) AND

- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

If the TJA1145 receives a CAN message containing errors (e.g. a 'stuffing' error) that are received in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The TJA1145 clears PNCOK after a write access to any of the CAN partial networking configuration registers (see [Section 6.3.2](#)).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern (according to ISO 11898-5/-6) will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC ≠ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

6.3.1 CAN FD frames

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as specified in ISO 11898-1. It still uses the CAN bus arbitration method. However, it increases the bit-rate by switching to a shorter bit time at the end of the arbitration process and returns to the longer bit time at the CRC Delimiter, before the receivers transmit their acknowledge bits. The effective data-rate is increased by allowing longer data fields. CAN uses four bits for the data length code, allowing for 16 different codes. However, only the first nine values are used to define the data field length (between 0 and 8 bytes; DLC values from 9 to 15 all indicate an 8-byte data field). In CAN FD, DLC codes 9 to 15 are used to signify longer data fields.

CAN FD is being gradually introduced into automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes). The TJA1145T/FD and TJA1145TK/FD enable FD-passive nodes by means of a dedicated implementation of the partial networking protocol.

The TJA1145/FD variants can be configured to recognize CAN FD frames as valid frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The TJA1145/FD remains in Sleep mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the TJA1145/FD ignores further bus signals until idle is again detected.

CAN FD frames are interpreted as frames with errors by the partial networking module in the TJA1145T and TJA1145TK and in the TJA1145/FD variants when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. Bit PNFDE is set to 1 and the device wakes up if the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow.

6.3.2 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 8. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 9. ID register 0 (address 27h)

Bit	Symbol	Access	Value	Description
7:0	ID07:ID00	R/W	-	bits ID07 to ID00 of the extended frame format

Table 10. ID register 1 (address 28h)

Bit	Symbol	Access	Value	Description
7:0	ID15:ID08	R/W	-	bits ID15 to ID08 of the extended frame format

Table 11. ID register 2 (address 29h)

Bit	Symbol	Access	Value	Description
7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID05 to ID00 of the standard frame format
1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format

Table 12. ID register 3 (address 2Ah)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID06 of the standard frame format

Table 13. Mask register 0 (address 2Bh)

Bit	Symbol	Access	Value	Description
7:0	M07:M00	R/W	-	mask bits ID07 to ID00 of the extended frame format

Table 14. Mask register 1 (address 2Ch)

Bit	Symbol	Access	Value	Description
7:0	M15:M08	R/W	-	mask bits ID15 to ID08 of the extended frame format

Table 15. Mask register 2 (address 2Dh)

Bit	Symbol	Access	Value	Description
7:2	M23:M18	R/W	-	mask bits ID23 to ID18 of the extended frame format mask bits ID05 to ID00 of the standard frame format
1:0	M17:M16	R/W	-	mask bits ID17 to ID16 of the extended frame format

Table 16. Mask register 3 (address 2Eh)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4:0	M28:M24	R/W	-	mask bits ID28 to ID24 of the extended frame format mask. bits ID10 to ID06 of the standard frame format

Table 17. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are 'don't care' for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected; DM0 ignored

Table 18. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

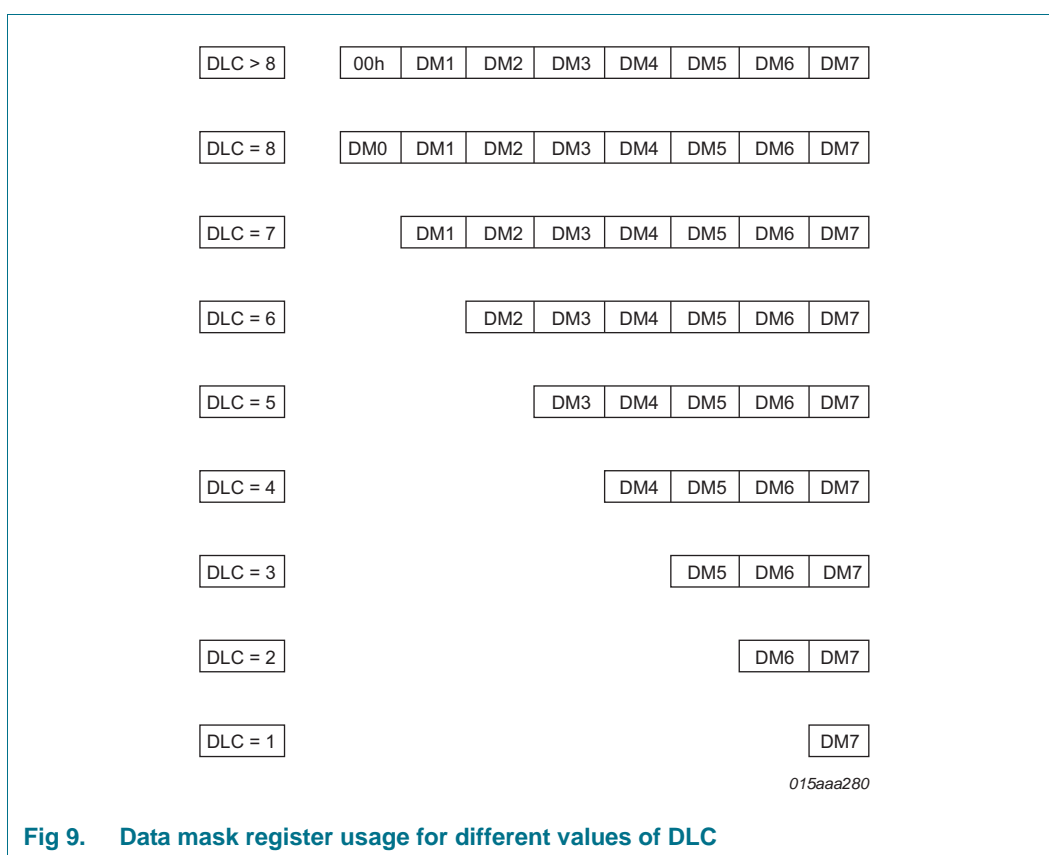


Fig 9. Data mask register usage for different values of DLC

6.4 Fail-safe features

6.4.1 TXD dominant time-out

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated ($CF = 1$; see [Table 24](#)), if enabled ($CFE = 1$; see [Table 27](#)). In addition, the status of the TXD dominant time-out can be read via the CFS bit in the Transceiver status register ([Table 7](#)) and bit CTS is set to 0.

6.4.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V_{IO} to ensure a safe defined recessive driver state in case the pin is left floating.

6.4.3 V_{CC} undervoltage event

An enabled CAN failure interrupt is generated ($CF = 1$) when the CAN transceiver supply voltage on VCC falls below the undervoltage detection threshold ($V_{UVD(VCC)}$), provided $CMC = 01$. In addition, status bit VCS is set to 1.

6.4.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

6.5 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see [Table 28](#)). A wake-up event is triggered by a LOW-to-HIGH (if $WPRE = 1$) and/or a HIGH-to-LOW (if $WPFE = 1$) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 19. WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the TJA1145 is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled ($WPRE = 1$ and/or $WPFE = 1$).

6.6 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the TJA1145 is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers ([Table 23](#) to [Table 25](#)) and is signaled on pin RXD pin, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the TJA1145 to switch to Sleep mode; see [Section 6.1.1.3](#)).

Table 20. Regular wake-up events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

Table 21. Interrupt events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	the TJA1145 has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (only detected in Normal mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal MC code or attempted write access to locked register (not in Sleep mode)
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$
CF	CAN failure	disabled	one of the following CAN failure events detected (not in Sleep mode): <ul style="list-style-type: none"> - CAN transceiver deactivated due to a dominant clamped TXD - CAN transceiver deactivated due to a V_{CC} undervoltage event (if CMC = 01)

PO and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers ([Table 26](#) to [Table 28](#)).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the TJA1145 is in Sleep mode when the event occurs, pin INH is forced HIGH and the TJA1145 switches to Standby mode. If the TJA1145 is in Standby mode when the event occurs, pin RXD is forced LOW to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby or Sleep mode.

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register ([Table 22](#)), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant table ([Table 23](#), [Table 24](#) or [Table 25](#) respectively).

After the event source has been identified, the status bit should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

6.6.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The TJA1145 incorporates an interrupt/wake-up delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d(event)}$, pin RXD remains HIGH (since there are no pending events). The event capture registers can be read at any time.

6.6.2 Sleep mode protection

It is very important that event detection is configured correctly when the TJA1145 switches to Sleep mode to ensure it will respond to a wake-up event. For this reason, and to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the TJA1145 switches to Sleep mode. Otherwise the TJA1145 will switch to Standby mode in response to a go-to-sleep command (MC = 001).

6.6.3 Event status and event capture registers

Table 22. Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R	0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R	0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	reserved	R	-	
0	SYSE	R	0	no pending system event
			1	system event pending at address 0x61

Table 23. System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	PO ^[1]	R/W	0	no recent power-on
			1	the TJA1145 has left Off mode after power-on
3	reserved	R	-	

Table 23. System event status register (address 61h) ...continued

Bit	Symbol	Access	Value	Description
2	OTW	R/W	0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W	0	no SPI failure detected
			1	SPI failure detected
0	reserved	R	-	

[1] PO is cleared when the TJA1145 is forced to Sleep mode due to an undervoltage event. The information stored in PO could be lost if the transition to Sleep mode was forced by an undervoltage event. Bit NMS, which is set to 0 when the TJA1145 switches to Normal mode after power-on, compensates for this.

Table 24. Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W	0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W	0	CAN bus is active
			1	no activity on CAN bus for $t_{to(silence)}$
3:2	reserved	R	-	
1	CF	R/W	0	no CAN failure event detected
			1	CAN failure event detected CF is only enabled in Normal mode while the transceiver is in CAN Active mode and is triggered if: - TXD is clamped dominant OR - a V_{CC} undervoltage is detected (when CMC = 01)
0	CW	R/W	0	no CAN wake-up event detected
			1	CAN wake-up event detected

Table 25. WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPR	R/W	0	no rising edge on WAKE pin detected
			1	rising edge on WAKE pin detected
0	WPF	R/W	0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

Table 26. System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	OTWE	R/W	0	overtemperature warning disabled
			1	overtemperature warning enabled
1	SPIFE	R/W	0	SPI failure detection disabled
			1	SPI failure detection enabled
0	reserved	R	-	

Table 27. Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W	0	CAN bus silence detection disabled
			1	CAN bus silence detection enabled
3:2	reserved	R	-	
1	CFE	R/W	0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W	0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 28. WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W	0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled
0	WPFE	R/W	0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

6.7 Device ID

A byte is reserved at address 0x7E for a TJA1145 identification code.

Table 29. Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS[7:0]	R		device identification code
			70h	TJA1145T, TJA1145TK
			74h	TJA1145T/FD, TJA1145TK/FD

6.8 Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the TJA1145 updating status registers etc.

Table 30. Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	cleared for future use
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F - partial networking data byte registers
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F
			0	SPI write-access enabled
			1	SPI write-access disabled

Table 30. Lock control register (address 0Ah) ...continued

Bit	Symbol	Access	Value	Description
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - WAKE pin configuration
			0	SPI write-access enabled
			1	SPI write-access disabled
3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control and partial networking
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F
			0	SPI write-access enabled
			1	SPI write-access disabled
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 - general purpose memory
			0	SPI write-access enabled
			1	SPI write-access disabled

6.9 General-purpose memory

TJA1145 allocates 4 bytes of RAM as general-purpose registers for storing user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09 (see [Table 31](#)).

6.10 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels of the TXD, RXD and the SPI interface pins to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

6.11 V_{CC}/V_{IO} undervoltage protection

If an undervoltage is detected on pins VCC or VIO, and it remains valid for longer than the undervoltage detection delay time, $t_{d(uvd)}$, the TJA1145 is forced to Sleep mode (see [Figure 4](#)). A number of preventative measures are taken when the TJA1145 is forced to Sleep mode to avoid deadlock and unpredictable states:

- All previously captured events (address range 0x61 to 0x64) are cleared before the TJA1145 switches to Sleep Mode to avoid repeated attempts to wake up while an undervoltage is present.
- Both CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a deadlock situation where the TJA1145 cannot be woken up after entering Sleep mode.
- Partial Networking is disabled (CPNC = 0) to ensure immediate wake-up in response to bus traffic after the TJA1145 has recovered from an undervoltage event.

- The Partial Networking Configuration bit is cleared (CPNOK = 0) to indicate that partial networking might not have been configured correctly when the TJA1145 switched to Sleep mode.

Status bit FSMS is set to 1 when a transition to Sleep mode is forced by an undervoltage event (see [Table 5](#)). This bit can be sampled after the TJA1145 wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

6.12 SPI

6.12.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock; default level is LOW due to internal pull-down
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in [Figure 10](#).

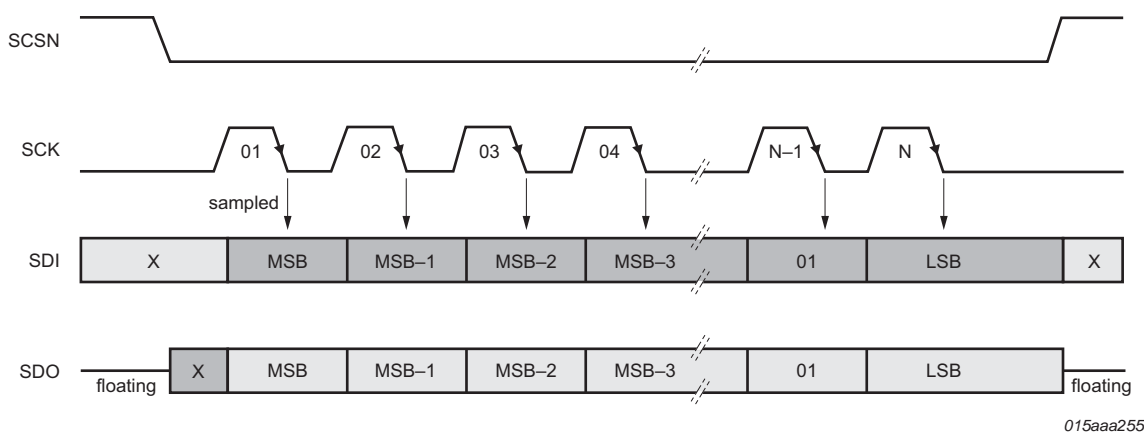


Fig 10. SPI timing protocol

The SPI data in the TJA1145 is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes must be transmitted to the TJA1145 for a single register write operation. The first byte contains the 7-bit address along with a 'read-only' bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in [Figure 11](#).

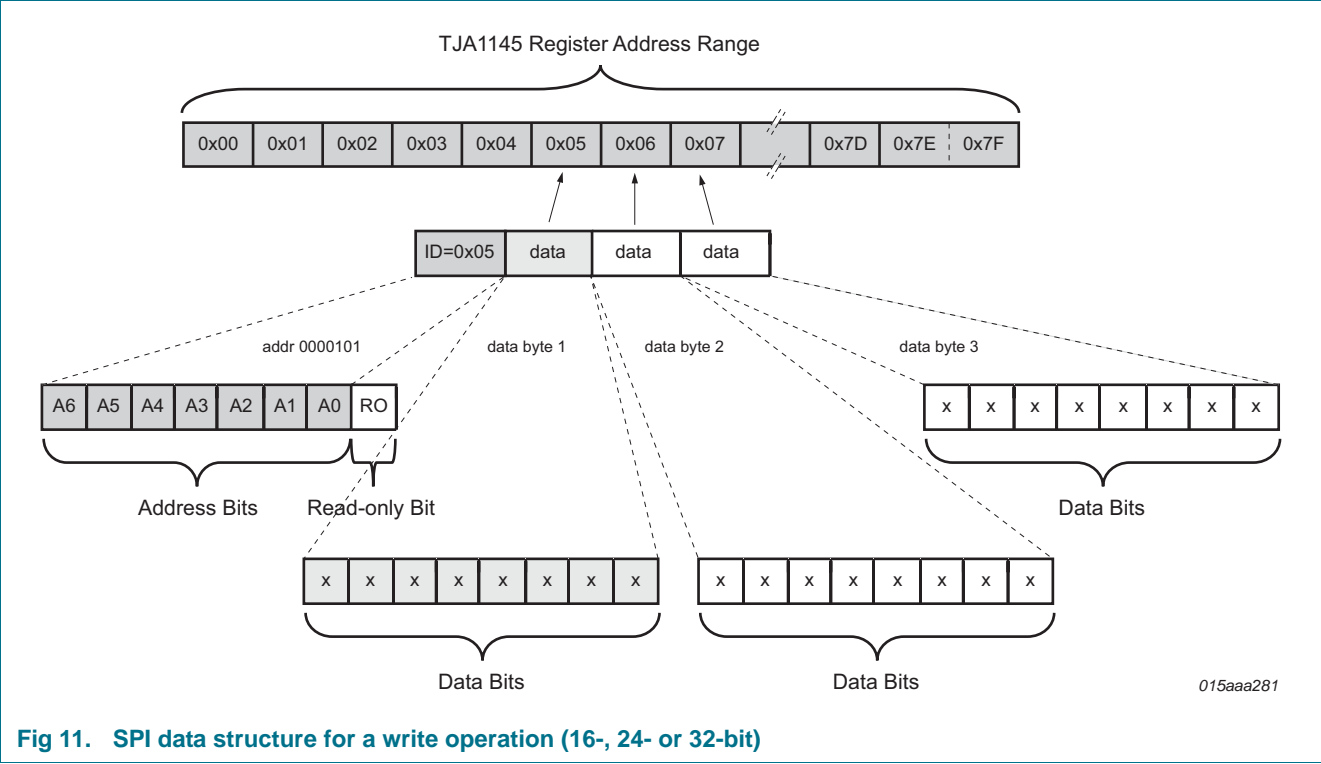


Fig 11. SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO.

The TJA1145 tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data overflows into address 0x00.

During a write operation, the TJA1145 monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

6.12.2 Register map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in [Table 31](#) to [Table 35](#). The functionality of the individual bits is discussed in more detail in relevant sections of the data sheet.

Table 31. Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x01	Mode control	reserved					MC		
0x03	Main status	FSMS	OTWS	NMS	reserved				
0x04	System event enable	reserved					OTWE	SPIFE	reserved
0x06	Memory 0	GPM[7:0]							
0x07	Memory 1	GPM[15:8]							
0x08	Memory 2	GPM[23:16]							
0x09	Memory 3	GPM[31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 32. Overview of transceiver control and partial networking registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x20	CAN control	reserved	CFDC	PNCOK	CPNC	reserved		CMC	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	reserved	VCS	CFS
0x23	Transceiver event enable	reserved			CBSE	reserved		CFE	CWE
0x26	Data rate	reserved					CDR		
0x27	Identifier 0	ID[7:0]							
0x28	Identifier 1	ID[15:8]							
0x29	Identifier 2	ID[23:16]							
0x2A	Identifier 3	reserved			ID[28:24]				
0x2B	Mask 0	M[7:0]							
0x2C	Mask 1	M[15:8]							
0x2D	Mask 2	M[23:16]							
0x2E	Mask 3	reserved			M[28:24]				
0x2F	Frame control	IDE	PNDM	reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

Table 33. Overview of WAKE pin control and status registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x4B	WAKE pin status	reserved						WPVS	reserved
0x4C	WAKE pin enable	reserved						WPRE	WPFE

Table 34. Overview of Event Capture registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Event capture status	reserved				WPE	TRXE	reserved	SYSE
0x61	System event status	reserved			PO	reserved	OTW	SPIF	reserved
0x63	Transceiver event status	reserved		PNFDE	CBS	reserved		CF	CW
0x64	WAKE pin event status	reserved						WPR	WPF

Table 35. Overview of Identification register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7E	Identification	IDS[7:0]							

6.12.3 Register configuration in TJA1145 operating modes

A number of register bits may change state automatically when the TJA1145 switches from one operating mode to another. This is particularly evident when the TJA1145 switches to Off mode or when an undervoltage event forces a transition to Sleep mode. These changes are summarized in [Table 36](#). If an SPI transmission is in progress when the TJA1145 changes state, the transmission is ignored (automatic state changes have priority).

Table 36. Register bit settings in TJA1145 operating modes

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtmp	Forced Sleep (uv)
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
FSMS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change

Table 36. Register bit settings in TJA1145 operating modes ...continued

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtmp	Forced Sleep (uv)
IDE	0	no change	no change	no change	no change	no change
IDS	01110000	01110000	01110000	01110000	01110000	01110000
LKnC	0	no change	no change	no change	no change	no change
Mn	00000000	no change	no change	no change	no change	no change
MC	100	100	111	001	don't care	001
NMS	1	no change	0	no change	no change	no change
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0
PO	1	no change	no change	no change	no change	0
SPIF	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	0
TRXE	0	no change	no change	no change	no change	0
VCS	0	actual state	actual state	actual state	actual state	actual state
WPE	0	no change	no change	no change	no change	0
WPF	0	no change	no change	no change	no change	0
WPFE	0	no change	no change	no change	no change	1
WPR	0	no change	no change	no change	no change	0
WPRE	0	no change	no change	no change	no change	1
WPVS	0	no change	no change	no change	no change	no change

7. Limiting values

Table 37. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	DC value			
		pins VCC, VIO	[1] -0.2	+6	V
		pins TXD, RXD, SDI, SDO, SCK, SCSN	-0.2	$V_{IO} + 0.2$	V
		pins WAKE, INH	-18	+40	V
		pin BAT	-0.2	+40	V
		pins CANH and CANL with respect to any other pin	-58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V

Table 37. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{trt}	transient voltage	on pins BAT via reverse polarity diode and capacitor to ground CANL, CANH, WAKE	[2] -150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[3]		
		on pins CANH and CANL; pin BAT with capacitor; pin WAKE with 10 nF capacitor and 10 k Ω resistor	-6	+6	kV
		HBM	[4]		
		on pins CANH, CANL	[5] -8	+8	kV
		on pins BAT, WAKE	-4	+4	kV
		on any other pin	-2	+2	kV
		MM	[6]		
		on any pin	-100	+100	V
		CDM	[7]		
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature		[8] -40	+150	°C
T_{stg}	storage temperature		-55	+150	°C

[1] When the device is not powered up, $I_{\text{VCC(max)}}$ = 25 mA.

[2] Verified by an external test house to ensure pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.

[3] ESD performance according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house; the result was equal to or better than ± 6 kV.[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 k Ω).

[5] VCC, VIO and BAT connected to GND, emulating the application circuit.

[6] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μ H, 10 Ω).

[7] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{\text{vj}} = T_{\text{amb}} + P \times R_{\text{th(j-a)}}$, where $R_{\text{th(j-a)}}$ is a fixed value used in the calculation of T_{vj} . The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

8. Thermal characteristics

Table 38. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{\text{th(vj-a)}}$	thermal resistance from virtual junction to ambient	SO14	[1] 106	K/W
		HVSON14	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μ m) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μ m).

9. Static characteristics

Table 39. Static characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BAT} = 4.5\text{ V}$ to 28 V ; $V_{IO} = 2.85\text{ V}$ to 5.5 V ; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 60\text{ }\Omega$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BAT} = 13\text{ V}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
V _{th(det)pon}	power-on detection threshold voltage	V _{BAT} rising	4.2	-	4.55	V
V _{th(det)poff}	power-off detection threshold voltage	V _{BAT} falling	2.8	-	3	V
V _{uvr(CAN)}	CAN undervoltage recovery voltage	V _{BAT} rising	4.5	-	5	V
V _{uvd(CAN)}	CAN undervoltage detection voltage	V _{BAT} falling	4.2	-	4.55	V
I _{BAT}	battery supply current	Sleep mode; MC = 001; CWE = 1; CAN Offline mode; −40 °C < T _{vj} < 85 °C; V _{BAT} = 7 V to 18 V	-	40	59	μA
		Standby mode; MC = 100; CWE = 1; CAN Offline mode; −40 °C < T _{vj} < 85 °C; V _{BAT} = 7 V to 18 V	-	44	68	μA
		additional current in CAN Offline Bias mode; −40 °C < T _{vj} < 85 °C	-	46	63	μA
		additional current when partial networking enabled; bus active; CPNC = 1; PNCOK = 1	-	300	400	μA
		additional current from WAKE input; WPRE = WPFE = 1; −40 °C < T _{vj} < 85 °C		2	3	μA
		Normal mode; MC = 111	-	1	1.5	mA
Supply; pin VCC						
V _{uvd(VCC)}	undervoltage detection voltage on pin VCC		4.5	-	4.75	V
I _{CC}	supply current	CAN Active mode; CAN recessive; V _{TXD} = V _{IO}	-	3	6	mA
		CAN Active mode; CAN dominant; V _{TXD} = 0 V	-	45	65	mA
		Standby/Normal mode; CAN inactive; −40 °C < T _{vj} < 85 °C	-	4.7	8.5	μA
		Sleep mode; CAN inactive; −40 °C < T _{vj} < 85 °C	-	3.8	7	μA
Supply; pin VIO						
V _{uvd(VIO)}	undervoltage detection voltage on pin VIO	V _{BAT} > 4.5 V	2.7	-	2.85	V

Table 39. Static characteristics ...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BAT} = 4.5\text{ V}$ to 28 V ; $V_{IO} = 2.85\text{ V}$ to 5.5 V ; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 60\text{ }\Omega$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BAT} = 13\text{ V}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{I(VIO)}	input current on pin VIO	Standby/Normal mode; −40 °C < T _{vj} < 85 °C	-	7.1	11	μA
		Sleep mode; −40 °C < T _{vj} < 85 °C	-	5	8	μA
Serial peripheral interface inputs; pins SDI, SCK and SCSN						
V _{th(sw)}	switching threshold voltage	V _{IO} = 2.97 V to 5.5 V	0.25V _{IO}	-	0.75V _{IO}	V
R _{pd(SCK)}	pull-down resistance on pin SCK		40	60	80	kΩ
R _{pu(SCSN)}	pull-up resistance on pin SCSN		40	60	80	kΩ
I _{LI(SDI)}	input leakage current on pin SDI		−5	-	+5	μA
Serial peripheral interface data output; pin SDO						
V _{OH}	HIGH-level output voltage	I _{OH} = −4 mA	V _{IO} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	I _{OL} = 4 mA	-	-	0.4	V
I _{LO(off)}	off-state output leakage current	V _{SCSN} = V _{IO} ; V _O = 0 V to V _{IO}	−5	-	+5	μA
Inhibit output: pin INH						
V _O	output voltage	I _{INH} = −180 μA	V _{BAT} − 0.8	-	V _{BAT}	V
R _{pd}	pull-down resistance	Sleep mode	3	4	5	MΩ
CAN transmit data input; pin TXD						
V _{th(sw)}	switching threshold voltage	V _{IO} = 2.97 V to 5.5 V	0.25V _{IO}	-	0.75V _{IO}	V
R _{pu}	pull-up resistance		40	60	80	kΩ
CAN receive data output; pin RXD						
V _{OH}	HIGH-level output voltage	I _{OH} = −4 mA	V _{IO} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	I _{OL} = 4 mA	-	-	0.4	V
R _{pu}	pull-up resistance	CAN Offline mode	40	60	80	kΩ
Local wake input; pin WAKE						
V _{th(sw)r}	rising switching threshold voltage		2.8	-	4.1	V
V _{th(sw)f}	falling switching threshold voltage		2.4	-	3.75	V
V _{hys(i)}	input hysteresis voltage		250	-	800	mV
I _i	input current	T _{vj} = −40 °C to +85 °C	-	-	1.5	μA
High-speed CAN bus lines; pins CANH and CANL						
V _{O(dom)}	dominant output voltage	CAN Active mode; V _{TXD} = 0 V				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
V _{dom(TX)sym}	transmitter dominant voltage symmetry	V _{dom(TX)sym} = V _{CC} − V _{CANH} − V _{CANL} ; V _{CC} = 5 V	−400	-	+400	mV
V _{TXsym}	transmitter voltage symmetry	V _{TXsym} = V _{CANH} + V _{CANL} ; f _{TXD} = 250 kHz; C _{SPLIT} = 4.7 nF	[1] 0.9V _{CC} [2]	-	1.1V _{CC}	V

Table 39. Static characteristics ...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BAT} = 4.5\text{ V}$ to 28 V ; $V_{IO} = 2.85\text{ V}$ to 5.5 V ; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 60\text{ }\Omega$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BAT} = 13\text{ V}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(dif)bus}$	bus differential output voltage	CAN Active mode (dominant); $V_{TXD} = 0\text{ V}$; $V_{CC} = 4.75\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 45\text{ }\Omega$ to $65\text{ }\Omega$	1.5	-	3.0	V
		CAN Active mode (recessive); CAN Listen-only mode; CAN Offline mode; $V_{TXD} = V_{IO}$; $R_{(CANH-CANL)} = \text{no load}$	-50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	CAN Active mode; $V_{TXD} = V_{IO}$; $R_{(CANH-CANL)} = \text{no load}$	2	$0.5V_{CC}$	3	V
		CAN Offline mode; $R_{(CANH-CANL)} = \text{no load}$	-0.1	-	+0.1	V
		CAN Offline Bias/Listen-only modes; $R_{(CANH-CANL)} = \text{no load}$; $V_{CC} = 0\text{ V}$	2	2.5	3	V
$I_{O(dom)}$	dominant output current	CAN Active mode; $V_{TXD} = 0\text{ V}$; $V_{CC} = 5\text{ V}$				
		pin CANH; $V_{CANH} = 0\text{ V}$	-50	-	-	mA
		pin CANL; $V_{CANL} = 5\text{ V}$	-	-	52	mA
$I_{O(rec)}$	recessive output current	$V_{CANL} = V_{CANH} = -27\text{ V}$ to $+32\text{ V}$; $V_{TXD} = V_{IO}$	-3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	CAN Active/Listen-only modes; $V_{CANL} = V_{CANH} = -12\text{ V}$ to $+12\text{ V}$	0.5	0.7	0.9	V
		CAN Offline mode; $V_{CANL} = V_{CANH} = -12\text{ V}$ to $+12\text{ V}$	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active/Listen-only modes; $V_{CANL} = V_{CANH} = -12\text{ V}$ to $+12\text{ V}$	50	200	400	mV
$R_{i(cm)}$	common-mode input resistance		9	15	28	k Ω
ΔR_i	input resistance deviation		-1	-	+1	%
$R_{i(dif)}$	differential input resistance	$V_{CANL} = V_{CANH} = -12\text{ V}$ to $+12\text{ V}$	19	30	52	k Ω
$C_{i(cm)}$	common-mode input capacitance	[1]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[1]	-	-	10	pF
I_{LI}	input leakage current	$V_{BAT} = V_{CC} = 0\text{ V}$ or $V_{BAT} = V_{CC}$ = shorted to ground via $47\text{ k}\Omega$; $V_{CANH} = V_{CANL} = 5\text{ V}$	-5	-	+5	μA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	$^{\circ}\text{C}$
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	$^{\circ}\text{C}$
$T_{th(warn)otp}$	overtemperature protection warning threshold temperature		127	137	147	$^{\circ}\text{C}$

[1] Not tested in production; guaranteed by design.

[2] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in [Figure 16](#).

10. Dynamic characteristics

Table 40. Dynamic characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BAT} = 4.5\text{ V}$ to 28 V ; $V_{IO} = 2.85\text{ V}$ to 5.5 V ; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 60\text{ }\Omega$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BAT} = 13\text{ V}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage sources; pins BAT, VCC and VIO						
t _{startup}	start-up time	from V _{BAT} exceeding the power-on detection threshold until INH active	-	2.8	4.7	ms
t _{d(uvd)}	undervoltage detection delay time		6	-	39	μs
t _{d(uvd-sleep)}	delay time from undervoltage detection to sleep mode	from undervoltage detection on VCC and/or VIO until TJA1145 forced to Sleep mode	200	-	400	ms
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO in Normal and Standby modes						
t _{cy(clk)}	clock cycle time	Normal/Standby modes	250	-	-	ns
		Sleep mode	1	-	-	μs
t _{SPILEAD}	SPI enable lead time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
t _{SPILAG}	SPI enable lag time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
t _{clk(H)}	clock HIGH time	Normal/Standby modes	125	-	-	ns
		Sleep mode	500	-	-	ns
t _{clk(L)}	clock LOW time	Normal/Standby modes	125	-	-	ns
		Sleep mode	500	-	-	ns
t _{su(D)}	data input set-up time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
t _{h(D)}	data input hold time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
t _{v(Q)}	data output valid time	pin SDO; C _L = 20 pF; Normal/Standby modes	-	-	50	ns
		pin SDO; C _L = 20 pF; Sleep mode	-	-	200	ns
t _{WH(S)}	chip select pulse width HIGH	pin SCSN; Normal/Standby modes	250	-	-	ns
		pin SCSN; Sleep mode	1	-	-	μs
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
t _{d(TXD-RXD)}	delay time from TXD to RXD	50 % V _{TXD} to 50 % V _{RXD} ; C _{RXD} = 15 pF; f _{TXD} = 250 kHz	-	-	255	ns
t _{d(TXD-busdom)}	delay time from TXD to bus dominant		-	80	-	ns
t _{d(TXD-busrec)}	delay time from TXD to bus recessive		-	80	-	ns
t _{d(busdom-RXD)}	delay time from bus dominant to RXD	C _{RXD} = 15 pF	-	105	-	ns
t _{d(busrec-RXD)}	delay time from bus recessive to RXD	C _{RXD} = 15 pF	-	120	-	ns

Table 40. Dynamic characteristics ...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BAT} = 4.5\text{ V}$ to 28 V ; $V_{IO} = 2.85\text{ V}$ to 5.5 V ; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $R_{(CANH-CANL)} = 60\text{ }\Omega$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BAT} = 13\text{ V}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	μs
		second pulse for wake-up on pins CANH and CANL	0.5	-	3.0	μs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	μs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	3.0	μs
$t_{to(wake)}$	wake-up time-out time	between first and second dominant pulses; CAN Offline mode	570	-	1200	μs
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; $V_{TXD} = 0\text{ V}$	2.7	-	3.3	ms
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes; $R_L = 120\text{ }\Omega$	0.95	-	1.17	s
$t_d(busact-bias)$	delay time from bus active to bias		-	-	200	μs
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = 1)	-	-	220	μs
Pin RXD: interrupt/wake-up event timing (valid in CAN Offline mode only) change to interrupt response time						
$t_d(event)$	event capture delay time	CAN Offline mode	0.9	-	1.1	ms
t_{blank}	blanking time	when switching from Offline to Active/Listen-only mode	-	-	25	μs
Pin WAKE						
t_{wake}	wake-up time		7	-	42	μs
Pin INH						
$t_d(buswake-INHH)$	delay time from bus wake-up to INH HIGH		-	-	100	μs

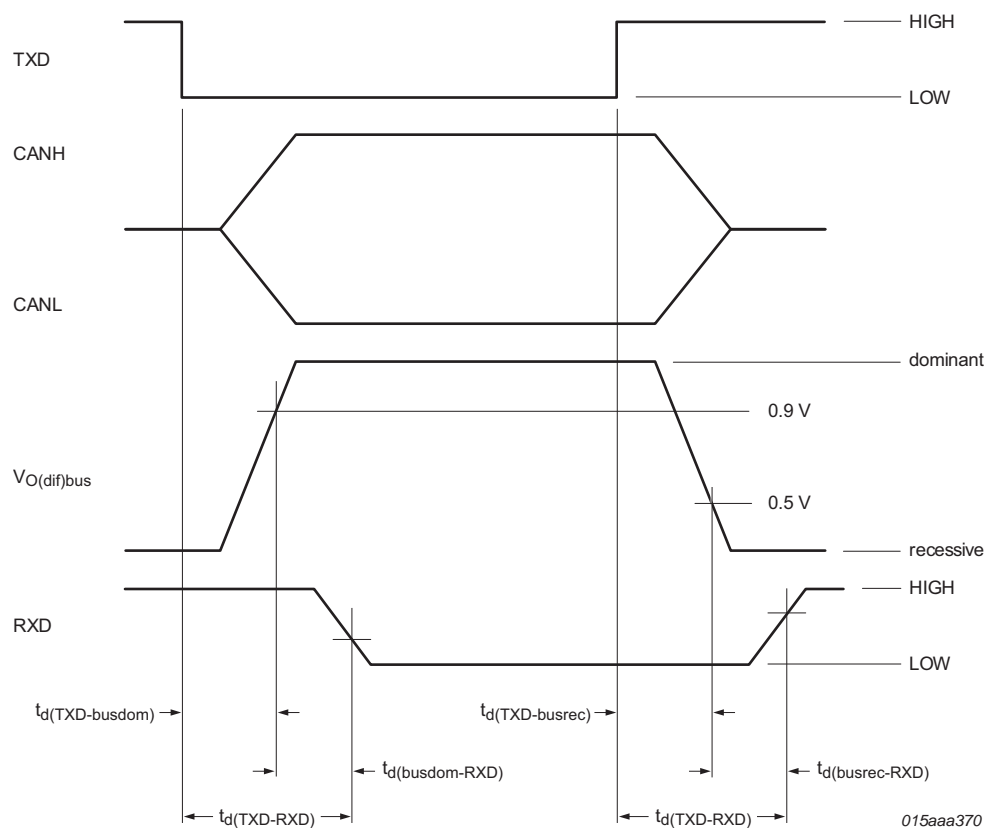


Fig 12. CAN transceiver timing diagram

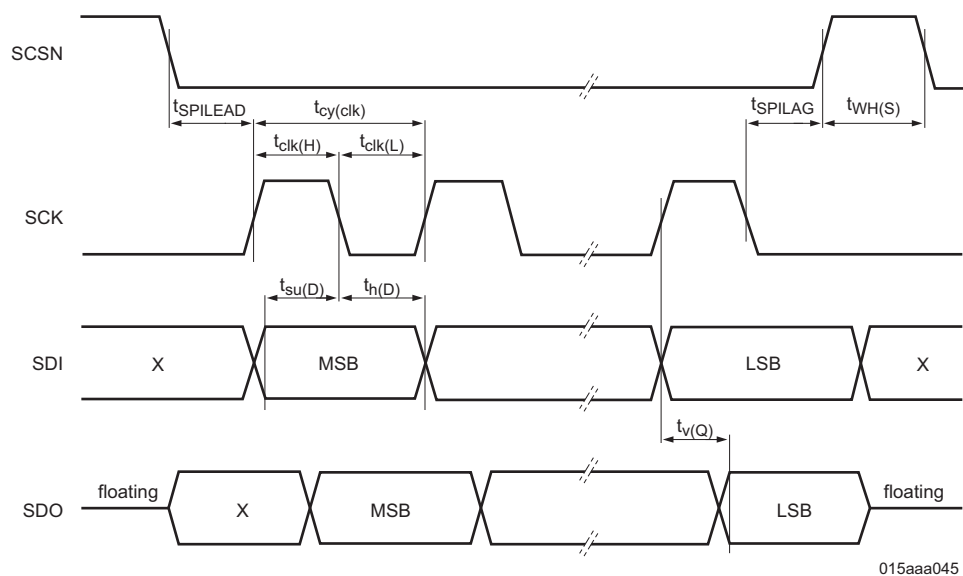
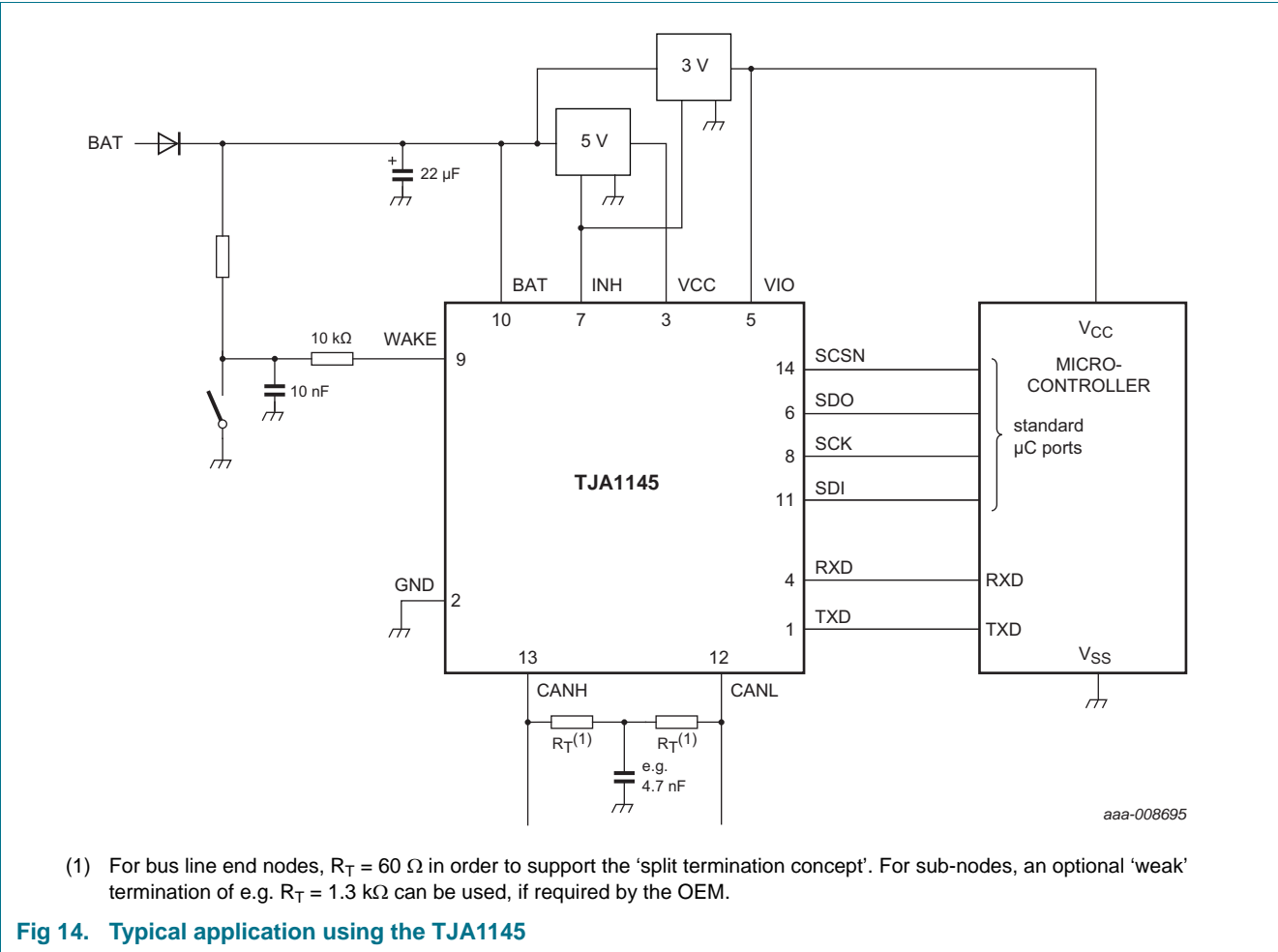


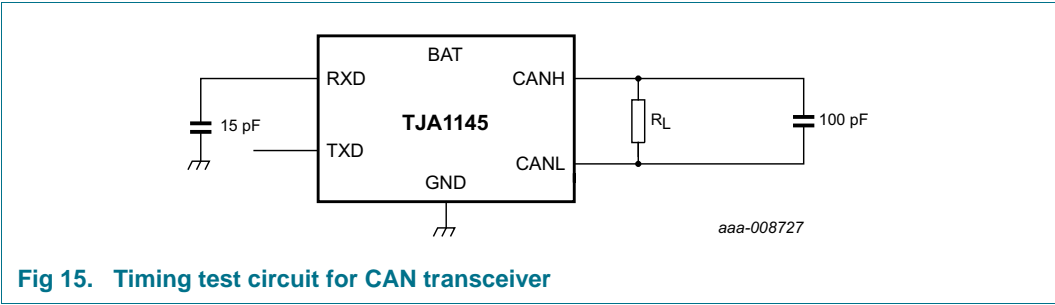
Fig 13. SPI timing diagram

11. Application information

11.1 Application diagram



12. Test information



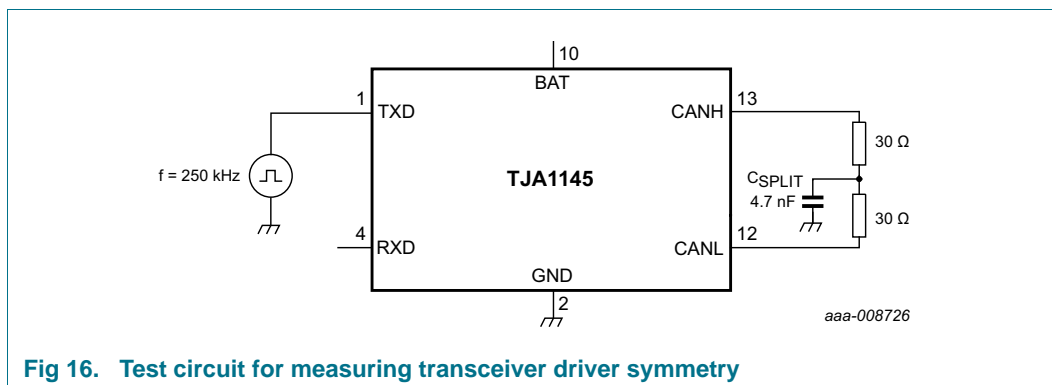


Fig 16. Test circuit for measuring transceiver driver symmetry

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1

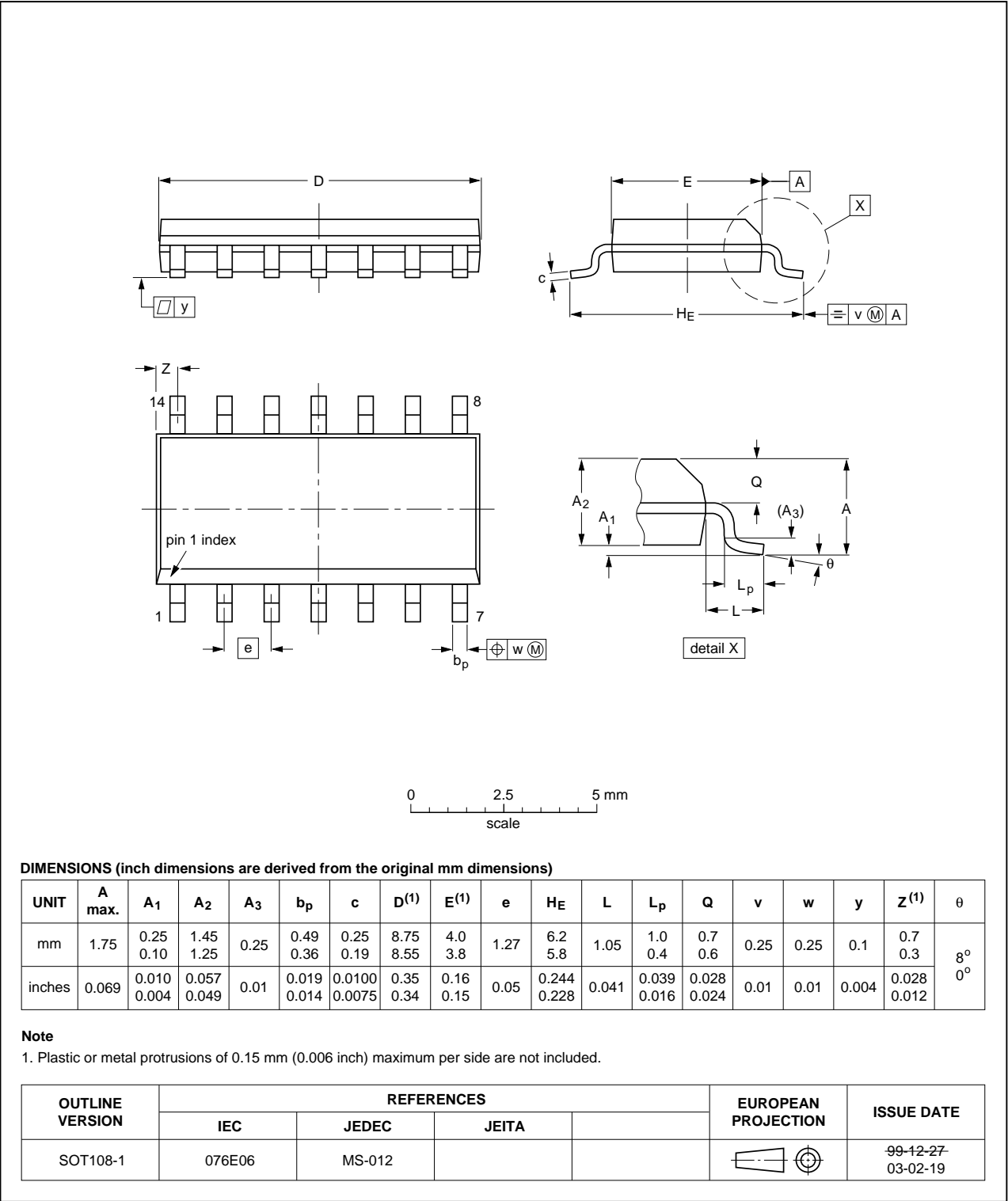


Fig 17. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads;
14 terminals; body 3 x 4.5 x 0.85 mm

SOT1086-2

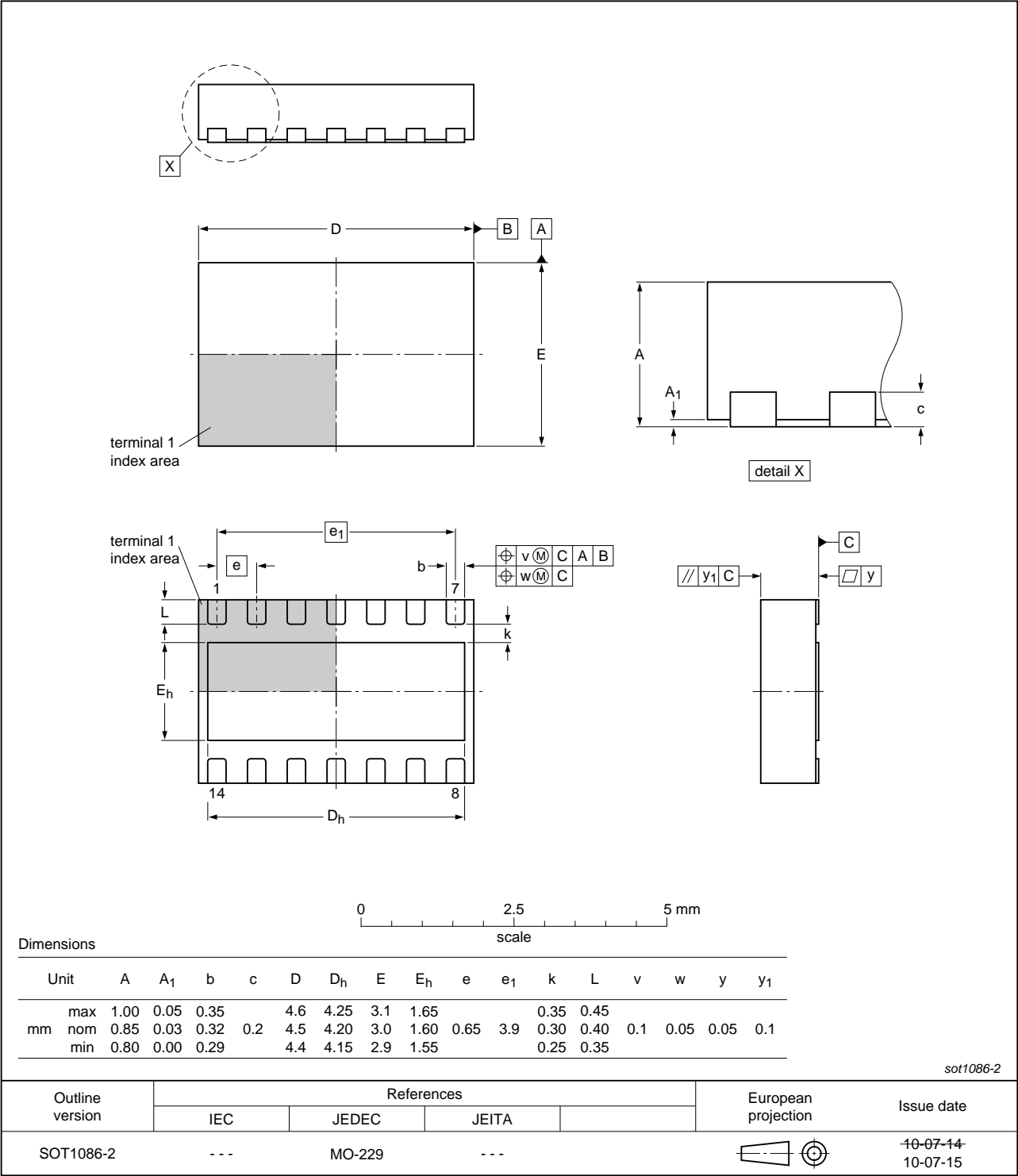


Fig 18. Package outline SOT1086-2 (HVSON14)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 41](#) and [42](#)

Table 41. SnPb eutectic process (from J-STD-020D)

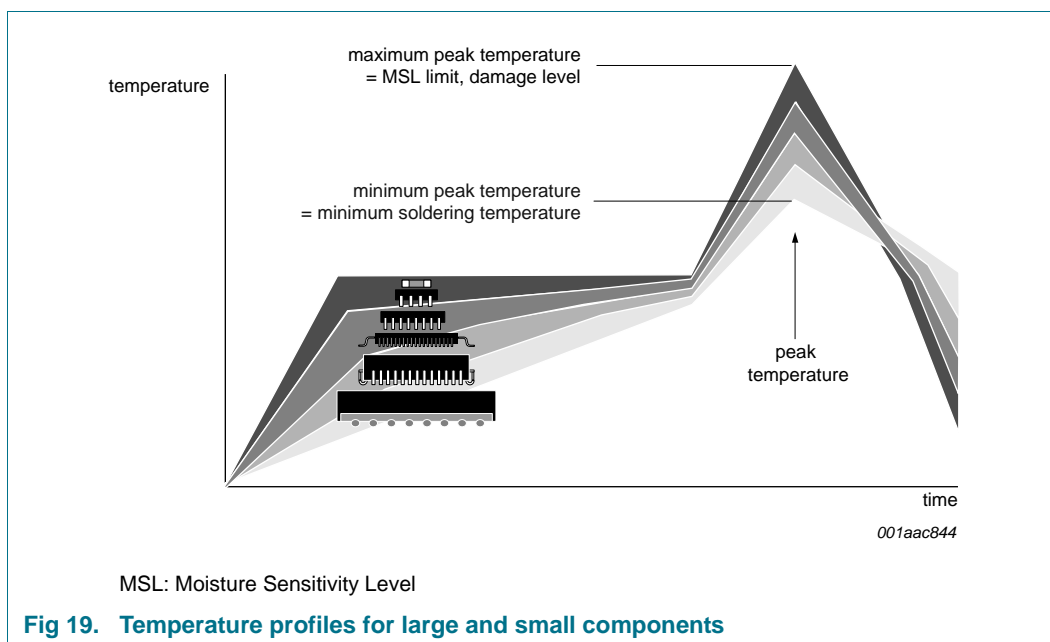
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 42. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

16. Soldering of HVSON packages

[Section 15](#) contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- *AN10365* “Surface mount reflow soldering description”
- *AN10366* “HVQFN application information”

17. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1145 v.1	20130927	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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