DATA SHEET

Part No.	MN5B02UC
Package Code No.	TQFP048-P-0707B

SEMICONDUCTOR COMPANY
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

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MN5B02UC

ICs for audio common use

■ Overview

- The MN5B02UC performs digital signal processing for 5.1-channel and 2-channel audio signals output from DVD, CD, MD, MP3, and other decoders to generate 3D playback with remarkable presence for output to stereo headphones.
- It offers 3 setting modes (Music, Cinema, Voice), allowing 3D effects to be configured to fit individual sources.

■ Features

- 3D sound effect settings: Music, Cinema, Voice, (Down mix (3D sound effect: OFF))
- Sampling frequency: 48 kHz / 44.1 kHz
- Audio serial input: 5.1-ch. (L, C, R, LS, RS, LFE) / 2-ch. (L, R)
- Audio serial output: 2-ch. (L, R)
- External memory: Not necessary
- Microcontroller interface (Serial): Control register settings
- Parallel interface: Control register settings
- Internal operating frequency: Approx. 50 MHz (with external clock)
- External clock: 512 fs / 256 fs
- Power save mode: PLL clock stopped
- Power supply: 3.3 V (External I/O), 1.5 V (Internal circuit)

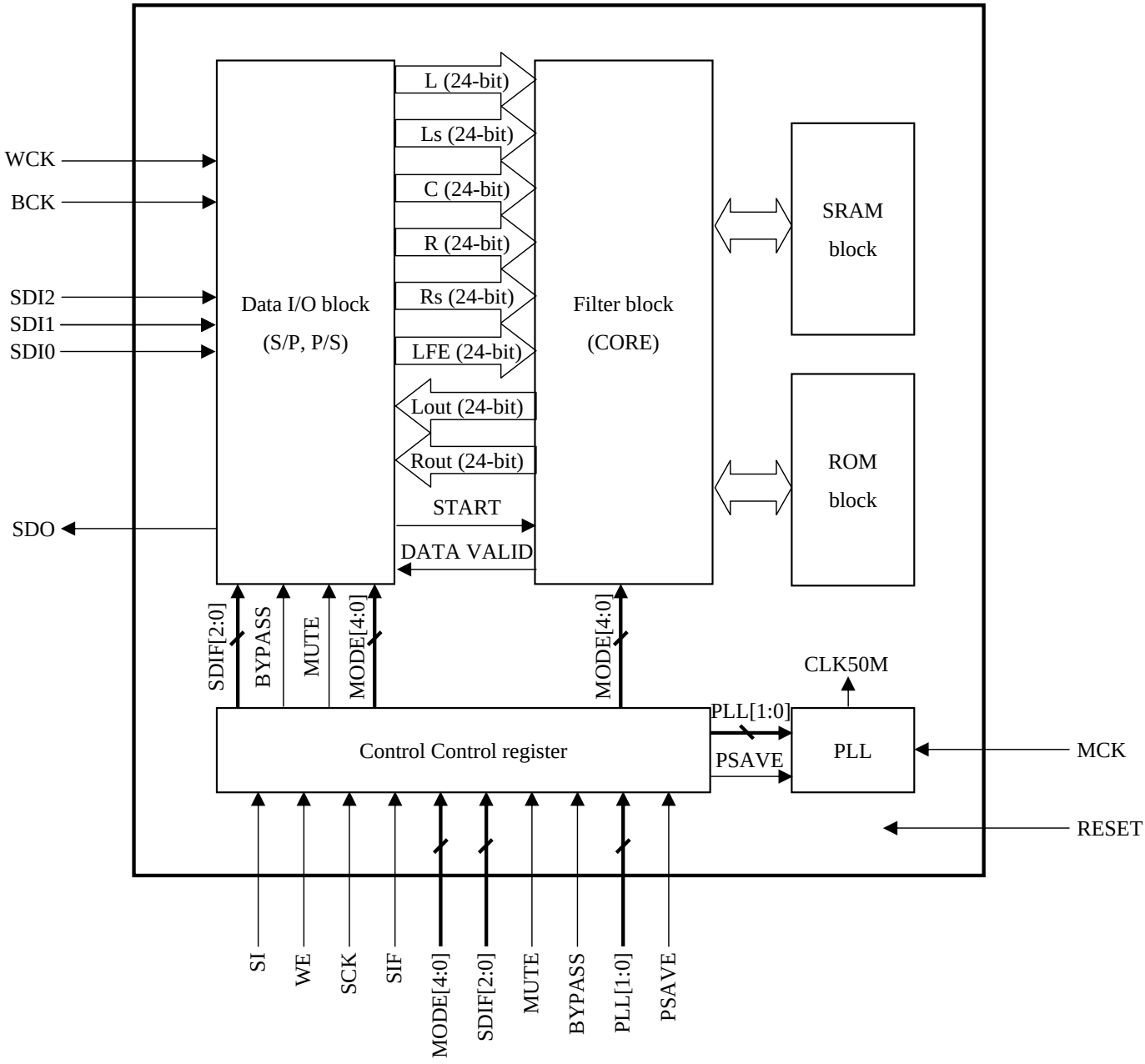
■ Applications

- Audio equipment, Portable DVD player, Headphone etc.

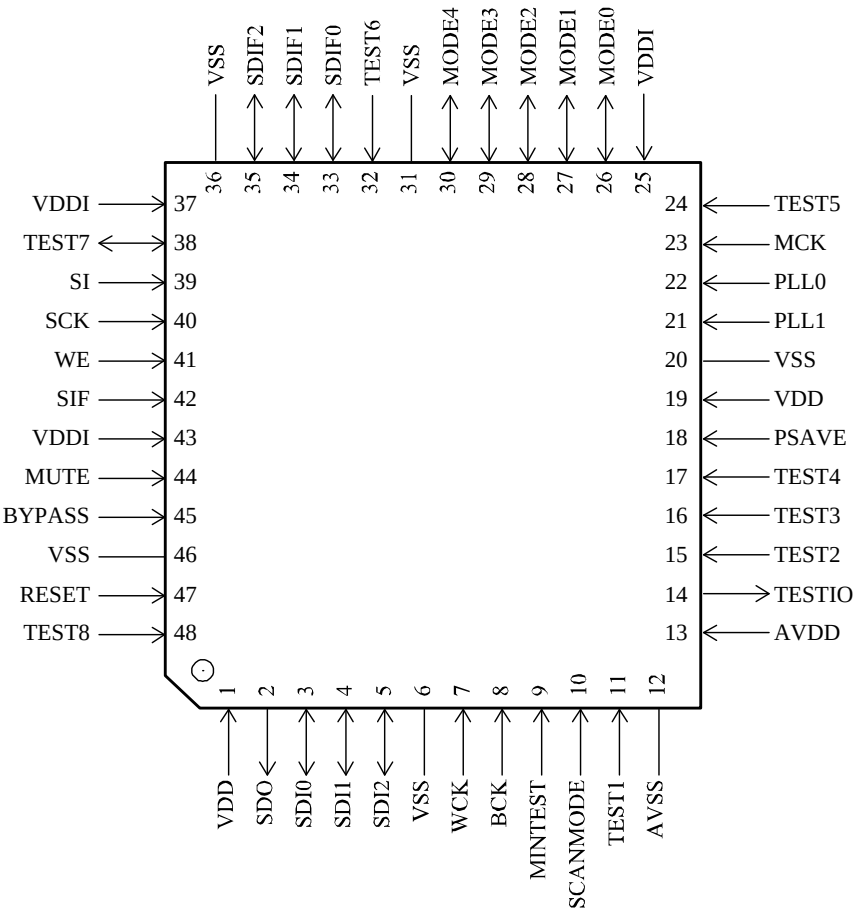
■ Package

- 48-pin TQFP (7 mm × 7 mm)

■ Block Diagram



■ Pin Arrangement



Note) All supply pins (VDD, VSS, VDDI, AVDD, AVSS) must be fixed.
Connect MINTEST pin VSS.

■ Pin Descriptions

Block	Pin No.	Symbol	I/O	Description
Audio input	7	WCK	I	Word clock for audio data input
	8	BCK	I	Bit clock for audio data I/O
	3	SDI0	I	Audio data serial input (L, R)
	4	SDI1	I	Audio data serial input (LS, RS)
	5	SDI2	I	Audio data serial input (C, LFE)
Audio output	2	SDO	O	Audio data serial output (L, R)
Serial microcontroller interface	40	SCK	I	Serial data I/O clock
	39	SI	I	Control register data input
	41	WE	I	Write enable (low active)
Parallel interface	42	SIF	I	Serial (low) / parallel (high) interface selection
	30	MODE4	I	Operating mode setting ・3D sound effect (Music, Cinema, Voice, (Down mix)) ・Number of input channels ・Sampling frequency
	29	MODE3	I	
	28	MODE2	I	
	27	MODE1	I	
	26	MODE0	I	
	35	SDIF2	I	Audio data I/O format setting
	34	SDIF1	I	
	33	SDIF0	I	
	44	MUTE	I	L, R output signal mute setting (high: mute ON)
	45	BYPASS	I	L, R input bypass output setting (high: bypass ON)
	18	PSAVE	I	Power save pin (low: PLL clock stopped)
	21	PLL1	I	PLL clock selection pin
	22	PLL0	I	
PLL	23	MCK	I	Operating clock input pin
Reset	47	RESET	I	System reset (low: reset ON)
Power supply	1	V_{DD}	—	+3.3 V external supply voltage
	19	V_{DD}	—	+3.3 V external supply voltage
	25	V_{DDI}	—	+1.5 V internal supply voltage
	37	V_{DDI}	—	+1.5 V internal supply voltage
	43	V_{DDI}	—	+1.5 V internal supply voltage
	13	AV_{DD}	—	+3.3 V external supply voltage (PLL)

■ Pin Descriptions (continued)

Block	Pin No.	Symbol	I/O	Description
Ground	6	V_{SS}	—	Ground
	20	V_{SS}	—	Ground
	31	V_{SS}	—	Ground
	36	V_{SS}	—	Ground
	46	V_{SS}	—	Ground
	12	AV_{SS}	—	Ground (PLL)
Test	9	MINTEST	I	Test pin (Connect to ground)
	10	SCANMODE	I	Test pin (Connect to ground)
	11	TEST1	I	Test pin (Connect to ground)
	14	TESTIO	O	Test pin (Not connected)
	15	TEST2	I	Test pin (Connect to ground)
	16	TEST3	I	Test pin (Connect to ground)
	17	TEST4	I	Test pin (Connect to ground)
	24	TEST5	I	Test pin (Connect to ground)
	32	TEST6	I	Test pin (Connect to ground)
	38	TEST7	I/O	Test pin (Not connected)
	48	TEST8	I	Test pin (Connect to ground)

■ Absolute Maximum Ratings $V_{SS} = AV_{SS} = 0$ V

	Parameter		Symbol	Rating	Unit
A1	External supply voltage *		V_{DD}	– 0.3 to +4.6	V
A2			AV_{DD}	– 0.3 to +4.6	
A3	Internal supply voltage *		V_{DDI}	– 0.3 to +2.0	V
A4	Input voltage		V_I	– 0.3 to V_{DD} + 0.3 (max. 4.6)	V
A5			V_{IA}	– 0.3 to AV_{DD} + 0.3 (max. 4.6)	
A6	Output voltage		V_O	– 0.3 to V_{DD} + 0.3 (max. 4.6)	V
A7	Output current	TYPE-HL2	I_O	±6	mA
A8		TYPE-HL4		±12	
A9	Input current power supply		I_V	±70 / pin	mA
A10	Power dissipation		P_D	410	mW
A11	Operating temperature		T_{opr}	–30 to +85	°C
A12	Storage temperature		T_{stg}	–50 to +150	°C

Note) 1. TYPE-HL2: BCK, SDI0 to SDI2, MODE0 to MODE4, SDIF0 to SDIF2
TYPE-HL4: SDO
2. The max. and min. limits define the range within which the chip is safe.
However the chip is not guaranteed to operate at the boundary conditions.
3. All power supply pins are connected directly to each power units or ground.
4. MINTEST pin are connected to V_{SS} .
5. * : In case of either V_{DD} or V_{DDI} is off, output turn out unfixed condition by flow-through current.
There is no regulations connected with power on/off (V_{DD} , V_{DDI}) sequence. But please power on (V_{DD} , V_{DDI}) at the same time.

■ Recommended Operating Range $V_{SS} = AV_{SS} = 0$ V

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
B1	External supply voltage	V_{DD}		3.0	3.3	3.6	V
B2		AV_{DD}		3.0	3.3	3.6	V
B3	Internal supply voltage	V_{DDI}		1.35	1.5	1.65	V
B4	Ambient temperature	T_a		–30		85	°C
B5	Input rise time	t_r		0		80	ns
B6	Input fall time	r_f		0		80	ns

■ Input/output capacitance

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
C1	Input terminal	C_{IN}	$V_{DD} = V_{DDI} = AV_{DD} = V_I = 0$ V, f = 1 MHz, T_a = 25°C		5	7	pF
C2	Output terminal	C_{OUT}			5	7	pF
C3	I/O terminal	C_{IO}			5	7	pF

■ Electrical Characteristics

V_{DD} = 3.0 V to 3.6 V, AV_{DD} = 3.0 V to 3.6 V, V_{DDI} = 1.35 V to 1.65 V, V_{SS} = 0 V, AV_{SS} = 0 V, f_{TEST} = 56 MHz, T_a = –30°C to +85°C

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D1	Static supply current	I_{DDS}	V_I (pull up) = Open, V_I (pull down) = Open, Input pins and bi-directional pins in the Hi-Z state are simultaneously connected to either V_{DD} or V_{SS} input levels.			20	mA
D2	Operating power consumption	P_{DDO}	$V_I = V_{DD}$ or V_{SS} , f = 56 MHz, V_{DD} = 3.3 V, AV_{DD} = 3.3 V, V_{DDI} = 1.5 V, External load = 65 pF output open		85	170	mW
Input LVCMOS level: SI, WE, MCK, PLL0, PLL1, SCK, SIF, WCK, MUTE, PSAVE, BYPASS, RESET, BCK							
D3	Input voltage high level	V_{IH}		$V_{DD} \times 0.7$		V_{DD}	V
D4	Input voltage low level	V_{IL}		0		$V_{DD} \times 0.3$	V
D5	Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}			±5	µA
Input LVCMOS level with pull-down resistor: MINTEST, TEST1 to TEST6, SCANMODE, TEST8							
D6	Input voltage high level	V_{IH}		$V_{DD} \times 0.7$		V_{DD}	V
D7	Input voltage low level	V_{IL}		0		$V_{DD} \times 0.3$	V
D8	Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
D9	Input leakage current	I_{LIL}	$V_I = V_{SS}$			±10	µA
Output pushpull: SDO							
D10	Output voltage high level	V_{OH}	I_{OH} = –4.0 mA, $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$			V
D11	Output voltage low level	V_{OL}	I_{OL} = 4.0 mA, $V_I = V_{DD}$ or V_{SS}			0.4	V
Input/output LVCMOS level: SDI0 to SDI2, MODE0 to MODE4, SDIF0 to SDIF2							
D12	Input voltage high level	V_{IH}		$V_{DD} \times 0.7$		V_{DD}	V
D13	Input voltage low level	V_{IL}		0		$V_{DD} \times 0.3$	V
D14	Output voltage high level	V_{OH}	I_{OH} = –2.0 mA, $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$			V
D15	Output voltage low level	V_{OL}	I_{OL} = 2.0 mA, $V_I = V_{DD}$ or V_{SS}			0.4	V
D16	Output leakage current	I_{LO}	V_O = Hi-Z, $V_I = V_{DD}$ or V_{SS} , $V_O = V_{DD}$ or V_{SS}			±5	µA

■ Electrical Characteristics (continued)

V_{DD} = 3.0 V to 3.6 V, AV_{DD} = 3.0 V to 3.6 V, V_{DDI} = 1.35 V to 1.65 V, V_{SS} = 0 V, AV_{SS} = 0 V, f_{TEST} = 56 MHz, T_a = –30°C to +85°C

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Input/output LVCMOS level with pull-down resistor: TEST7							
D17	Input voltage high level	V_{IH}		$V_{DD} \times 0.7$		V_{DD}	V
D18	Input voltage low level	V_{IL}		0		$V_{DD} \times 0.3$	V
D19	Output voltage high level	V_{OH}	I_{OH} = –2.0 mA, $V_I = V_{DD}$ or V_{SS}	$V_{DD} - 0.6$			V
D20	Output voltage low level	V_{OL}	I_{OL} = 2.0 mA, $V_I = V_{DD}$ or V_{SS}			0.4	V
D21	Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
D22	Output leakage current	I_{LOL}	V_O = Pull-down, $V_I = V_{DD}$ or V_{SS} , $V_O = V_{SS}$			±10	μA

■ Clock Generator (PLL) Characteristic

V_{DD} = 3.3 V, AV_{DD} = 3.3 V, V_{DDI} = 1.50 V, V_{SS} = 0 V, AV_{SS} = 0 V, T_a = 25°C

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
E1	Input frequency	f_{IN1}			25		MHz
E2	Output frequency	F_{OUT1}	× 4		100		MHz
E3	Input frequency	f_{IN2}			12.5		MHz
E4	Output frequency	F_{OUT2}	× 8		100		MHz
E5	Input frequency	f_{IN3}			19		MHz
E6	Output frequency	F_{OUT3}	× 6		114		MHz

Note) Pin name: TESTIO a0nalog bi-direction pin

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