

74LVC1G80

Single D-type flip-flop; positive-edge trigger

Rev. 13 — 5 December 2016

Product data sheet

1. General description

The 74LVC1G80 provides a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the $\overline{Q}$ output on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G80GW	−40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G80GV	−40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G80GM	−40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G80GF	−40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74LVC1G80GN	−40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G80GS	−40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G80GX	−40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.35 mm	SOT1226

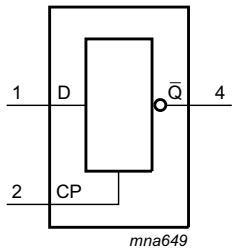
4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74LVC1G80GW	VT
74LVC1G80GV	V80
74LVC1G80GM	VT
74LVC1G80GF	VT
74LVC1G80GN	VT
74LVC1G80GS	VT
74LVC1G80GX	VT

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



The logic symbol for the 74LVC1G80 is a rectangular box. It has two inputs on the left: 'D' at pin 1 and 'CP' at pin 2. The 'CP' input has a triangle pointing to it, indicating a clock input. There is one output on the right, 'Q', at pin 4, which has a bubble (inverter) at its output. The symbol is labeled 'mna649' at the bottom.

Fig 1. Logic symbol



The IEC logic symbol for the 74LVC1G80 is a rectangular box. It has two inputs on the left: 'D' at pin 1 and 'CP' at pin 2. The 'CP' input has a triangle pointing to it, indicating a clock input. There is one output on the right, 'Q', at pin 4. The symbol is labeled '001aac523' at the bottom.

Fig 2. IEC logic symbol

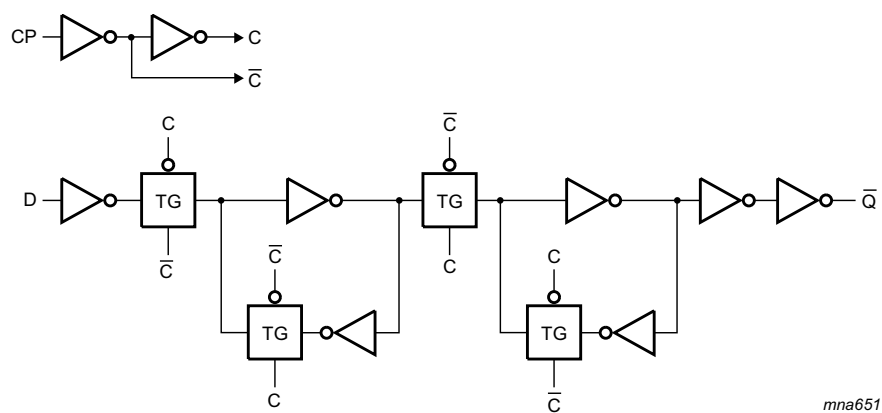


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

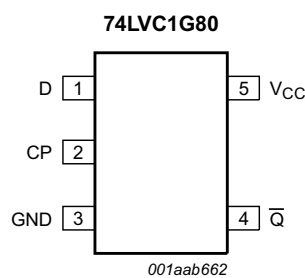


Fig 4. Pin configuration SOT353-1 and SOT753

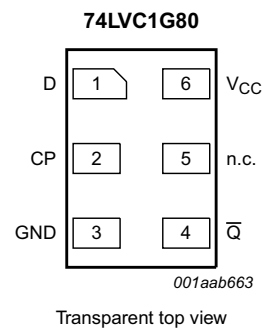


Fig 5. Pin configuration SOT886

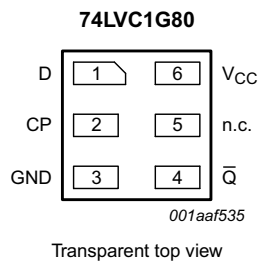


Fig 6. Pin configuration SOT891, SOT1115 and SOT1202

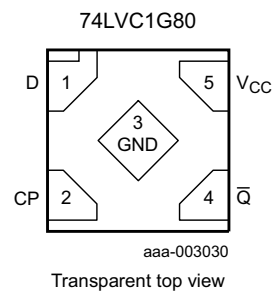


Fig 7. Pin configuration SOT1226 (X2SON5)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
D	1	1	data input
CP	2	2	clock pulse input
GND	3	3	ground (0 V)
$\overline{Q}$	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
CP	D	$\overline{Q}$
↑	L	H
↑	H	L
L	X	$\overline{q}$

- [1] H = HIGH voltage level;
L = LOW voltage level.
↑ = LOW-to-HIGH CP transition;
X = don't care;
 $\overline{q}$ = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	Active mode [1][2]	-0.5	$V_{CC} + 0.5$	V
		Power-down mode [1][2]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	-	250	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 and X2SON5 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = –100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} – 0.1	-	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	2.3	-	-	V
		I _O = –32 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	4	µA
ΔI _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} – 0.6 V; I _O = 0 A	-	5	500	µA
C _I	input capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC}	-	5	-	pF
T_{amb} = –40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V

Table 7. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	-	4	µA
ΔI _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	-	500	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	CP to $\overline{Q}$; see Figure 8 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.4	9.9	1.0	13.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.3	7.0	0.5	9.0	ns
		V _{CC} = 2.7 V	0.5	2.5	6.0	0.5	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	2.4	5.0	0.9	6.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.8	4.5	0.5	6.0	ns
t _{su}	set-up time	HIGH or LOW; D to CP; see Figure 9 ^[3]						
		V _{CC} = 1.65 V to 1.95 V	2.3	0.8	-	2.3	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	0.6	-	1.5	-	ns
		V _{CC} = 2.7 V	1.5	0.5	-	1.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	0.4	-	1.3	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.1	0.5	-	1.1	-	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _h	hold time	D to CP; see Figure 9						
		V _{CC} = 1.65 V to 1.95 V	0	–0.6	-	0	-	ns
		V _{CC} = 2.3 V to 2.7 V	0	–0.4	-	0	-	ns
		V _{CC} = 2.7 V	+0.5	–0.2	-	0.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	0.2	-	0.9	-	ns
		V _{CC} = 4.5 V to 5.5 V	+0.5	–0.1	-	0.5	-	ns
t _w	pulse width	CP HIGH or LOW; see Figure 9						
		V _{CC} = 1.65 V to 1.95 V	3.0	1.1	-	3.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.5	0.7	-	2.5	-	ns
		V _{CC} = 2.7 V	2.5	0.6	-	2.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	0.6	-	2.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.0	0.5	-	2.0	-	ns
f _{max}	maximum frequency	CP; see Figure 9						
		V _{CC} = 1.65 V to 1.95 V	160	300	-	160	-	MHz
		V _{CC} = 2.3 V to 2.7 V	160	350	-	160	-	MHz
		V _{CC} = 2.7 V	160	350	-	160	-	MHz
		V _{CC} = 3.0 V to 3.6 V	160	350	-	160	-	MHz
		V _{CC} = 4.5 V to 5.5 V	200	400	-	200	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[4]	-	17	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{su} is the same as t_{su(H)} and t_{su(L)}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms

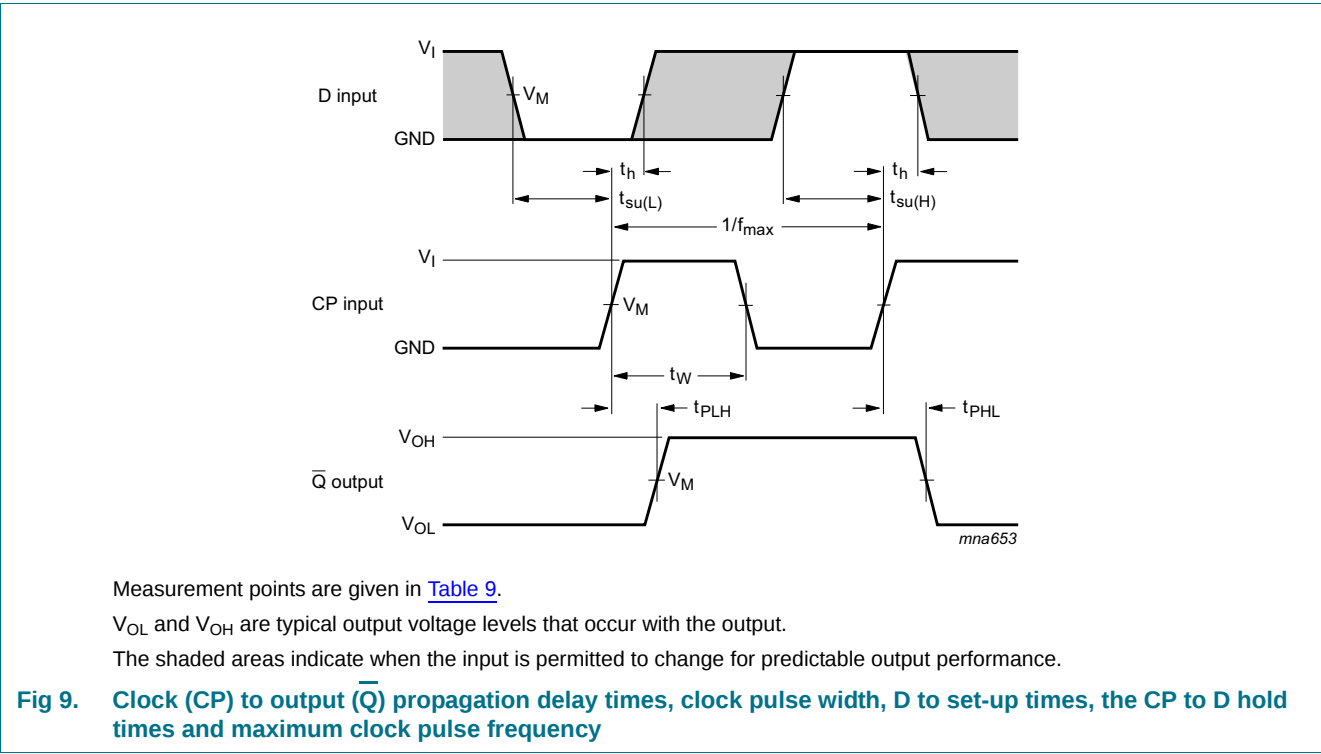
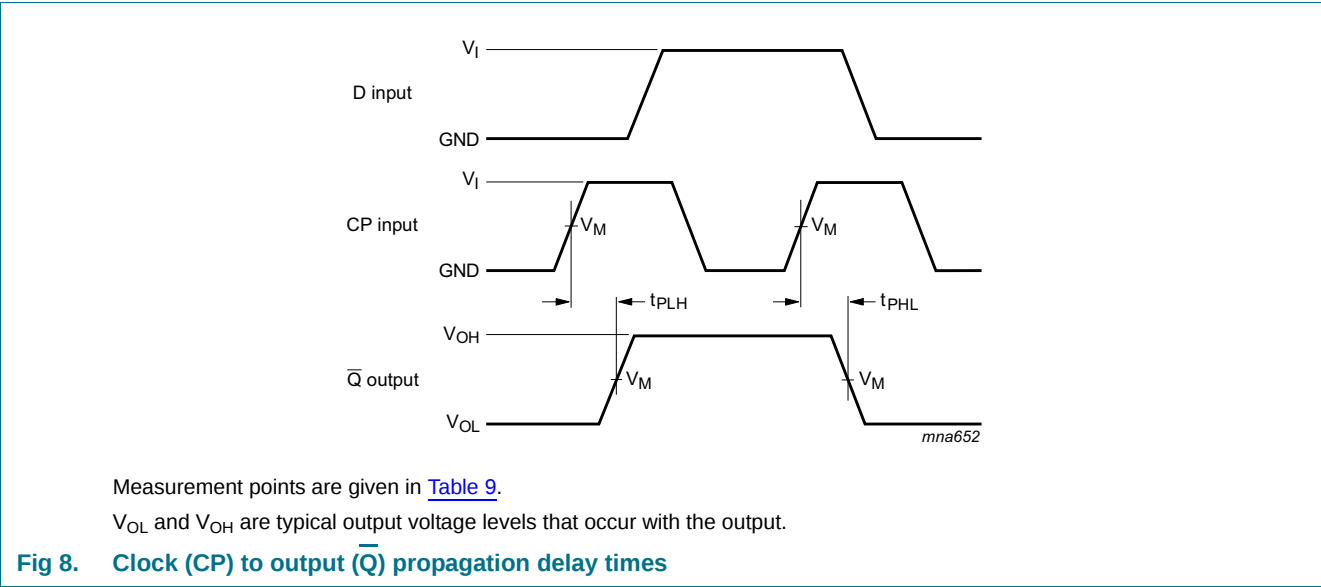
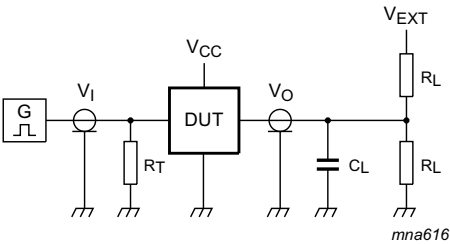


Table 9. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}



Test data is given in [Table 10](#).
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

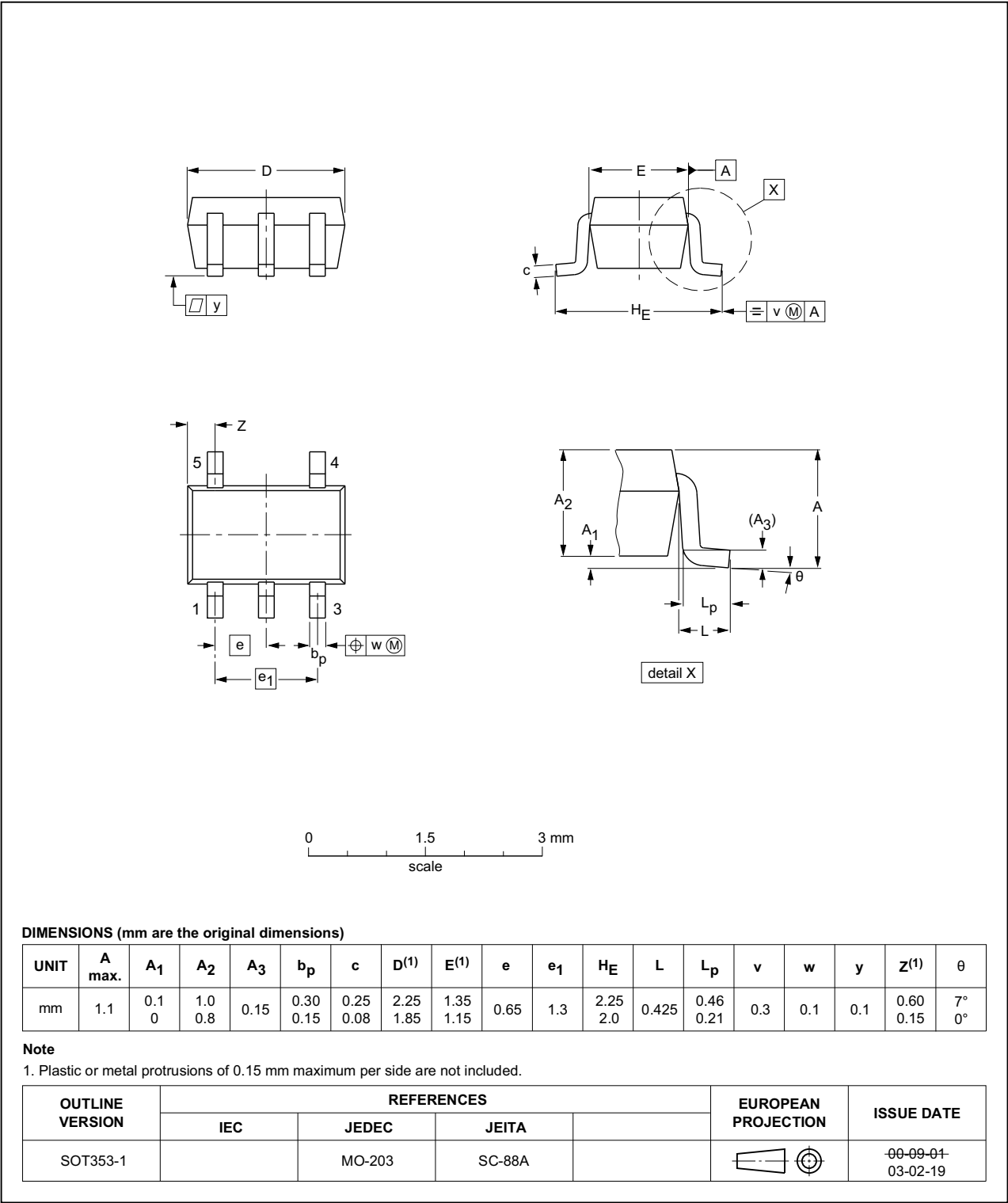


Fig 11. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

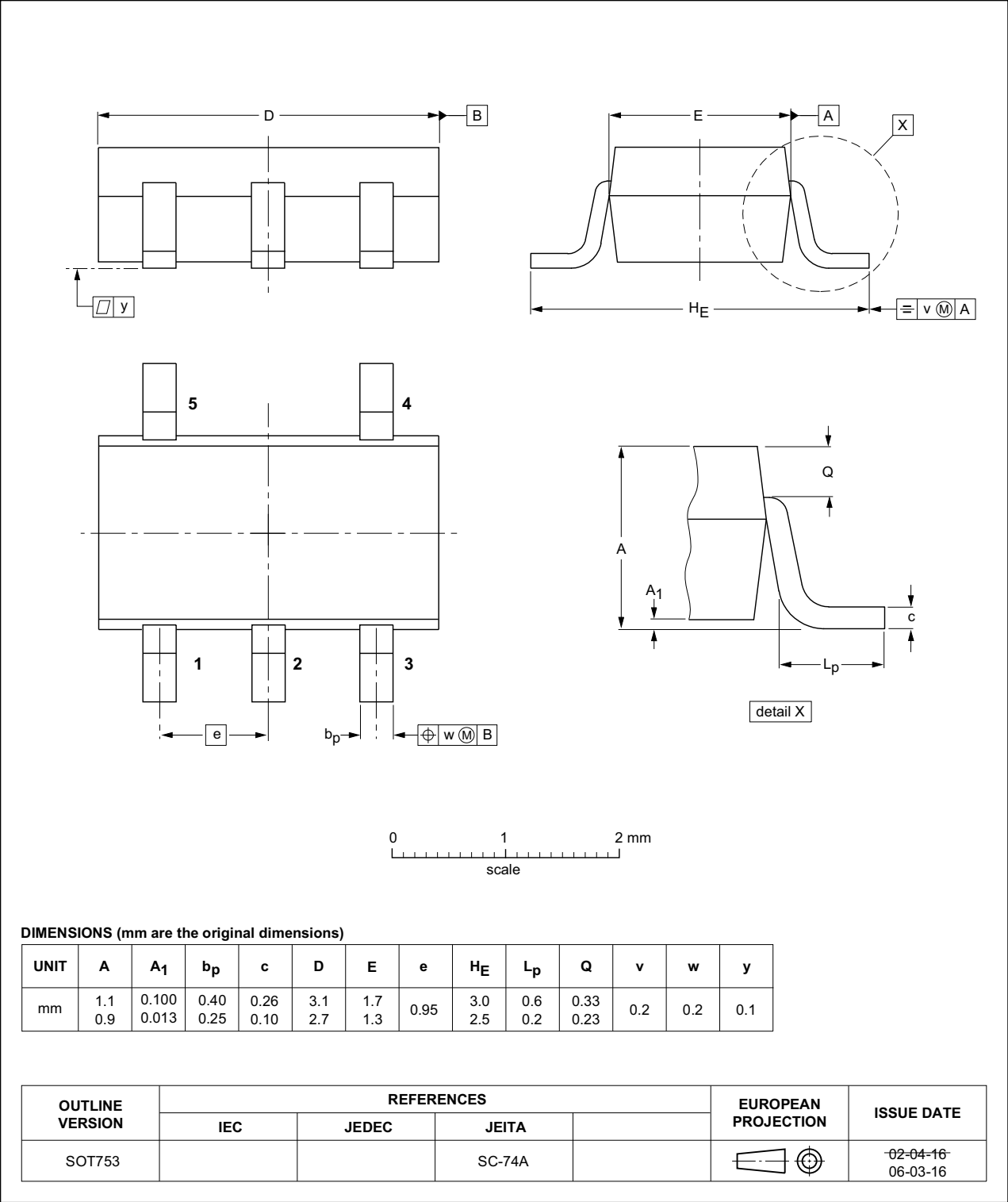


Fig 12. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

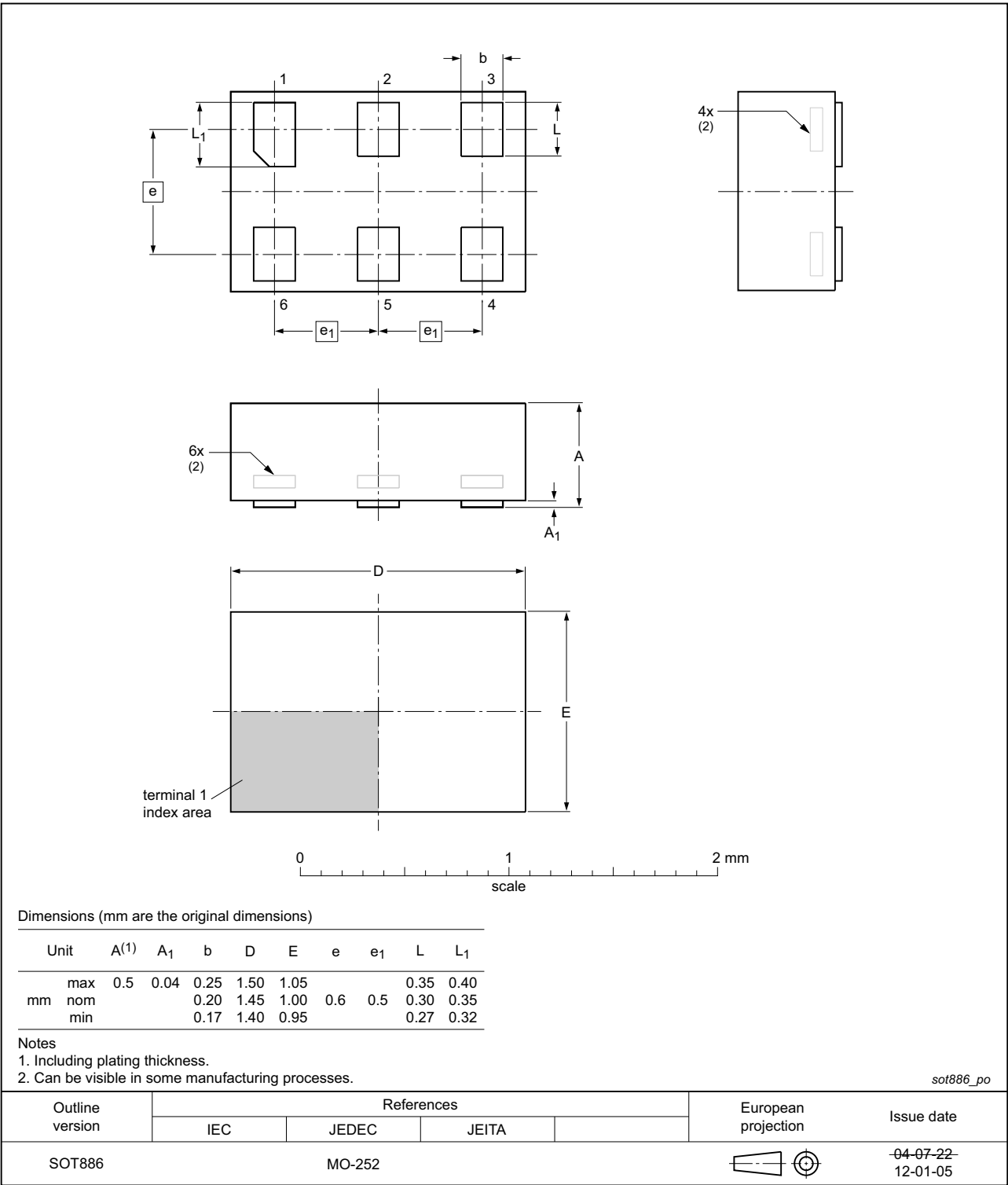


Fig 13. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

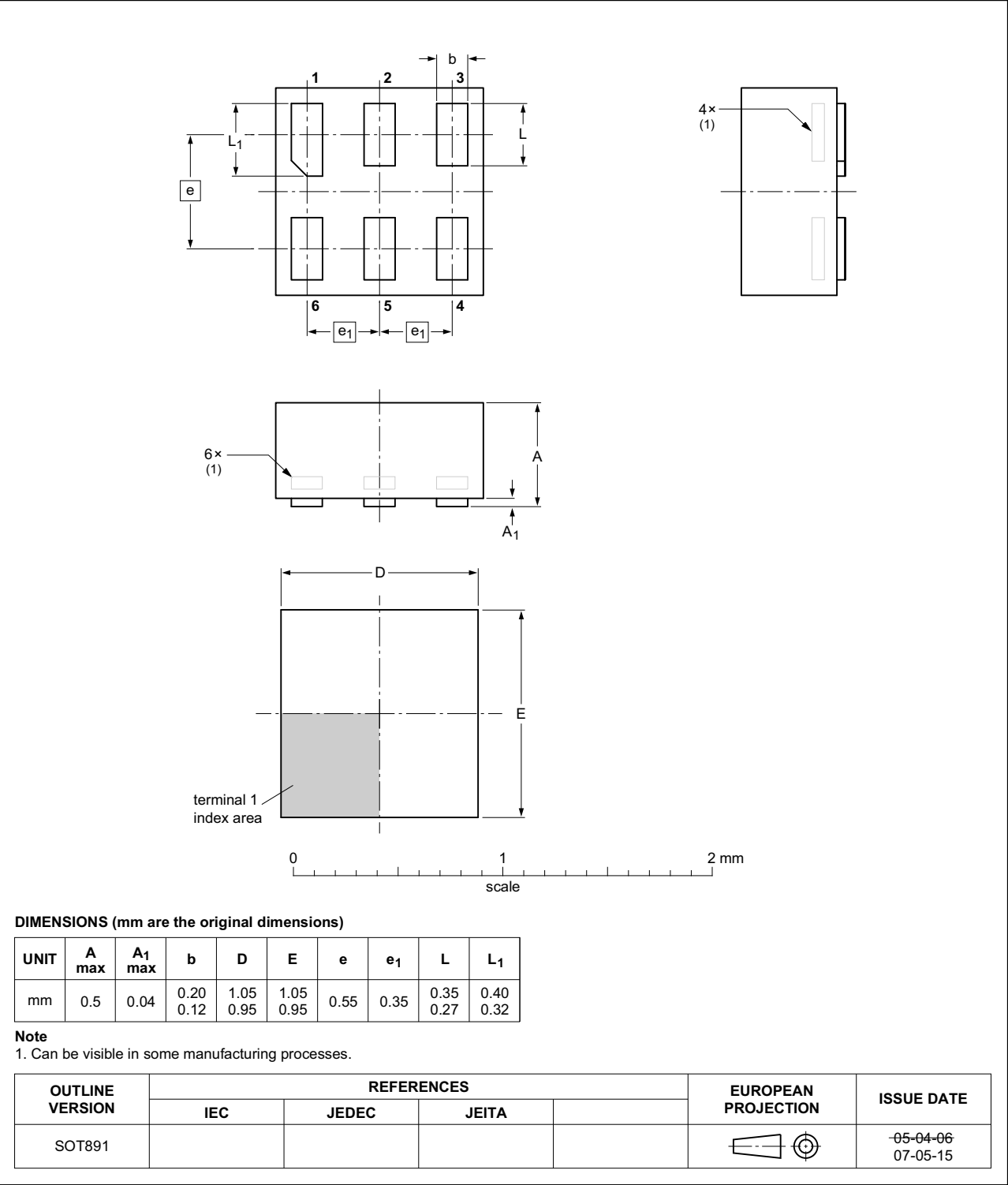


Fig 14. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

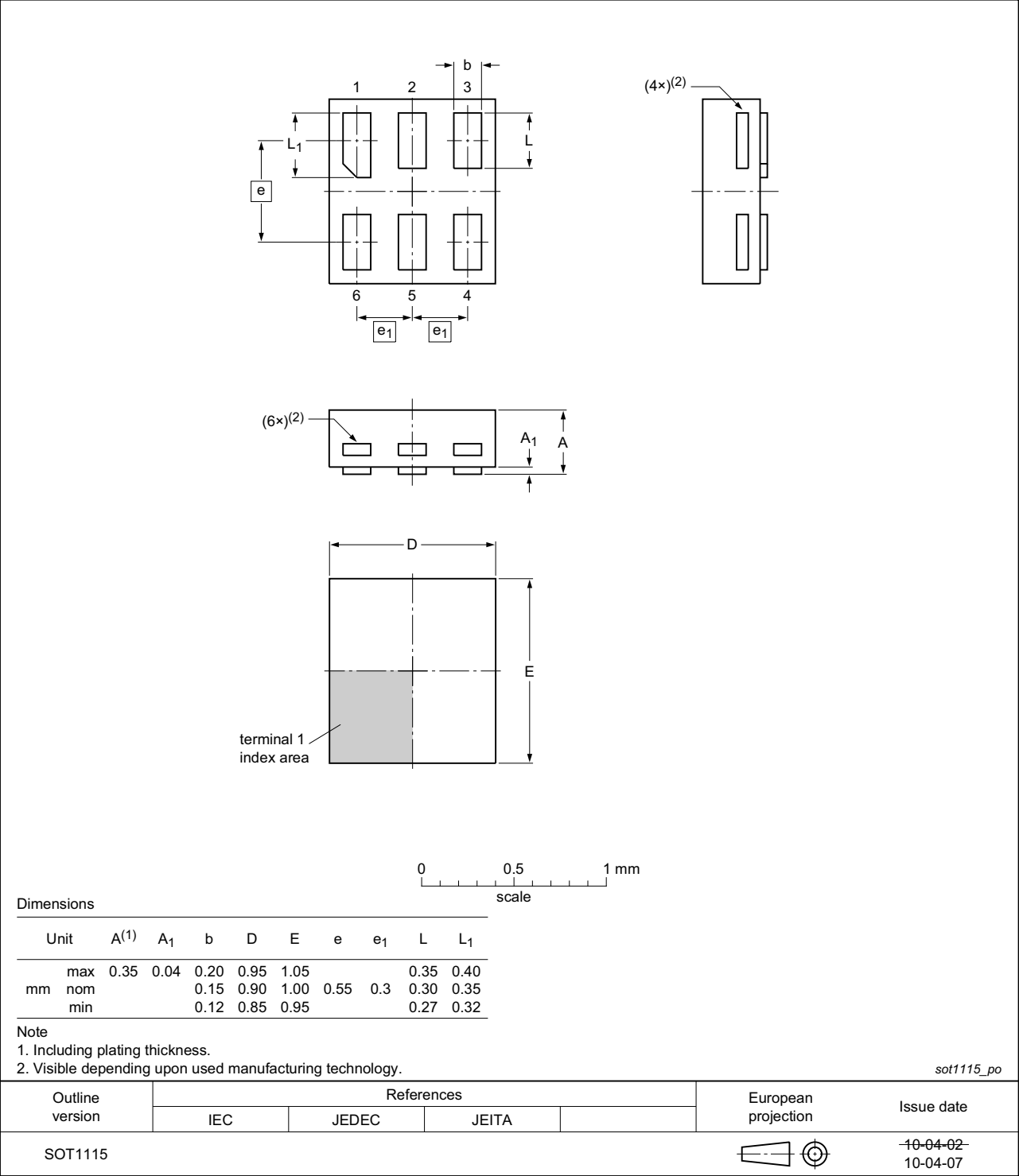


Fig 15. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202

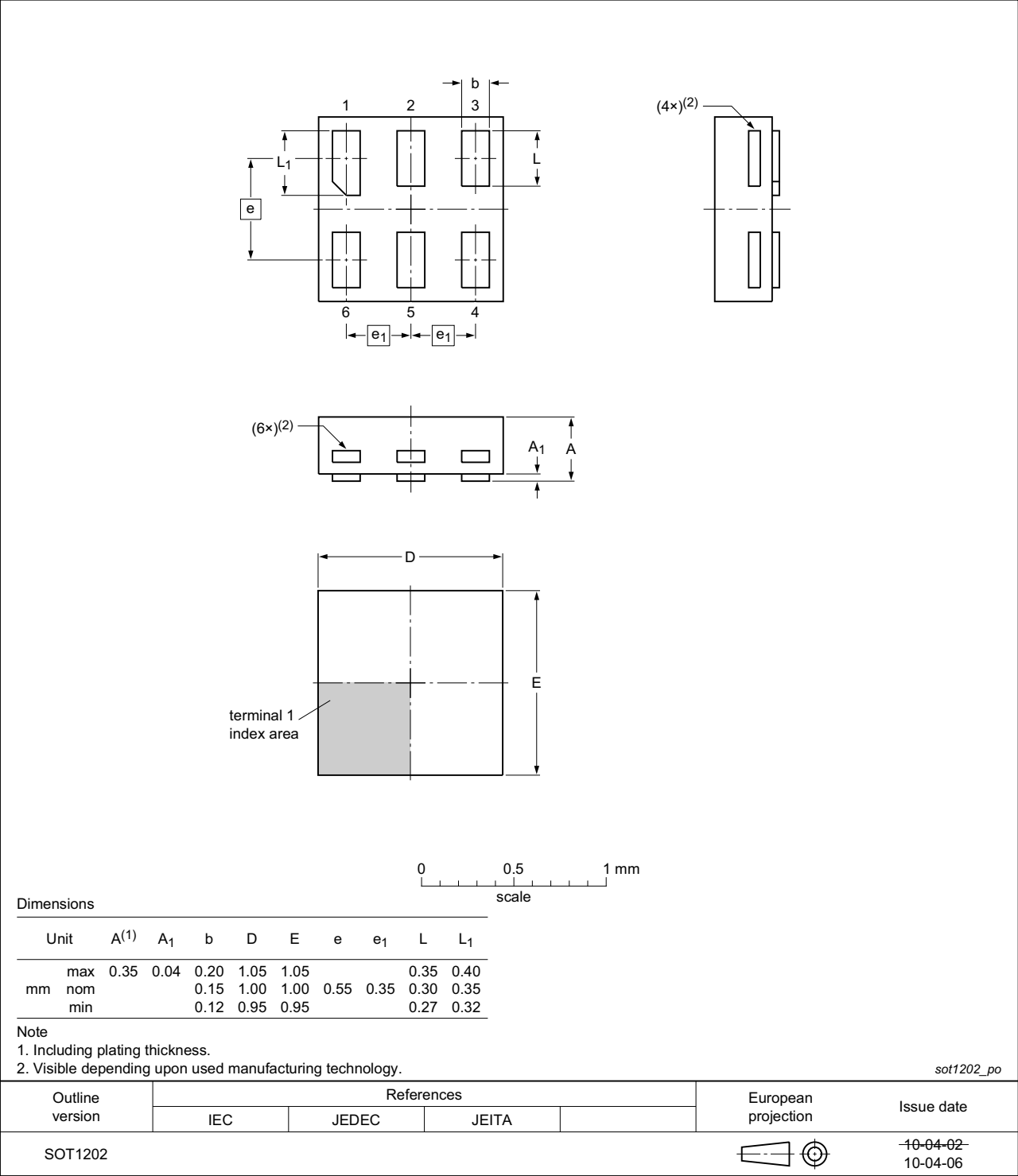


Fig 16. Package outline SOT1202 (XSON6)

**X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;
5 terminals; body 0.8 x 0.8 x 0.35 mm**

SOT1226

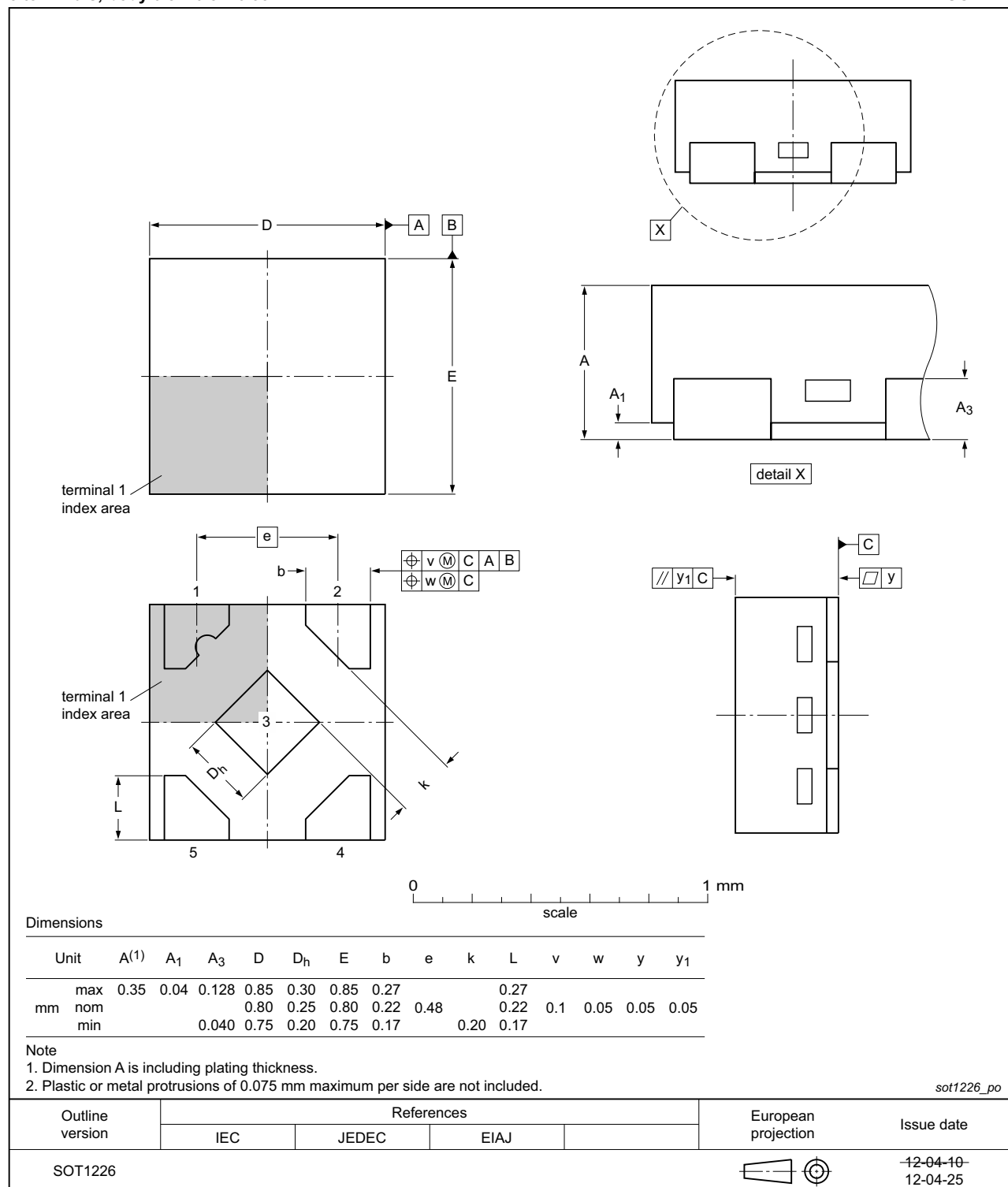


Fig 17. Package outline SOT1226 (X2SON5)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G80 v.13	20161205	Product data sheet	-	74LVC1G80 v.12
Modifications:	Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G80 v.12	20120702	Product data sheet	-	74LVC1G80 v.11
Modifications:	Added type number 74LVC1G80GX (SOT1226)			
74LVC1G80 v.11	20120402	Product data sheet	-	74LVC1G80 v.10
Modifications:	Errata in table 3 corrected (description CP input).			
74LVC1G80 v.10	20111202	Product data sheet	-	74LVC1G80 v.9
Modifications:	Legal pages updated.			
74LVC1G80 v.9	20100928	Product data sheet	-	74LVC1G80 v.8
Modifications:	- Added type number 74LVC1G80GN (SOT1115/XSON6 package). - Added type number 74LVC1G80GS (SOT1202/XSON6 package).			
74LVC1G80 v.8	20070829	Product data sheet	-	74LVC1G80 v.7
74LVC1G80 v.7	20061012	Product data sheet	-	74LVC1G80 v.6
74LVC1G80 v.6	20040910	Product specification	-	74LVC1G80 v.5
74LVC1G80 v.5	20040629	Product specification	-	74LVC1G80 v.4
74LVC1G80 v.4	20040429	Product specification	-	74LVC1G80 v.3
74LVC1G80 v.3	20030526	Product specification	-	74LVC1G80 v.2
74LVC1G80 v.2	20030130	Product specification	-	74LVC1G80 v.1
74LVC1G80 v.1	20010404	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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17. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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