SCOPE: IMPROVED, QUAD, SPST, CMOS ANALOG MULTIPLEXER

Device Type	Generic Number
01	DG441A(x)/883B
02	DG442A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
Z	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V^-

V^+ to V^- 44V
V^- to GND 25V
V_L ..... (GND-0.3V) to V+ +0.3V)
Digital Inputs, V_S, V_D 1/ .....(V^-) -2V to (V^+)+2V
or 30mA whichever occurs first
Continuous Current, Any terminal 30mA
Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
20 lead LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 20 lead LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{AL} (max) 0.8V
V_{AH} (min) 2.4V

NOTE 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLY

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S=-10mA, V_D=±8.5V, V^+=13.5V, V^-=-13.5V	1 2,3	All		85 100	Ω
On-Resistance Match Between Channels 4/	Δr_{DS} (ON)	I_S=-10mA, V_D=±10V, V^+=15V, V^-=-15V	1 2,3	All		4 5	Ω
On-Resistance Flatness 4/	r_{FLAT} (ON)	I_S=-10mA, V_D=5V or -5V, V^+=15V, V^-=-15V	1 2,3	All		9 15	Ω
Source- OFF Leakage Current	$I_{S(OFF)}$	V^+=16.5V, V^-=-16.5V, V_{IN}=2.4V V_S=±15.5V V_D=±15.5V	1 2,3	All	-0.5 -20	0.5 20	nA
Drain- OFF Leakage Current	$I_{D(OFF)}$	V^+=16.5V, V^-=-16.5V, V_S=±15.5V V_D=±15.5V	1 2,3	All	-0.5 -20	0.5 20	nA
Channel-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V^+=16.5V, V^-=-16.5V, V_S=±15.5V V_D=±15.5V	1 2,3	01	-0.5 -20	0.5 20	nA
INPUT							
Input Current/Voltage High	I_{INH}	V_{IN}=2.4V	1,2,3	All	-500	500	nA
Input Current/Voltage Low	I_{INL}	V_{IN}= 0.8V	1,2,3	All	-500	500	nA
SUPPLY							
Power Supply Range			1,2,3	All	±4.5	±20	V
Positive Supply Current	I+	All channels on or off, V^+=16.5V, V^-=-16.5V, V_{IN}=0 or 5V	1,2,3	All		100	µA
Negative Supply Current	I-	All channels on or off, V^+=16.5V, V^-=-16.5V, V_{IN}=0 or 5V	1 2,3	All	-1 -5	1 5	µA
Ground Current	IGND	All channels on or off, V^+=16.5V, V^-=-16.5V, V_{IN}=0 or 5V	1,2,3	All	-100		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S=±10V, R_L=1kΩ, Figure 2	9	All		250	ns
Turn-Off Time	t_{OFF}	V_D=±10V, R_L=1kΩ, Figure 2	9	01 02		120 170	ns
Charge Injection NOTE 2	Q	C_L=1nF, V_{GEN}=0V, R_{GEN}=0Ω, Figure 3	9	All		10	pC

TABLE 1. ELECTRICAL TESTS: SINGLE SUPPLY

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+12V, V^-=0V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S=1.0mA, V_D=3V or 8V, V^+=10.8V	1,3 2	All		160 200	Ω
SUPPLY							
Power Supply Range			1,2,3	All	10	30	V
Positive Supply Current	I+	All channels on or off, V_{IN}=0 or 5V	1,2,3	All		100	µA
Negative Supply Current	I-	All channels on or off, V_{IN}=0 or 5V	1 2,3	All	-1 -5	1 5	µA
Ground Current	IGND	All channels on or off, V_{IN}=0 or 5V	1,2,3	All	-100		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S=8V, Figure 2	9	All		400	ns
Turn-Off Time	t_{OFF}	V_S=8V, Figure 2	9	All		200	ns
Charge Injection	Q	C_L=1nF, V_{GEN}=0V NOTE 3	9	All		10	pC

NOTE 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

NOTE 3: Guaranteed by design.

NOTE 4: On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

TRUTH TABLE **TERMINAL CONNECTION**

LOGIC	DG441A SWITCH		TERMINAL NUMBER	01 DG441A	01 DG441A	02 DG442A	02 DG442A
0	ON			J16	20LCC	J16	20LCC
1	OFF		1	IN1	NC	IN1	NC
			2	D1	IN1	D1	IN1
			3	S1	D1	S1	D1
LOGIC	**DG442A**		4	V-	S1	V-	S1
	SWITCH		5	GND	V-	GND	V-
0	OFF		6	S4	NC	S4	NC
1	ON		7	D4	GND	D4	GND
			8	IN4	S4	IN4	S4
			9	IN3	D4	IN3	D4
			10	D3	IN4	D3	IN4
			11	S3	NC	S3	NC
			12	NC	IN3	NC	IN3
			13	V+	D3	V+	D3
			14	S2	S3	S2	S3
			15	D2	NC	D2	NC
			16	IN2	NC	IN2	NC
			17		V+		V+
			18		S2		S2
			19		D2		D2
			20		IN2		IN2

Figure 2. Switching Time: See Commercial Data Sheet.
Figure 3. Charge Injection: See Commercial Data Sheet.

ORDERING INFORMATION:	
DG441AK/883B 16 CDIP	DG442AK/883B 16 CDIP
DG441AZ/883B 20 LCC	DG442AZ/883B 20 LCC

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:
1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:
1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.