

Computer On Module

- Processor Freescale i.MX 6Quad, 1GHz
- RAM 1GB DDR3 SDRAM 64-bit
- ROM 128MB NAND Flash or 8GB eMMC
- Power supply Single 3.1V to 5.5V
- Size 31mm SO-DIMM
- Temperature Grade Extended Consumer (-20°C to 105°C Tj)

Key Features

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- Full HD LCD controller, 24bpp
- OpenGL ES 2.0 and OpenVG 1.1 hardware accelerators
- Multi-format HD 1080p60 video decoder and 1080p30 encoder hardware engine
- Two Camera Interfaces
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - dual, single-precision floating point execute pipeline
- Unified 1MB L2 cache
- Several interfaces:
 - 3x UART, 2x SDIO, 2x SSI/AC97/I2S, I2C, CSPI, Keypad, Ext. Memory I/F
- 3.3V I/O
- IEEE1588 support
- 2x Controller Area Network (FlexCAN)
- PCIe 2.0 (1-lane)

LVDS Option only:

- Dual LVDS display port
- SATA

OS Support

- Windows Embedded Compact 7
- Linux
- Android by kernel concepts www.kernelconcepts.de
- QNX by SITRE www.sitre.fr

Development System

- Starter-Kit V



**Quad
Cortex A9**

Board highlights:

- Highly integrated
- Standard TX-DIMM pinout
- as small as possible - only 31mm
- 3.3V I/O

The TX6 is a member of the TX module series, specially designed for Freescale i.MX multimedia processors. TX modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TX modules includes a Freescale® i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX6 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

Computer on module

- Freescale® i.MX 6Quad up to 1 GHz
- 1GByte SDRAM (64bit) DDR3-1066
- 128 MByte NAND Flash memory or 8GB eMMC
- DIMM200-module (67,6mm x 31 mm x 4mm)
- Operating temperature ranges (Processor junction temperature)
 - Extended Consumer Grade: -20°C ..105°C
 - Industrial Grade: -40°C ..105°C
 - Automotive Grade: -40°C ..125°C, AEC-Q100 Grade 3

Processor

The i.MX 6Dual and i.MX 6Quad processors represent Freescale Semiconductor's latest achievement in integrated multimedia applications processors. These processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption. The i.MX 6Dual and i.MX 6Quad processors feature Freescale's advanced implementation of the quad ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3/LPDDR2-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

High Performance CPU : ARM Quad Cortex-A9

- ARM Cortex-A9, with ARMv7™, Neon, VFPv3 and Trustzone support
- 32K instruction and data L1 caches and 256 KB to 1 MB of L2 cache
- Multi-stream-capable HD video engine delivering 1080p60 decode, 1080p30 encode and 3D video playback in HD in high performance families
- Superior 3D graphics performance with up to quad shaders performing 200 MT/s
- Separate 2D and/or Vertex acceleration engines for an optimal user interface experience
- Stereoscopic image sensor support for 3D imaging

Standard TX-DIMM pinout:

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

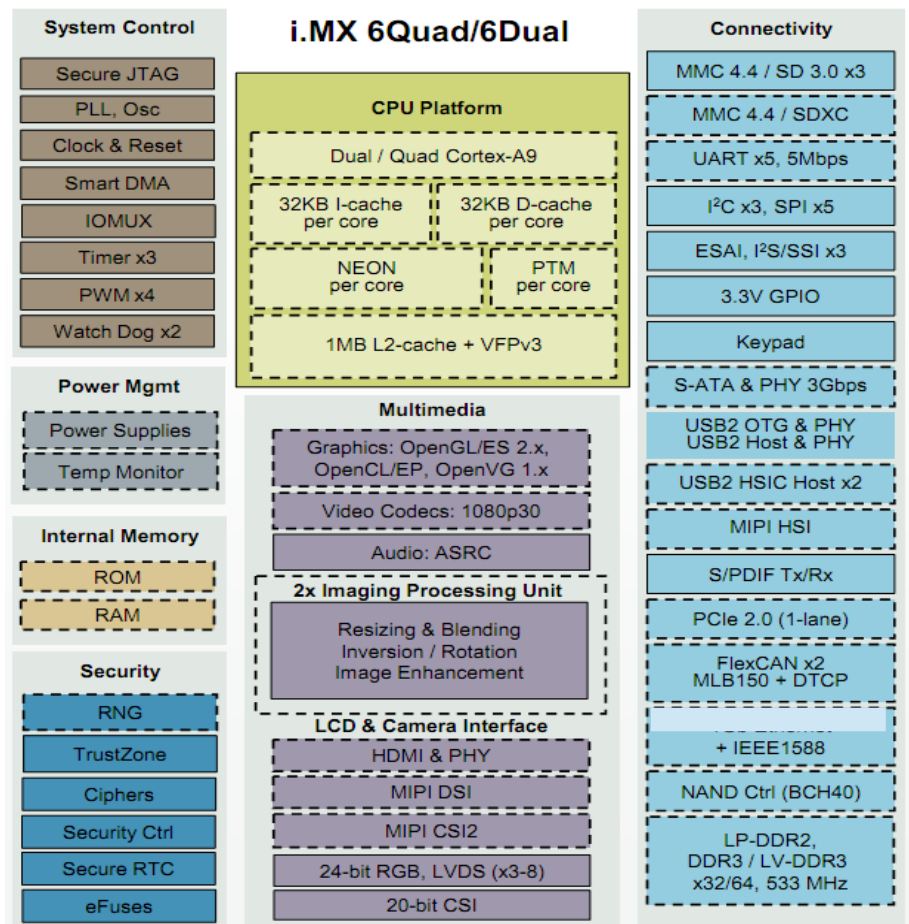
Power Supply

The TX6 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (up to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide

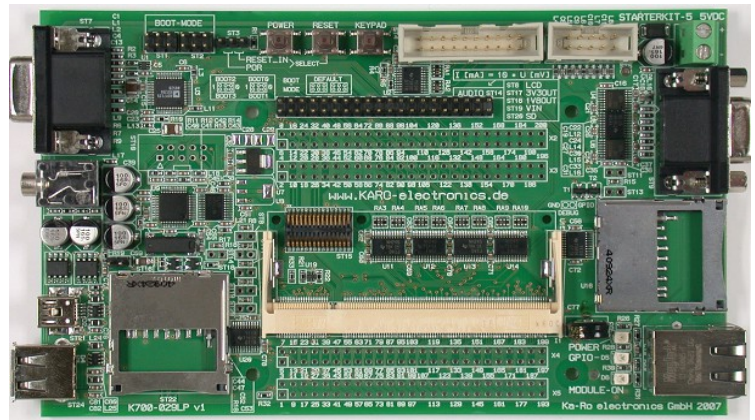


Order Number	CPU	SDRAM	Flash	Temp. Grade
TX6Q/1000/1024S/128F	1GHz MCIMX6Q5 Quad Core Consumer	1GB	128MB	Extended Consumer
TX6Q/1000/1024S/8GF	1GHz MCIMX6Q5 Quad Core Consumer	1GB	8GB	Extended Consumer
TX6Q/1000/1024S/128F/LVDS	1GHz MCIMX6Q5 Quad Core Consumer	1GB	128MB	Extended Consumer

STARTER-KIT V

The Starter-Kit V is a ready-to-use development system for building applications based on the TX embedded processor boards.

- DIMM200 TX socket
- Two SD-card sockets
- USB 2.0 OTG and USB 2.0 Host connector
- D-SUB 15 VGA connector
- 40pin LCD flat cable header
- 3.5mm headphone connector
- JTAG interface
- SGTL5000 audio codec
- TSC2007 touchscreen controller
- RS232 on 10pin flat cable and SUB-D header
- All pins of the TX socket are connected to daughter board slot for easy application design-in
- 10/100 Mbit/s Ethernet
- 5VDC Power Supply by USB-OTG or power jack.
- 100mm x 160mm
- Schematics of the base board are included for reference.



DISPLAY OPTIONS

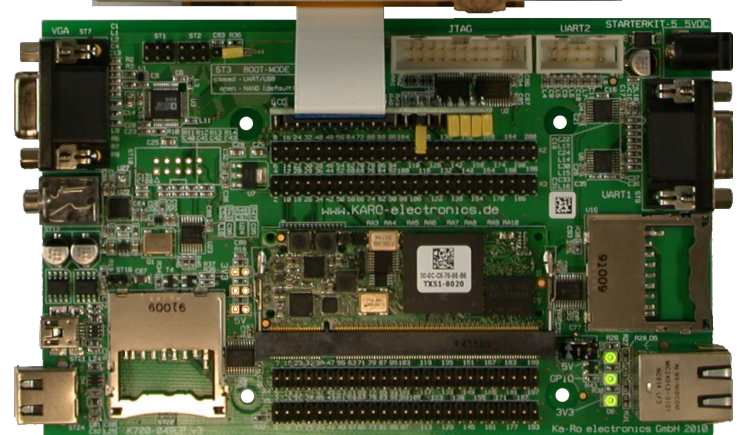
The optional display comes with an FFC cable and a small adapter PCB which can be plugged directly onto the Starter-Kit 40pin LCD header.

TX00-DV01: 5,7" VGA Resistive Touch

- 5,7 inch TFT display
- 640 x 480 dots
- White LED backlight
- Resistive Touchscreen

TX00-DV04: 5,7" VGA PolyTouch™

- 5,7 inch TFT display
- 640 x 480 dots
- White LED backlight
- Capacitive Touchscreen



PINOUT

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
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POWER SUPPLY & RESET

1-4	power	VIN				Module power supply input (3.3V-5V, observe DIMM socket contact current rating)
5-7, 9-12	power	VOUT				3.3V power supply output (up to 1A under observance of the max. rated VIN current)
8	3V3	BOOTMODE				Boot mode select H: Boot from NAND / L: Boot from UART/USB
13	power	VBACKUP				DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
14	VIN	PMIC_PWR_BTN				External Power-On control, connected to LTC3676 ON Refer to LTC3676 datasheet for details. Leave unconnected if not used. LTC3676 IRQ is connected to i.MX6 pad EIM_A25
15	3V3	#RESET_OUT	GPIO_17	ESAI1_TX0 ENET_1588_EVENT3_IN CCM_PMIC_RDY SDMA_EXT_EVENT[0] SPDIF_OUT1 SJC_JTAG_ACT	GPIO7[12]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controller by a GPIO function during runtime.
16		#POR	POR_B			Power On Reset — Active low input signal Leave unconnected, if not used.
17		#RESET_IN	POR_B			Wire ored to pin 16
18	GND	GND				

Ethernet

19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				

USB-HOST

27	3V3	USBH_VBUSEN	EIM_D31	WEIM_D[31] IPU1_DISP1_DAT[20] IPU1_DIO_PIN12 IPU1_CSI0_D[2] UART3_RTS USBOH3_USBH1_PWR MX6Q_PER_HPROT[1]	GPIO3[31]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	EIM_D30	WEIM_D[30] IPU1_DISP1_DAT[21] IPU1_DIO_PIN11 IPU1_CSI0_D[3] UART3_CTS USBOH3_USBH1_OC MX6Q_PER1_HPROT[0]	GPIO3[30] 10K-PU	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM	USB_H1_DN			D- pin of the USB cable
30	analog	USBH_VBUS	USB_H1_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP	USB_H1_DP			D+ pin of the USB cable
32	GND	GND				

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
USB-OTG / 2nd CAN						
33	3V3	USBOTG_ID	EIM_D23	WEIM_D[23] DIO_D0_CS UART3_CTS UART1_DCD IPU2_CSI1_DATA_EN IPU1_DI1_PIN2 IPU1_DI1_PIN14	GPIO3[23]	
34	3V3	USBOTG_VBUSEN CAN_TX	GPIO_7	ESAI1_TX4_RX1 ECSP15_RDY EPIT1_EPITO CAN1_TXCAN UART2_TXD_MUX SPDIF_PLOCK OTGUSB_HOST_MODE	GPIO1[7]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	USB_OTG_DN			D- pin of the USB cable
36	3V3	#USBOTG_OC CAN_RX	GPIO_8	ESAI1_TX5_RX0 EPIT2_EPITO CAN1_RXCAN UART2_RXD_MUX SPDIF_SRCLK USB_PWRCTL_WAKEUP	GPIO1[8] 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB_OTG_DP			D+ pin of the USB cable
38	analog	USBOTG_VBUS	USB_OTG_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND				
I2C						
40	3V3	I2C_DATA	GPIO_6	ESAI1_SCKT OBSRV_INT_OUT1 I2C3_SDA CCM_CCM_OUT_0 CSU_CSU_INT_DEB USDHC2_LCTL MLB_MLB SIG	GPIO1[6]	I2C Data
41	3V3	I2C_CLK	GPIO_3	ESAI1_HCKR OBSRV_INT_OUT0 I2C3_SCL CCM_CLK02 USBOH3_USBH1_OC MLB_MLBCLK	GPIO1[3]	I2C Clock
PWM						
42	3V3	PWM	GPIO_1	ESAI1_SCKR WDOG2_WDOG_B KPP_ROW[5] PWM2_PWM0 USDHC1_CD SRC_TESTER_ACK	GPIO1[1]	PWM Output
1-WIRE						
43	3V3	OWDAT	GPIO_18	ESAI1_TX1 ENET_RX_CLK USDHC3_VSELECT SDMA_EXT_EVENT[1] ASRC_ASRC_EXT_CLK SNVS_VIO_5_CTL SRC_SYSTEM_RST	GPIO7[13]	1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system.
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	EIM_EB2	WEIM_EB[2] ECSP11_SS0 CCM_DI1_EXT_CLK IPU2_CSI1_D[19] HDMI_TX_DDC_SCL I2C2_SCL SRC_BT_CFG[30]	GPIO2[30]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	EIM_D19	WEIM_D[19] ECSP11_SS1 IPU1_DIO_PIN8 IPU2_CSI1_D[16] UART1_CTS EPIT1_EPITO MX6Q_PER_HRESP	GPIO3[19]	Slave Select (Selectable polarity) signal

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
46	3V3	CSPI_MOSI	EIM_D18	WEIM_D[18] ECSPI1_MOSI IPU1_DIO_PIN7 IPU2_CSI1_D[17] IPU1_DI1_D0_CS I2C3_SDA MX6Q_PER_HBURST[2]	GPIO3[18]	Master Out/Slave In signal
47	3V3	CSPI_MISO	EIM_D17	WEIM_D[17] ECSPI1_MISO IPU1_DIO_PIN6 IPU2_CSI1_PIXCLK DCIC1_DCIC_OUT I2C3_SCL MX6Q_PER_HBURST[1]	GPIO3[17]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	EIM_D16	WEIM_D[16] ECSPI1_SCLK IPU1_DIO_PIN5 IPU2_CSI1_D[18] HDMI_TX_DDC_SDA I2C2_SDA	GPIO3[16]	Serial Clock signal
49	3V3	CSPI_RDY	GPIO_19	KPP_COL[5] ENET_1588_EVENT0 SPDIF_OUT1 CCM_CLKO ECSPI1_RDY ENET_TX_ER SRC_INT_BOOT	GPIO4[5]	Serial Data Ready signal
50	GND	GND				

SD – Secure Digital Interface 1

51	3V3	SD1_CD	SD3_CMD	USDHC3_CMD UART2_CTS CAN1_TXCAN USBOH3_UH3_ DFD_OUT[4] USBOH3_UH2_ DFD_OUT[4] MIPI_CORE_DPHY_ TEST_IN[16]	GPIO7[2]	SD Card Detect – connected to a GPIO
52	3V3	SD1_D[0]	SD1_DAT0	USDHC1_DAT0 ECSPI5_MISO CAAM_WRAPPER_ RNG_OSC_OBS GPT_CAPIN1 PCIE_CTRL_DIAG_ STATUS_BUS_MUX[8] HDMI_TX_OPHYDTB[1]	GPIO1[16]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	SD1_DAT1	USDHC1_DAT1 ECSPI5_SS0 PWM3_PWM0 GPT_CAPIN2 PCIE_CTRL_DIAG_ STATUS_BUS_MUX[7] HDMI_TX_OPHYDTB[0]	GPIO1[17]	
54	3V3	SD1_D[2]	SD1_DAT2	USDHC1_DAT2 ECSPI5_SS1 GPT_CMPOUT2 PWM2_PWM0 WDOG1_WDOG_B WDOG1_WDOG_ RST_B_DEB	GPIO1[19]	
55	3V3	SD1_D[3]	SD1_DAT3	USDHC1_DAT3 ECSPI5_SS2 GPT_CMPOUT3 PWM1_PWM0 WDOG2_WDOG_B WDOG2_WDOG_ RST_B_DEB	GPIO1[21]	
56	3V3	SD1_CMD	SD1_CMD	USDHC1_CMD ECSPI5_MOSI PWM4_PWM0 GPT_CMPOUT1	GPIO1[18]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD1_CLK	USDHC1_CLK ECSPI5_SCLK OSC32K_32K_OUT GPT_CLKIN PHY_DTB[0] SATA_PHY_DTB[0]	GPIO1[20]	SD Output Clock.
58	GND	GND				

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
1st UART						
59	3V3	TXD	SD3_DAT7	USDHC3_DAT7 UART1_TXD_MUX PCIE_CTRL_DIAG_ STATUS_BUS_MUX[24] USBOH3_UH3_ DFD_OUT[0] USBOH3_UH2_ DFD_OUT[0] MIPI_CORE_ DPHY_TEST_IN[12]	GPIO6[17]	Application UART 1 Transmit Data output signal
60	3V3	RXD	SD3_DAT6	USDHC3_DAT6 UART1_RXD_MUX PCIE_CTRL_DIAG_ STATUS_BUS_MUX[25] USBOH3_UH3_ DFD_OUT[1] USBOH3_UH2_ DFD_OUT[1] MIPI_CORE_ DPHY_TEST_IN[13]	GPIO6[18]	Application UART 1 Receive Data input signal
61	3V3	RTS	SD3_DAT1	USDHC3_DAT1 UART1_RTS CAN2_RXCAN USBOH3_UH3_ DFD_OUT[7] USBOH3_UH2_ DFD_OUT[7] MIPI_CORE_ DPHY_TEST_IN[19]	GPIO7[5]	Application UART 1 Request to Send input signal
62	3V3	CTS	SD3_DAT0	USDHC3_DAT0 UART1_CTS CAN2_TXCAN USBOH3_UH3_ DFD_OUT[6] USBOH3_UH2_ DFD_OUT[6] MIPI_CORE_ DPHY_TEST_IN[18]	GPIO7[4]	Application UART 1 Clear to Send output signal
2nd UART						
63	3V3	TXD	SD4_DAT7	RAWNAND_D15 USDHC4_DAT7 UART2_TXD_MUX USBOH3_UH2_ DFD_OUT[31] USBOH3_UH3_ DFD_OUT[31] IPU1_IPU_DIAG_BUS[15] IPU2_IPU_DIAG_BUS[15]	GPIO2[15]	Application UART 2 Transmit Data output signal
64	3V3	RXD	SD4_DAT4	RAWNAND_D12 USDHC4_DAT4 UART2_RXD_MUX USBOH3_UH2_ DFD_OUT[28] USBOH3_UH3_ DFD_OUT[28] IPU1_IPU_DIAG_BUS[12] IPU2_IPU_DIAG_BUS[12]	GPIO2[12]	Application UART 2 Receive Data input signal
65	3V3	RTS	SD4_DAT5	RAWNAND_D13 USDHC4_DAT5 UART2_RTS USBOH3_UH2_ DFD_OUT[29] USBOH3_UH3_ DFD_OUT[29] IPU1_IPU_DIAG_BUS[13] IPU2_IPU_DIAG_BUS[13]	GPIO2[13]	Application UART 2 Request to Send input signal
66	3V3	CTS	SD4_DAT6	RAWNAND_D14 USDHC4_DAT6 UART2_CTS USBOH3_UH2_ DFD_OUT[30] USBOH3_UH3_ DFD_OUT[30] IPU1_IPU_DIAG_BUS[14] IPU2_IPU_DIAG_BUS[14]	GPIO2[14]	Application UART 2 Clear to Send output signal

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
3rd UART						
67	3V3	TXD	EIM_D24	WEIM_D[24] ECSP14_SS2 UART3_TXD_MUX ECSP11_SS2 ECSP12_SS2 AUDMUX_AUD5_RXFS UART1_DTR	GPIO3[24]	Application UART 3 Transmit Data output signal
68	3V3	RXD	EIM_D25	WEIM_D[25] ECSP14_SS3 UART3_RXD_MUX ECSP11_SS3 ECSP12_SS3 AUDMUX_AUD5_RXC UART1_DSR	GPIO3[25]	Application UART 3 Receive Data input signal
69	3V3	RTS	SD3_RST	USDHC3_RST UART3_RTS PCIE_CTRL_DIAG_ STATUS_BUS_MUX[30] USBOH3_UH3_ DFD_OUT[10] USBOH3_UH2_ DFD_OUT[10] MIPI_CORE_ DPHY_TEST_IN[22]	GPIO7[8]	Application UART 3 Request to Send input signal
70	3V3	CTS	SD3_DAT3	USDHC3_DAT3 UART3_CTS PCIE_CTRL_DIAG_ STATUS_BUS_MUX[29] USBOH3_UH3_ DFD_OUT[9] USBOH3_UH2_ DFD_OUT[9] MIPI_CORE_ DPHY_TEST_IN[21]	GPIO7[7]	Application UART 3 Clear to Send output signal
71	GND	GND				
KEYPAD / 1st CAN						
72	3V3	KP_COL[0]	GPIO_9	ESAI1_FSR WDOG1_WDOG_B KPP_COL[6] CCM_REF_EN_B PWM1_PWMO USDHC1_WP SRC_EARLY_RST	GPIO1[9]	
73	3V3	KP_COL[1]	GPIO_4	ESAI1_HCKT OBSRV_INT_OUT3 KPP_COL[7] CCM_CCM_OUT_2 CSU_ALARM_AUT[1] USDHC2_CD OCOTP_CTRL_WRAPPER _FUSE_LATCHED	GPIO1[4]	
74	3V3	KP_COL[2]	KEY_COL2	ECSP11_SS1 ENET_RDATA[2] CAN1_TXCAN KPP_COL[2] ENET_MDC USBOH3_H1USB_ PWRCTL_WAKEUP MX6Q_PER1_HADDR[3]	GPIO4[10]	
75	3V3	KP_COL[3]	KEY_COL3	ECSP11_SS3 ENET_CRS HDMI_TX_DDC_SCL KPP_COL[3] I2C2_SCL SPDIF_IN1 MX6Q_PER1_HADDR[5]	GPIO4[12]	
76	3V3	TXCAN	KEY_COL4	CAN2_TXCAN IPU1_SIGS[4] USBOH3_USBOTG_OC KPP_COL[4] UART5_RTS MMDC_DEBUG[49] MX6Q_PER1_HADDR[7]	GPIO4[14]	

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
77	3V3	KP_ROW[0]	GPIO_2	ESAI1_FST OBSRV_INT_OUT2 KPP_ROW[6] CCM_CCM_OUT_1 CSU_ALARM_AUT[0] USDHC2_WP MLB_MLBDAT	GPIO1[2]	
78	3V3	KP_ROW[1]	GPIO_5	ESAI1_TX2_RX3 OBSRV_INT_OUT4 KPP_ROW[7] CCM_CLKO CSU_ALARM_AUT[2] I2C3_SCL MPCORE_EVENTI	GPIO1[5]	
79	3V3	KP_ROW[2]	KEY_ROW2	ECSP11_SS2 ENET_TDATA[2] CAN1_RXCAN KPP_ROW[2] USDHC2_VSELECT HDMI_TX_CEC_LINE MX6Q_PER1_HADDR[4]	GPIO4[11]	
80	3V3	KP_ROW[3]	KEY_ROW3	OSC32K_32K_OUT ASRC_ASRC_EXT_CLK HDMI_TX_DDC_SDA KPP_ROW[3] I2C2_SDA USDHC1_VSELECT MX6Q_PER1_HADDR[6]	GPIO4[13]	
81	3V3	RXCAN	KEY_ROW4	CAN2_RXCAN IPU1_SISG[5] USBOH3_USBOTG_PWR KPP_ROW[4] UART5_CTS MMDC_DEBUG[50] MX6Q_PER1_HADDR[8]	GPIO4[15]	
82	GND	GND				

SSI 1 - Serial Audio Port 1

83	3V3	SSI1_INT	EIM_D26	WEIM_D[26] IPU1_DI1_PIN11 IPU1_CSI0_D[1] IPU2_CSI1_D[14] UART2_TXD_MUX IPU1_SISG[2] IPU1_DISP1_DAT[22]	GPIO3[26]	GPIO
84	3V3	SSI1_RXD	KEY_ROW1	ECSP11_SS0 ENET_COL AUDMUX_AUD5_RXD KPP_ROW[1] UART5_RXD_MUX USDHC2_VSELECT MX6Q_PER1_HADDR[2]	GPIO4[9]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	KEY_ROW0	ECSP11_MOSI ENET_TDATA[3] AUDMUX_AUD5_TXD KPP_ROW[0] UART4_RXD_MUX DCIC2_DCIC_OUT MX6Q_PER1_HADDR[0]	GPIO4[7]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	KEY_COL0	ECSP11_SCLK ENET_RDATA[3] AUDMUX_AUD5_TXC KPP_COL[0] UART4_TXD_MUX DCIC1_DCIC_OUT SRC_ANY_PU_RST	GPIO4[6]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	KEY_COL1	ECSP11_MISO ENET_MDIO AUDMUX_AUD5_TXFS KPP_COL[1] UART5_TXD_MUX USDHC1_VSELECT MX6Q_PER1_HADDR[1]	GPIO4[8]	Serial Audio Interface left/right clock
88	GND	GND				

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	EIM_D27	WEIM_D[27] IPU1_DI1_PIN13 IPU1_CSI0_D[0] IPU2_CSI1_D[13] UART2_RXD_MUX IPU1_SISG[3] IPU1_DISP1_DAT[23]	GPIO3[27]	GPIO
90	3V3	SSI2_RXD	CSI0_DAT7	IPU1_CSI0_D[7] WEIM_D[5] ECSPI1_SS0 KPP_ROW[6] AUDMUX_AUD3_RXD MMDC_DEBUG[46] MPCORE_TRACE[4]	GPIO5[25]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	CSI0_DAT5	IPU1_CSI0_D[5] WEIM_D[3] ECSPI1_MOSI KPP_ROW[5] AUDMUX_AUD3_TXD MMDC_DEBUG[44] MPCORE_TRACE[2]	GPIO5[23]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	CSI0_DAT4	IPU1_CSI0_D[4] WEIM_D[2] ECSPI1_SCLK KPP_COL[5] AUDMUX_AUD3_TXC MMDC_DEBUG[43] MPCORE_TRACE[1]	GPIO5[22]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	CSI0_DAT6	IPU1_CSI0_D[6] WEIM_D[4] ECSPI1_MISO KPP_COL[6] AUDMUX_AUD3_TXFS MMDC_DEBUG[45] MPCORE_TRACE[3]	GPIO5[24]	Serial Audio Interface left/right clock
94	GND	GND				
Secure Digital Interface 2						
95	3V3	SD2_CD	SD3_CLK	USDHC3_CLK UART2_RTS CAN1_RXCAN USB0H3_UH3_ DFD_OUT[5] USB0H3_UH2_ DFD_OUT[5] MIPI_CORE_DPHY_ TEST_IN[17]	GPIO7[3]	SD Card Detect – connected to a GPIO
96	3V3	SD2_D[0]	SD2_DAT0	USDHC2_DAT0 ECSPI5_MISO AUDMUX_AUD4_RXD KPP_ROW[7] DCIC2_DCIC_OUT	GPIO1[15]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
97	3V3	SD2_D[1]	SD2_DAT1	USDHC2_DAT1 ECSPI5_SS0 WEIM_CS[2] AUDMUX_AUD4_TXFS KPP_COL[7] CCM_WAIT	GPIO1[14]	
98	3V3	SD2_D[2]	SD2_DAT2	USDHC2_DAT2 ECSPI5_SS1 WEIM_CS[3] AUDMUX_AUD4_TXD KPP_ROW[6] CCM_STOP	GPIO1[13]	
99	3V3	SD2_D[3]	SD2_DAT3	USDHC2_DAT3 ECSPI5_SS3 KPP_COL[6] AUDMUX_AUD4_TXC PCIE_CTRL_DIAG_ STATUS_BUS_MUX[11] SJC_DONE	GPIO1[12]	

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
100	3V3	SD2_CMD	SD2_CMD	USDHC2_CMD ECSPI5_MOSI KPP_ROW[5] AUDMUX_AUD4_RXC PCIE_CTRL_DIAG_STATU S_BUS_MUX[10]	GPIO1[11]	SD Command bidirectional signal
101	3V3	SD2_CLK	SD2_CLK	USDHC2_CLK ECSPI5_SCLK KPP_COL[5] AUDMUX_AUD4_RXFS PCIE_CTRL_DIAG_ STATUS_BUS_MUX[9] PHY_DTB[1] SATA_PHY_DTB[1]	GPIO1[10]	SD Output Clock.
102	GND	GND				

CMOS Sensor Interface

103	3V3	CSI0_DAT12	CSI0_DAT12	IPU1_CSI0_D[12] WEIM_D[8] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[16] UART4_TXD_MUX SDMA_DEBUG_PC[6] MMDC_DEBUG[35] MPCORE_TRACE[9]	GPIO5[30]	
104	3V3	CSI0_DAT13	CSI0_DAT13	IPU1_CSI0_D[13] WEIM_D[9] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[17] UART4_RXD_MUX SDMA_DEBUG_PC[7] MMDC_DEBUG[36] MPCORE_TRACE[10]	GPIO5[31]	
105	3V3	CSI0_DAT14	CSI0_DAT14	IPU1_CSI0_D[14] WEIM_D[10] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[18] UART5_TXD_MUX SDMA_DEBUG_PC[8] MMDC_DEBUG[37] MPCORE_TRACE[11]	GPIO6[0]	
106	3V3	CSI0_DAT15	CSI0_DAT15	IPU1_CSI0_D[15] WEIM_D[11] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[19] UART5_RXD_MUX SDMA_DEBUG_PC[9] MMDC_DEBUG[38] MPCORE_TRACE[12]	GPIO6[1]	
107	3V3	CSI0_DAT16	CSI0_DAT16	IPU1_CSI0_D[16] WEIM_D[12] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[20] UART4_RTS SDMA_DEBUG_PC[10] MMDC_DEBUG[39] MPCORE_TRACE[13]	GPIO6[2]	
108	3V3	CSI0_DAT17	CSI0_DAT17	IPU1_CSI0_D[17] WEIM_D[13] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[21] UART4_CTS SDMA_DEBUG_PC[11] MMDC_DEBUG[40] MPCORE_TRACE[14]	GPIO6[3]	
109	3V3	CSI0_DAT18	CSI0_DAT18	IPU1_CSI0_D[18] WEIM_D[14] PCIE_CTRL_DIAG_ STATUS_BUS_MUX[22] UART5_RTS SDMA_DEBUG_PC[12] MMDC_DEBUG[41] MPCORE_TRACE[15]	GPIO6[4]	

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
110	3V3	CSI0_DAT19	CSI0_DAT19	IPU1_CSI0_D[19] WEIM_D[15] PCIE_CTRL_DIAG STATUS_BUS_MUX[23] UART5_CTS SDMA_DEBUG_PC[13] MMDC_DEBUG[42]	GPIO6[5]	
111	GND	GND				
112	3V3	CSI0_HSYNC	CSI0_MCLK	IPU1_CSI0_HSYNC PCIE_CTRL_DIAG STATUS_BUS_MUX[13] CCM_CLKO SDMA_DEBUG_PC[1] MMDC_DEBUG[30] MPCORE_TRCTL	GPIO5[19]	
113	3V3	CSI0_VSYNC	CSI0_VSYNC	IPU1_CSI0_VSYNC WEIM_D[1] PCIE_CTRL_DIAG STATUS_BUS_MUX[15] SDMA_DEBUG_PC[3] MMDC_DEBUG[32] MPCORE_TRACE[0]	GPIO5[21]	
114	3V3	CSI0_PIXCLK	CSI0_PIXCLK	IPU1_CSI0_PIXCLK PCIE_CTRL_DIAG STATUS_BUS_MUX[12] SDMA_DEBUG_PC[0] MMDC_DEBUG[29] MPCORE_EVENTO	GPIO5[18]	
115	3V3	CSI0_MCLK	GPIO_0	CCM_CLKO KPP_COL[5] EPIT1_EPITO USBOH3_USBH1_PWR SNVS_HP_WRAPPER_ SNVS_VIO_5	GPIO1[0]	
116	GND	GND				

LCD Controller and Smart LCD Controller

117	3V3	LD0	DISP0_DAT0	IPU1_DISP0_DAT[0] IPU2_DISP0_DAT[0] ECSPI3_SCLK USDHC1_USDHC_ DEBUG[0] SDMA_DEBUG_ CORE_RUN MMDC_DEBUG[5]	GPIO4[21]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX2_N	not available		TX6Q LVDS version: LVDS display output port 1
118	3V3	LD1	DISP0_DAT1	IPU1_DISP0_DAT[1] IPU2_DISP0_DAT[1] ECSPI3_MOSI USDHC1_USDHC_ DEBUG[1] SDMA_DEBUG_ EVENT_CHANNEL_SEL MMDC_DEBUG[6] MX6Q_PER1_HADDR[12]	GPIO4[22]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX1_N	not available		TX6Q LVDS version: LVDS display output port 1
119	3V3	LD2	DISP0_DAT2	IPU1_DISP0_DAT[2] IPU2_DISP0_DAT[2] ECSPI3_MISO USDHC1_USDHC_ DEBUG[2] SDMA_DEBUG_MODE MMDC_DEBUG[7] MX6Q_PER1_HADDR[13]	GPIO4[23]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX2_P	not available		TX6Q LVDS version: LVDS display output port 1
120	3V3	LD3	DISP0_DAT3	IPU1_DISP0_DAT[3] IPU2_DISP0_DAT[3] ECSPI3_SS0 USDHC1_USDHC_ DEBUG[3] SDMA_DEBUG_BUS_ERR MMDC_DEBUG[8] MX6Q_PER1_HADDR[14]	GPIO4[24]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX1_P	not available		TX6Q LVDS version: LVDS display output port 1

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
121	3V3	LD4	DISP0_DAT4	IPU1_DISP0_DAT[4] IPU2_DISP0_DAT[4] ECSP13_SS1 USDHC1_USDHC_DEBUG[4] SDMA_DEBUG_BUS_RWB MMD_C_DEBUG[9] MX6Q_PER1_HADDR[15]	GPIO4[25]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX3_N	not available		TX6Q LVDS version: LVDS display output port 1
122	3V3	LD5	DISP0_DAT5	IPU1_DISP0_DAT[5] IPU2_DISP0_DAT[5] ECSP13_SS2 AUDMUX_AUD6_RXFS SDMA_DEBUG_MATCHED_DMBUS MMD_C_DEBUG[10] MX6Q_PER1_HADDR[16]	GPIO4[26]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX0_N	not available		TX6Q LVDS version: LVDS display output port 1
123	3V3	LD6	DISP0_DAT6	IPU1_DISP0_DAT[6] IPU2_DISP0_DAT[6] ECSP13_SS3 AUDMUX_AUD6_RXC SDMA_DEBUG_RTBUFFER_WRITE MMD_C_DEBUG[11] MX6Q_PER1_HADDR[17]	GPIO4[27]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX3_P	not available		TX6Q LVDS version: LVDS display output port 1
124	3V3	LD7	DISP0_DAT7	IPU1_DISP0_DAT[7] IPU2_DISP0_DAT[7] ECSP13_RDY USDHC1_USDHC_DEBUG[5] SDMA_DEBUG_EVENT_CHANNEL[0] MMD_C_DEBUG[12] MX6Q_PER1_HADDR[18]	GPIO4[28]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_TX0_P	not available		TX6Q LVDS version: LVDS display output port 1
125	3V3	LD8	DISP0_DAT8	IPU1_DISP0_DAT[8] IPU2_DISP0_DAT[8] PWM1_PWM0 WDOG1_WDOG_B SDMA_DEBUG_EVENT_CHANNEL[1] MMD_C_DEBUG[13] MX6Q_PER1_HADDR[19]	GPIO4[29]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_CLK_N	not available		TX6Q LVDS version: LVDS display output port 1
126	3V3	LD9	DISP0_DAT9	IPU1_DISP0_DAT[9] IPU2_DISP0_DAT[9] PWM2_PWM0 WDOG2_WDOG_B SDMA_DEBUG_EVENT_CHANNEL[2] MMD_C_DEBUG[14] MX6Q_PER1_HADDR[20]	GPIO4[30]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX3_P	not available		TX6Q LVDS version: LVDS display output port 0
127	3V3	LD10	DISP0_DAT10	IPU1_DISP0_DAT[10] IPU2_DISP0_DAT[10] USDHC1_USDHC_DEBUG[6] SDMA_DEBUG_EVENT_CHANNEL[3] MMD_C_DEBUG[15] MX6Q_PER1_HADDR[21]	GPIO4[31]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS1_CLK_P	not available		TX6Q LVDS version: LVDS display output port 1
128	3V3	LD11	DISP0_DAT11	IPU1_DISP0_DAT[11] IPU2_DISP0_DAT[11] USDHC1_USDHC_DEBUG[7] SDMA_DEBUG_EVENT_CHANNEL[4] MMD_C_DEBUG[16] MX6Q_PER1_HADDR[22]	GPIO5[5]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX3_N	not available		TX6Q LVDS version: LVDS display output port 0

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
129	GND	GND				
130	3V3	LD12	DISP0_DAT12	IPU1_DISP0_DAT[12] IPU2_DISP0_DAT[12] SDMA_DEBUG_ EVENT_CHANNEL[5] MMDC_DEBUG[17] MX6Q_PER1_HADDR[23]	GPIO5[6]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_CLK_P	not available		TX6Q LVDS version: LVDS display output port 0
131	3V3	LD13	DISP0_DAT13	IPU1_DISP0_DAT[13] IPU2_DISP0_DAT[13] AUDMUX_AUD5_RXFS SDMA_DEBUG_ EVT_CHN_LINES[0] MMDC_DEBUG[18] MX6Q_PER1_HADDR[24]	GPIO5[7]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX2_P	not available		TX6Q LVDS version: LVDS display output port 0
132	3V3	LD14	DISP0_DAT14	IPU1_DISP0_DAT[14] IPU2_DISP0_DAT[14] AUDMUX_AUD5_RXC SDMA_DEBUG_ EVT_CHN_LINES[1] MMDC_DEBUG[19]	GPIO5[8]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_CLK_N	not available		TX6Q LVDS version: LVDS display output port 0
133	3V3	LD15	DISP0_DAT15	IPU1_DISP0_DAT[15] IPU2_DISP0_DAT[15] ECSPI1_SS1 ECSPI2_SS1 SDMA_DEBUG_ EVT_CHN_LINES[2] MMDC_DEBUG[20] MX6Q_PER1_HADDR[25]	GPIO5[9]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX2_N	not available		TX6Q LVDS version: LVDS display output port 0
134	3V3	LD16	DISP0_DAT16	IPU1_DISP0_DAT[16] IPU2_DISP0_DAT[16] ECSPI2_MOSI AUDMUX_AUD5_TXC SDMA_EXT_EVENT[0] MMDC_DEBUG[21] MX6Q_PER1_HADDR[26]	GPIO5[10]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX1_P	not available		TX6Q LVDS version: LVDS display output port 0
135	3V3	LD17	DISP0_DAT17	IPU1_DISP0_DAT[17] IPU2_DISP0_DAT[17] ECSPI2_MISO AUDMUX_AUD5_TXD SDMA_EXT_EVENT[1] MMDC_DEBUG[22] MX6Q_PER1_HADDR[27]	GPIO5[11]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX0_P	not available		TX6Q LVDS version: LVDS display output port 0
136	3V3	LD18	DISP0_DAT18	IPU1_DISP0_DAT[18] IPU2_DISP0_DAT[18] ECSPI2_SS0 AUDMUX_AUD5_TXFS AUDMUX_AUD4_RXFS MMDC_DEBUG[23] WEIM_CS[2]	GPIO5[12]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX1_N	not available		TX6Q LVDS version: LVDS display output port 0
137	3V3	LD19	DISP0_DAT19	IPU1_DISP0_DAT[19] IPU2_DISP0_DAT[19] ECSPI2_SCLK AUDMUX_AUD5_RXD AUDMUX_AUD4_RXC MMDC_DEBUG[24] WEIM_CS[3]	GPIO5[13]	TX6Q standard version: LCD Data Bus
	LVDS		LVDS0_TX0_N	not available		TX6Q LVDS version: LVDS display output port 0

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
138	3V3	LD20	DISP0_DAT20	IPU1_DISP0_DAT[20] IPU2_DISP0_DAT[20] ECSPI1_SCLK AUDMUX_AUD4_TXC SDMA_DEBUG_ EVT_CHN_LINES[7] MMDC_DEBUG[25] MX6Q_PER1_HADDR[28]	GPIO5[14]	TX6Q standard version: LCD Data Bus
	SATA		SATA_RXM	not available		TX6Q LVDS version: SATA port
139	3V3	LD21	DISP0_DAT21	IPU1_DISP0_DAT[21] IPU2_DISP0_DAT[21] ECSPI1_MOSI AUDMUX_AUD4_TXD SDMA_DEBUG_ BUS_DEVICE[0] MMDC_DEBUG[26] MX6Q_PER1_HADDR[29]	GPIO5[15]	TX6Q standard version: LCD Data Bus
	SATA		SATA_TXM	not available		TX6Q LVDS version: SATA port
140	3V3	LD22	DISP0_DAT22	IPU1_DISP0_DAT[22] IPU2_DISP0_DAT[22] ECSPI1_MISO AUDMUX_AUD4_TXFS SDMA_DEBUG_ BUS_DEVICE[1] MMDC_DEBUG[27] MX6Q_PER1_HADDR[30]	GPIO5[16]	TX6Q standard version: LCD Data Bus
	SATA		SATA_RXP	not available		TX6Q LVDS version: SATA port
141	3V3	LD23	DISP0_DAT23	IPU1_DISP0_DAT[23] IPU2_DISP0_DAT[23] ECSPI1_SS0 AUDMUX_AUD4_RXD SDMA_DEBUG_ BUS_DEVICE[2] MMDC_DEBUG[28] MX6Q_PER1_HADDR[31]	GPIO5[17]	TX6Q standard version: LCD Data Bus
	SATA		SATA_TXP	not available		TX6Q LVDS version: SATA port
142	GND	GND				
143	3V3	HSYNC	DIO_PIN2	IPU1_DIO_PIN2 IPU2_DIO_PIN2 AUDMUX_AUD6_TXD MIPI_CORE_ DPHY_TEST_OUT[30] SDMA_DEBUG_ CORE_STATE[2] MMDC_DEBUG[2] MX6Q_PER1_HADDR[9]	GPIO4[18]	
144	3V3	VSYNC	DIO_PIN3	IPU1_DIO_PIN3 IPU2_DIO_PIN3 AUDMUX_AUD6_TXFS MIPI_CORE_ DPHY_TEST_OUT[31] SDMA_DEBUG_ CORE_STATE[3] MMDC_DEBUG[3] MX6Q_PER1_HADDR[10]	GPIO4[19]	
145	3V3	OE_ACD	DIO_PIN15	IPU1_DIO_PIN15 IPU2_DIO_PIN15 AUDMUX_AUD6_TXC MIPI_CORE_ DPHY_TEST_OUT[29] SDMA_DEBUG_ CORE_STATE[1] MMDC_DEBUG[1]	GPIO4[17]	
146	3V3	LSCLK	DIO_DISP_CLK	IPU1_DIO_DISP_CLK IPU2_DIO_DISP_CLK MIPI_CORE_ DPHY_TEST_OUT[28] SDMA_DEBUG_ CORE_STATE[0] MMDC_DEBUG[0]	GPIO4[16]	
147	GND	GND				

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
Module Specific Signals						
148	3V3	CSI1_MCLK	NANDF_CS2	RAWNAND_CE2N IPU1_SISG[0] ESAI1_TX0 WEIM_CRE CCM_CLKO2 IPU2_SISG[0] WEIM_A[16]	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	IPU1_DI1_DISP_CLK IPU2_CSI1_PIXCLK MIPI_CORE_ DPHY_TEST_OUT[23] TPSMP_HDATA[6] SRC_BT_CFG[16]	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	WEIM_D[29] IPU1_DI1_PIN15 ECSPI4_SS0 UART2_RTS IPU2_CSI1_VSYNC IPU1_DIO_PIN14	GPIO3[29]	
151	3V3	CSI1_HSYNC	EIM_EB3	WEIM_EB[3] ECSPI4_RDY UART3_RTS UART1_RI IPU2_CSI1_HSYNC IPU1_DI1_PIN3 SRC_BT_CFG[31]	GPIO2[31]	
152	3V3	CSI1_D[12]	EIM_A17	WEIM_A[17] IPU1_DISP1_DAT[12] IPU2_CSI1_D[12] MIPI_CORE_ DPHY_TEST_OUT[22] TPSMP_HDATA[5] SRC_BT_CFG[17]	GPIO2[21]	
153	3V3	CSI1_D[13]	EIM_A18	WEIM_A[18] IPU1_DISP1_DAT[13] IPU2_CSI1_D[13] MIPI_CORE_ DPHY_TEST_OUT[21] TPSMP_HDATA[4] SRC_BT_CFG[18]	GPIO2[20]	
154	3V3	CSI1_D[14]	EIM_A19	WEIM_A[19] IPU1_DISP1_DAT[14] IPU2_CSI1_D[14] MIPI_CORE_ DPHY_TEST_OUT[20] TPSMP_HDATA[3] SRC_BT_CFG[19]	GPIO2[19]	
155	3V3	CSI1_D[15]	EIM_A20	WEIM_A[20] IPU1_DISP1_DAT[15] IPU2_CSI1_D[15] MIPI_CORE_ DPHY_TEST_OUT[19] TPSMP_HDATA[2] SRC_BT_CFG[20]	GPIO2[18]	
156	3V3	CSI1_D[16]	EIM_A21	WEIM_A[21] IPU1_DISP1_DAT[16] IPU2_CSI1_D[16] MIPI_CORE_ DPHY_TEST_OUT[18] TPSMP_HDATA[1] SRC_BT_CFG[21]	GPIO2[17]	
157	3V3	CSI1_D[17]	EIM_A22	WEIM_A[22] IPU1_DISP1_DAT[17] IPU2_CSI1_D[17] TPSMP_HDATA[0] SRC_BT_CFG[22]	GPIO2[16]	
158	3V3	CSI1_D[18]	EIM_A23	WEIM_A[23] IPU1_DISP1_DAT[18] IPU2_CSI1_D[18] IPU2_SISG[3] IPU1_SISG[3] MX6Q_PER1_HPROT[3] SRC_BT_CFG[23]	GPIO6[6]	

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
159	3V3	CSI1_D[19]	EIM_A24	WEIM_A[24] IPU1_DISP1_DAT[19] IPU2_CSI1_D[19] IPU2_SISG[2] IPU1_SISG[2] MX6Q_PER1_HPROT[2] SRC_BT_CFG[24]	GPIO5[4]	
160	GND	GND				
161	3V3		CSI0_DAT8	IPU1_CSI0_D[8] WEIM_D[6] ECSP12_SCLK KPP_COL[7] I2C1_SDA MMDC_DEBUG[47] MPCORE_TRACE[5]	GPIO5[26]	
162	3V3		CSI0_DAT9	IPU1_CSI0_D[9] WEIM_D[7] ECSP12_MOSI KPP_ROW[7] I2C1_SCL MMDC_DEBUG[48] MPCORE_TRACE[6]	GPIO5[27]	
163	3V3		CSI0_DAT10	IPU1_CSI0_D[10] AUDMUX_AUD3_RXC ECSP12_MISO UART1_TXD_MUX SDMA_DEBUG_PC[4] MMDC_DEBUG[33] MPCORE_TRACE[7]	GPIO5[28]	
164	3V3		CSI0_DAT11	IPU1_CSI0_D[11] AUDMUX_AUD3_RXFS ECSP12_SS0 UART1_RXD_MUX SDMA_DEBUG_PC[5] MMDC_DEBUG[34] MPCORE_TRACE[8]	GPIO5[29]	
165	3V3		EIM_D22	WEIM_D[22] ECSP14_MISO IPU1_D10_PIN1 IPU2_CSI1_D[10] USB0H3_USBOTG_PWR SPDIF_OUT1 MX6Q_PER_HWRITE	GPIO3[22]	
166	LVDS		CLK1_N			Alternate reference clock for PCIe
167	LVDS		PCI_E_RXM			
168	LVDS		CLK1_P			Alternate reference clock for PCIe
169	LVDS		PCI_E_RXP			
170	LVDS		PCI_E_TXM			
171	GND	GND				
172	LVDS		PCI_E_TXP			
173	3V3	EIM_CS0	EIM_CS0	WEIM_CS[0] IPU1_DI1_PIN5 ECSP12_SCLK MIPI_CORE_ DPHY_TEST_OUT[24] TPSMP_HDATA[7]	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	WEIM_CS[1] IPU1_DI1_PIN6 ECSP12_MOSI MIPI_CORE_ DPHY_TEST_OUT[25] TPSMP_HDATA[8]	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	IPU1_CSI0_DATA_EN WEIM_D[0] PCI_E_CTRL_DIAG_ STATUS_BUS_MUX[14] SDMA_DEBUG_PC[2] MMDC_DEBUG[31] MPCORE_TRCLK	GPIO5[20]	
176	3V3	EIM_WAIT	EIM_WAIT	WEIM_WAIT WEIM_DTACK_B TPSMP_HDATA[30] SRC_BT_CFG[25]	GPIO5[0]	

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
177	3V3	EIM_EB0	EIM_EB0	WEIM_EB[0] IPU1_DISP1_DAT[11] IPU2_CSI1_D[11] MIPI_CORE_ DPHY_TEST_OUT[0] CCM_PMIC_RDY TPSMP_HDATA[12] SRC_BT_CFG[27]	GPIO2[28]	
178	3V3	EIM_EB1	EIM_EB1	WEIM_EB[1] IPU1_DISP1_DAT[10] IPU2_CSI1_D[10] MIPI_CORE_ DPHY_TEST_OUT[1] TPSMP_HDATA[13] SRC_BT_CFG[28]	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	WEIM_OE IPU1_DI1_PIN7 ECSPI2_MISO MIPI_CORE_ DPHY_TEST_OUT[26] TPSMP_HDATA[9]	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	WEIM_LBA IPU1_DI1_PIN17 ECSPI2_SS1 TPSMP_HDATA[11] SRC_BT_CFG[26]	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	WEIM_RW IPU1_DI1_PIN8 ECSPI2_SS0 MIPI_CORE_ DPHY_TEST_OUT[27] TPSMP_HDATA[10] SRC_BT_CFG[29]	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	WEIM_BCLK IPU1_DI1_PIN16 GPIO6_GPIO[31] TPSMP_HDATA[31]	GPIO6[31]	TX6Q NAND version
	POWER		NVCC_RGMII NVCC_ENET	1V8 power supply output RN5T618 LOD4 max.:180mA		TX6Q eMMC version
183	GND	GND				
184	3V3	EIM_DA0	EIM_DA0	WEIM_DA_A[0] IPU1_DISP1_DAT[9] IPU2_CSI1_D[9] MIPI_CORE_ DPHY_TEST_OUT[2] TPSMP_HDATA[14] SRC_BT_CFG[0]	GPIO3[0]	TX6Q NAND version
	1V8	ENET_REF_CLK	ENET_REF_CLK	ENET_TX_CLK ESAI_RX_FS SPDIF_SR_CLK	GPIO1[23]	TX6Q eMMC version
185	3V3	EIM_DA1	EIM_DA1	WEIM_DA_A[1] IPU1_DISP1_DAT[8] IPU2_CSI1_D[8] MIPI_CORE_ DPHY_TEST_OUT[3] TPSMP_HDATA[15] SRC_BT_CFG[1]	GPIO3[1]	TX6Q NAND version
	1V8	ENET0_MDC	ENET0_MDC	Fixed function		TX6Q eMMC version
186	3V3	EIM_DA2	EIM_DA2	WEIM_DA_A[2] IPU1_DISP1_DAT[7] IPU2_CSI1_D[7] MIPI_CORE_ DPHY_TEST_OUT[4] TPSMP_HDATA[16] SRC_BT_CFG[2]	GPIO3[2]	TX6Q NAND version
	1V8	ENET0_MDIO	ENET0_MDIO	Fixed function		TX6Q eMMC version

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
187	3V3	EIM_DA3	EIM_DA3	WEIM_DA_A[3] IPU1_DISP1_DAT[6] IPU2_CSI1_D[6] MIPI_CORE_ DPHY_TEST_OUT[5] TPSMP_HDATA[17] SRC_BT_CFG[3]	GPIO3[3]	TX6Q NAND version
	POWER			1V2 power supply output RN5T618 LOD5 max.:200mA		TX6Q eMMC version
188	3V3	EIM_DA4	EIM_DA4	WEIM_DA_A[4] IPU1_DISP1_DAT[5] IPU2_CSI1_D[5] MIPI_CORE_ DPHY_TEST_OUT[6] TPSMP_HDATA[18] SRC_BT_CFG[4]	GPIO3[4]	TX6Q NAND version
	1V8	RGMII_RXC	RGMII_RXC	USB_H3_STROBE	GPIO6[30]	TX6Q eMMC version
189	3V3	EIM_DA5	EIM_DA5	WEIM_DA_A[5] IPU1_DISP1_DAT[4] IPU2_CSI1_D[4] MIPI_CORE_ DPHY_TEST_OUT[7] TPSMP_HDATA[19] SRC_BT_CFG[5]	GPIO3[5]	TX6Q NAND version
	1V8	RGMII_RD3	RGMII_RD3	HSI_TX_WAKE	GPIO6[29]	TX6Q eMMC version
190	3V3	EIM_DA6	EIM_DA6	WEIM_DA_A[6] IPU1_DISP1_DAT[3] IPU2_CSI1_D[3] MIPI_CORE_ DPHY_TEST_OUT[8] TPSMP_HDATA[20] SRC_BT_CFG[6]	GPIO3[6]	TX6Q NAND version
	1V8	RGMII_RD2	RGMII_RD2	HSI_TX_DATA	GPIO6[28]	TX6Q eMMC version
191	3V3	EIM_DA7	EIM_DA7	WEIM_DA_A[7] IPU1_DISP1_DAT[2] IPU2_CSI1_D[2] MIPI_CORE_ DPHY_TEST_OUT[9] TPSMP_HDATA[21] SRC_BT_CFG[7]	GPIO3[7]	TX6Q NAND version
	1V8	RGMII_RD1	RGMII_RD1	HSI_TX_FLAG	GPIO6[27]	TX6Q eMMC version
192	3V3	EIM_DA8	EIM_DA8	WEIM_DA_A[8] IPU1_DISP1_DAT[1] IPU2_CSI1_D[1] MIPI_CORE_ DPHY_TEST_OUT[10] TPSMP_HDATA[22] SRC_BT_CFG[8]	GPIO3[8]	TX6Q NAND version
	1V8	RGMII_RD0	RGMII_RD0	HSI_RX_READY	GPIO6[25]	TX6Q eMMC version
193	3V3	EIM_DA9	EIM_DA9	WEIM_DA_A[9] IPU1_DISP1_DAT[0] IPU2_CSI1_D[0] MIPI_CORE_ DPHY_TEST_OUT[11] TPSMP_HDATA[23] SRC_BT_CFG[9]	GPIO3[9]	TX6Q NAND version
	1V8	RGMII_RX_CTL	RGMII_RX_CTL	USB_H3_DATA	GPIO6[24]	TX6Q eMMC version

PIN	Type	Function	i.MX6 Quad Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
194	3V3	EIM_DA10	EIM_DA10	WEIM_DA_A[10] IPU1_DI1_PIN15 IPU2_CSI1_DATA_EN MIPI_CORE_ DPHY_TEST_OUT[12] TPSMP_HDATA[24] SRC_BT_CFG[10]	GPIO3[10]	TX6Q NAND version
	1V8	RGMII_TD3	RGMII_TD3	HSI_RX_WAKE	GPIO6[23]	TX6Q eMMC version
195	3V3	EIM_DA11	EIM_DA11	WEIM_DA_A[11] IPU1_DI1_PIN2 IPU2_CSI1_HSYNCS MIPI_CORE_ DPHY_TEST_OUT[13] SDMA_DEBUG_ EVT_CHN_LINES[6] TPSMP_HDATA[25] SRC_BT_CFG[11]	GPIO3[11]	TX6Q NAND version
	1V8	RGMII_TD2	RGMII_TD2	HSI_RX_DATA	GPIO6[22]	TX6Q eMMC version
196	3V3	EIM_DA12	EIM_DA12	WEIM_DA_A[12] IPU1_DI1_PIN3 IPU2_CSI1_VSYNCS MIPI_CORE_ DPHY_TEST_OUT[14] SDMA_DEBUG_ EVT_CHN_LINES[3] TPSMP_HDATA[26] SRC_BT_CFG[12]	GPIO3[12]	TX6Q NAND version
	1V8	RGMII_TD1	RGMII_TD1	HSI_RX_FLAG	GPIO6[21]	TX6Q eMMC version
197	3V3	EIM_DA13	EIM_DA13	WEIM_DA_A[13] IPU1_DI1_D0_CS CCM_DI1_EXT_CLK MIPI_CORE_ DPHY_TEST_OUT[15] SDMA_DEBUG_ EVT_CHN_LINES[4] TPSMP_HDATA[27] SRC_BT_CFG[13]	GPIO3[13]	TX6Q NAND version
	1V8	RGMII_TD0	RGMII_TD0	HSI_TX_READY	GPIO6[20]	TX6Q eMMC version
198	3V3	EIM_DA14	EIM_DA14	WEIM_DA_A[14] IPU1_DI1_D1_CS CCM_DI0_EXT_CLK MIPI_CORE_ DPHY_TEST_OUT[16] SDMA_DEBUG_ EVT_CHN_LINES[5] TPSMP_HDATA[28] SRC_BT_CFG[14]	GPIO3[14]	TX6Q NAND version
	1V8	RGMII_TX_CTL	RGMII_TX_CTL	USB_H2_STROBE ENET_REF_CLK	GPIO6[26]	TX6Q eMMC version
199	3V3	EIM_DA15	EIM_DA15	WEIM_DA_A[15] IPU1_DI1_PIN1 IPU1_DI1_PIN4 MIPI_CORE_ DPHY_TEST_OUT[17] TPSMP_HDATA[29] SRC_BT_CFG[15]	GPIO3[15]	TX6Q NAND version
	1V8	RGMII_TXC	RGMII_TXC	USB_H2_DATA SPDIF_EXT_CLK XTALOSC_REF_CLK_24M	GPIO6[19]	TX6Q eMMC version
200	GND	GND				

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