N *National Semiconductor*

LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage — 1 mV (max)
- Input offset voltage drift — 10 μV/°C (max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 3 MHz (min)
- High slew rate — 10V/μs (min)
- Low supply current — 1.8 mA/Amplifier
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz — ≤0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

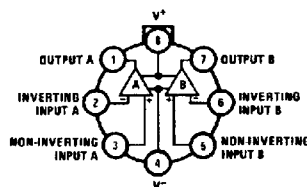## Typical Connection
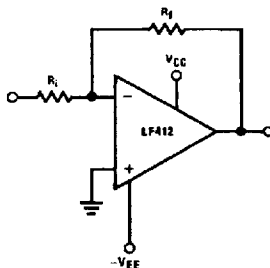
Ordering Information

LF412XYZ

X indicates electrical grade
Y indicates temperature range
    "M" for military
    "C" for commercial
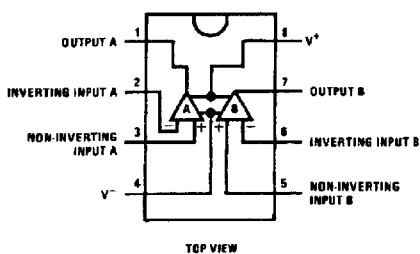**Z** indicates package type
    "H" or "N"

Connection Diagrams

Metal Can Package

Note. Pin 4 connected to case.
TOP VIEW

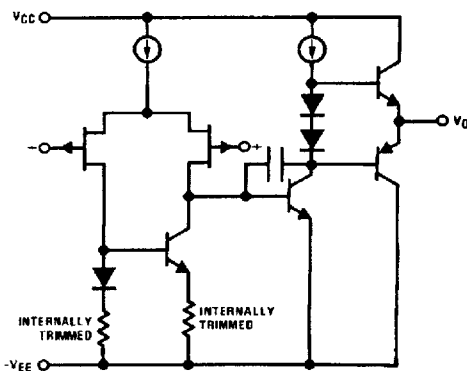**Order Number LF412AMH, LF412MH, LF412CH or LF412MH/883***
See NS Package Number H08A

Simplified Schematic

1/2 Dual

*Available per JM38510/11905

BI-FET II™ is a trademark of National Semiconductor Corporation.

Dual-In-Line Package

TOP VIEW

TL/H/5656–1

Order Number LF412ACN, LF412CN or LF412MJ/883*
See NS Package Number J08A or N08E

RRD-B30M115/Printed in U. S. A.

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

	LF412A	LF412		H Package	N Package
Supply Voltage	± 22V	± 18V	Power Dissipation (Note 10)	(Note 3)	670 mW
Differential Input Voltage	± 38V	± 30V	T_j max	150°C	115°C
Input voltage Range (Note 1)	± 19V	± 15V	θ_{jA} (Typical)	152°C/W	115°C/W
			Operating Temp. Range	(Note 4)	(Note 4)
Output Short Circuit Duration (Note 2)	Continuous	Continuous	Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
			Lead Temp. (Soldering, 10 sec.)	260°C	260°C
			ESD Tolerance (Note 11)	1700V	1700V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A			LF412			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10$ kΩ (Note 6)			7	10		7	20	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15$V (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15$V (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15$V, $V_O = \pm 10$V, $R_L = 2$k, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15$V, $R_L = 10$k		± 12	± 13.5		± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range			± 16	$+19.5$		± 11	$+14.5$		V
					-16.5			-11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10$k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current	$V_O = 0$V, $R_L = \infty$			3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		-120			-120		dB
SR	Slew Rate	$V_S = \pm 15$V, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15$V, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

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Typical Performance Characteristics

TL/H/5656-2

3
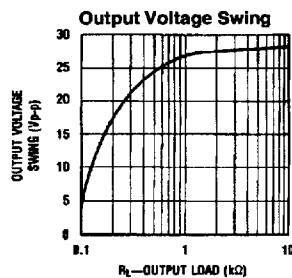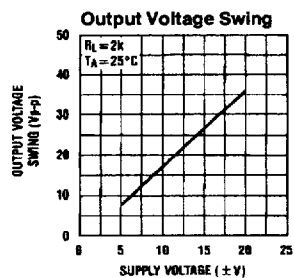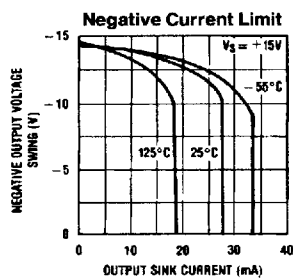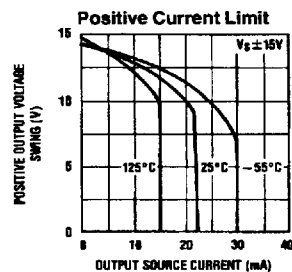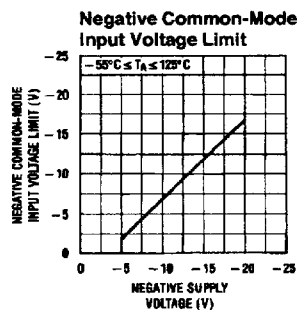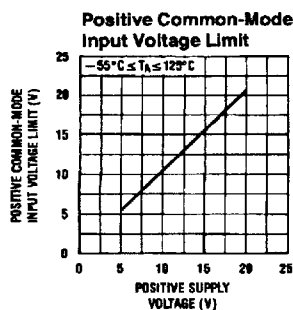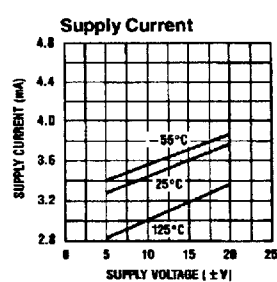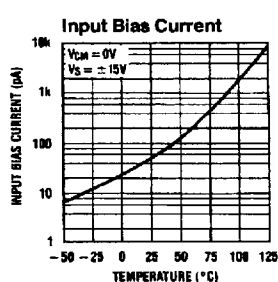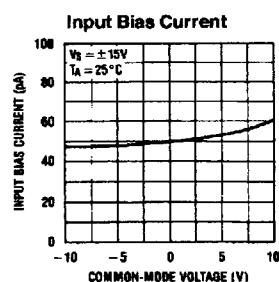
Typical Performance Characteristics (Continued)

Gain Bandwidth

Bode Plot

Slew Rate

Distortion vs Frequency

Undistorted Output Voltage Swing

Open Loop Frequency Response

Common-Mode Rejection Ratio

Power Supply Rejection Ratio

Equivalent Input Noise Voltage

Open Loop Voltage Gain

Output Impedance

Inverter Settling Time

TL/H/5656-3

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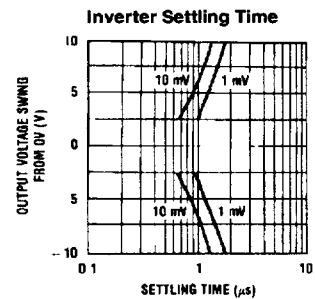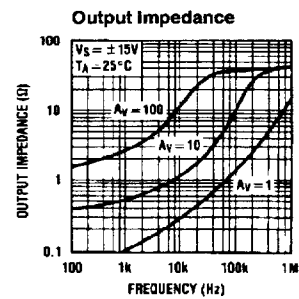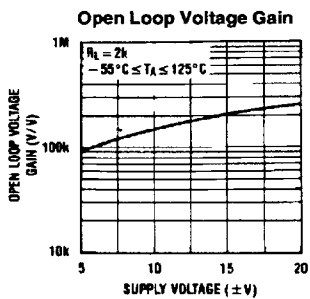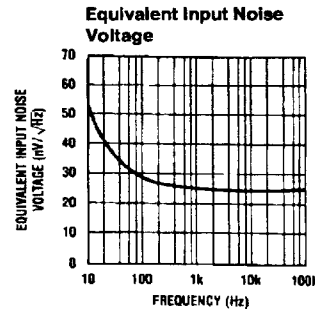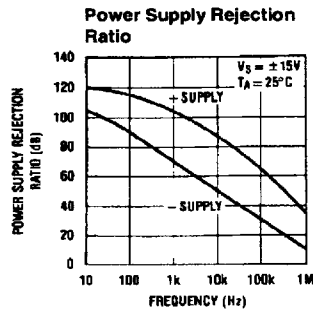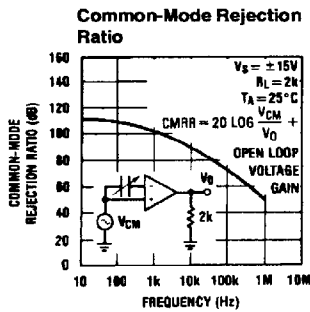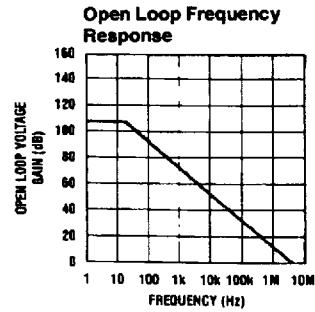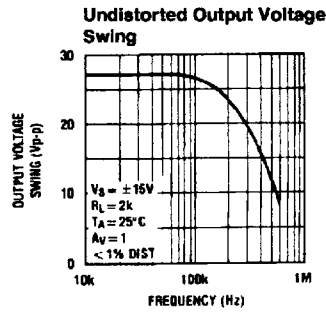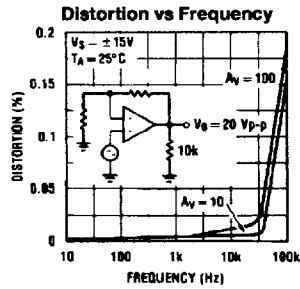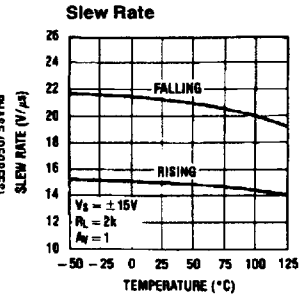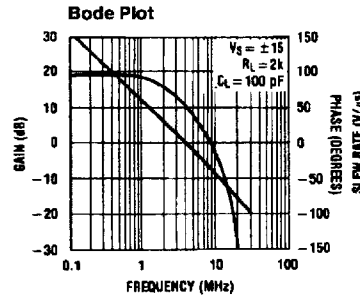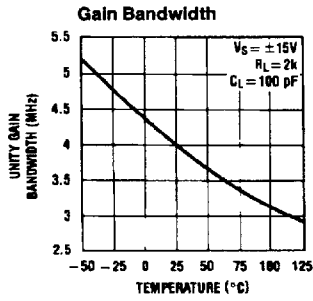
Pulse Response $R_L = 2\,k\Omega$, $C_L = 10\,pF$

Small Signal Inverting
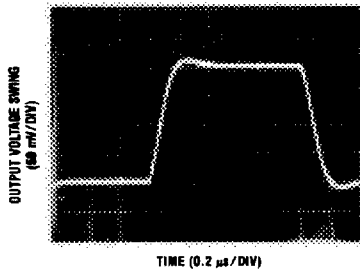
OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.2 µs/DIV)

Small Signal Non-Inverting

OUTPUT VOLTAGE SWING (50 mV/DIV)

TIME (0.2 µs/DIV)

Large Signal Inverting

OUTPUT VOLTAGE SWING (5V/DIV)

TIME (2 µs/DIV)

Large Signal Non-Inverting

OUTPUT VOLTAGE SWING (5V/DIV)

TIME (2 µs/DIV)

Current Limit ($R_L = 100\,\Omega$)

OUTPUT VOLTAGE SWING (1V/DIV)

TIME (5 µs/DIV)
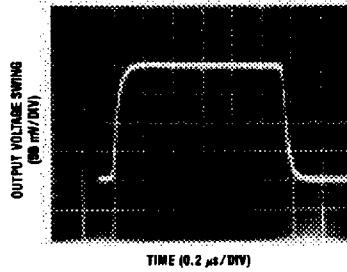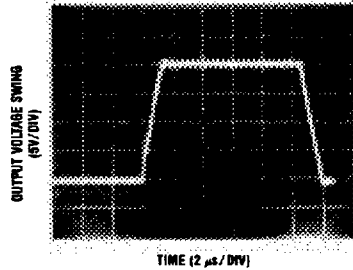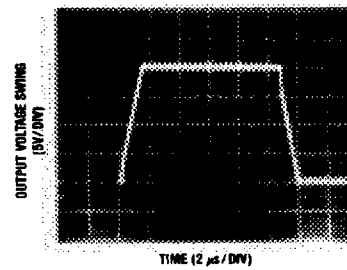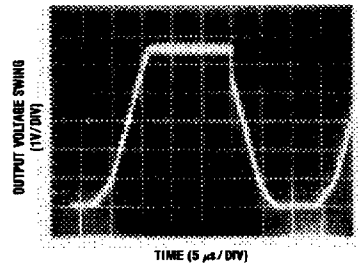
TL/H/5656-4

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

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Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.
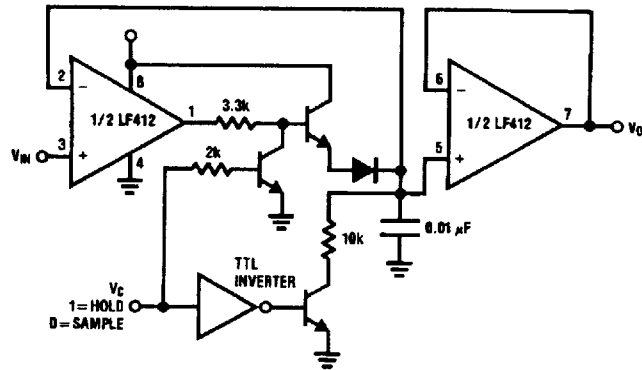
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.
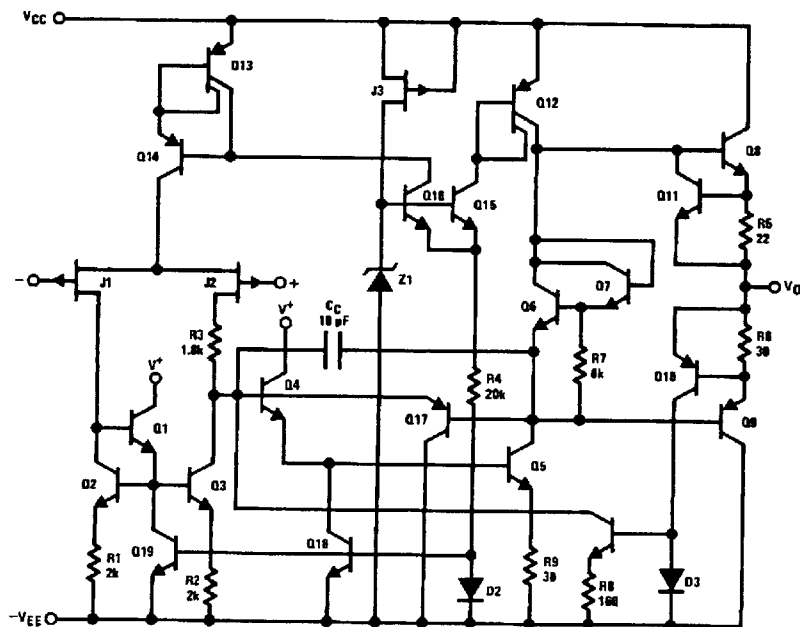
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

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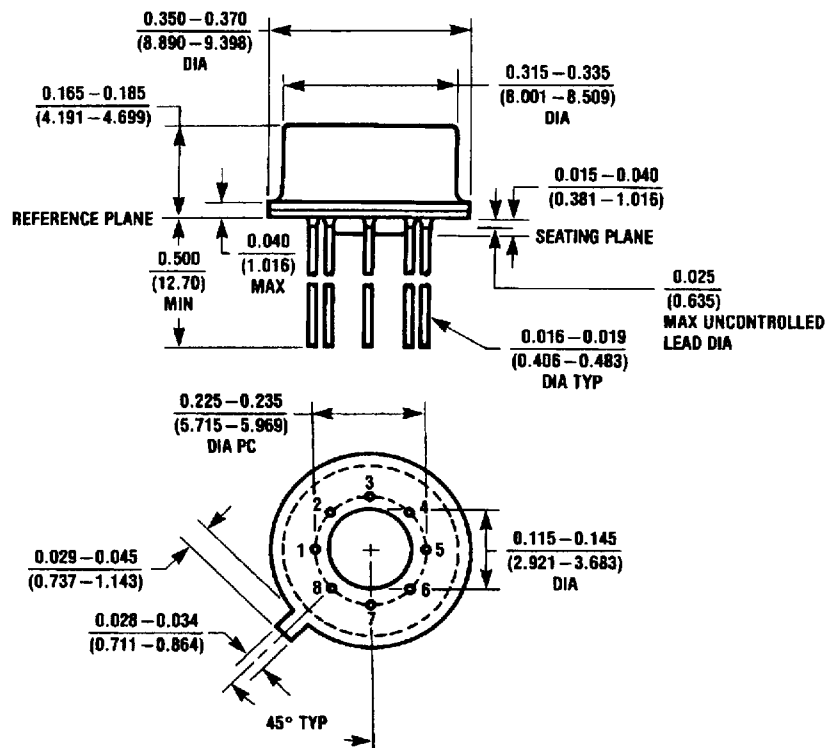## Typical Application

**Single Supply Sample and Hold**

Detailed Schematic

TL/H/5656-9

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Physical Dimensions inches (millimeters)

0.350 − 0.370
(8.890 − 9.398)
DIA

0.315 − 0.335
(8.001 − 8.509)
DIA

0.165 − 0.185
(4.191 − 4.699)

0.015 − 0.040
(0.381 − 1.016)

REFERENCE PLANE

SEATING PLANE

0.040
(1.016)
MAX

0.500
(12.70)
MIN

0.025
(0.635)
MAX UNCONTROLLED
LEAD DIA

0.016 − 0.019
(0.406 − 0.483)
DIA TYP

0.225 − 0.235
(5.715 − 5.969)
DIA PC

0.029 − 0.045
(0.737 − 1.143)

0.115 − 0.145
(2.921 − 3.683)
DIA

0.028 − 0.034
(0.711 − 0.864)

45° TYP

H08A (REV C)

Metal Can Package (H)
Order Number LF412AMH, LF412MH, LF412MH/883 or LF412CH
NS Package Number H08A

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Physical Dimensions inches (millimeters) (Continued)

Dual-In-Line Package (J)
Order Number LF412MJ/883
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)

Dual-In-Line Package (N)
Order Number LF412ACN or LF412CN
NS Package Number N08E
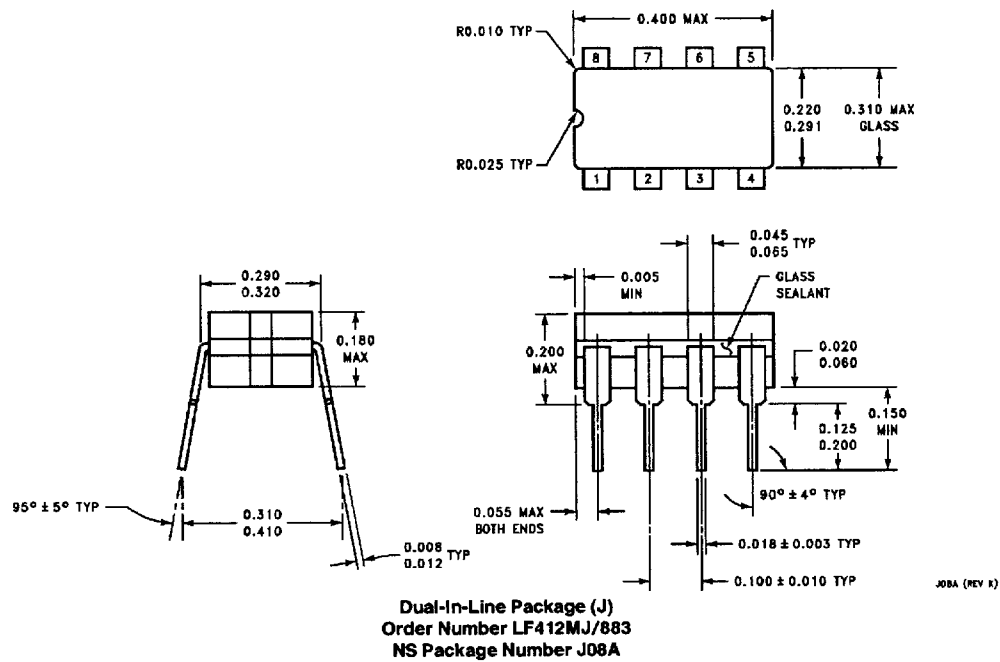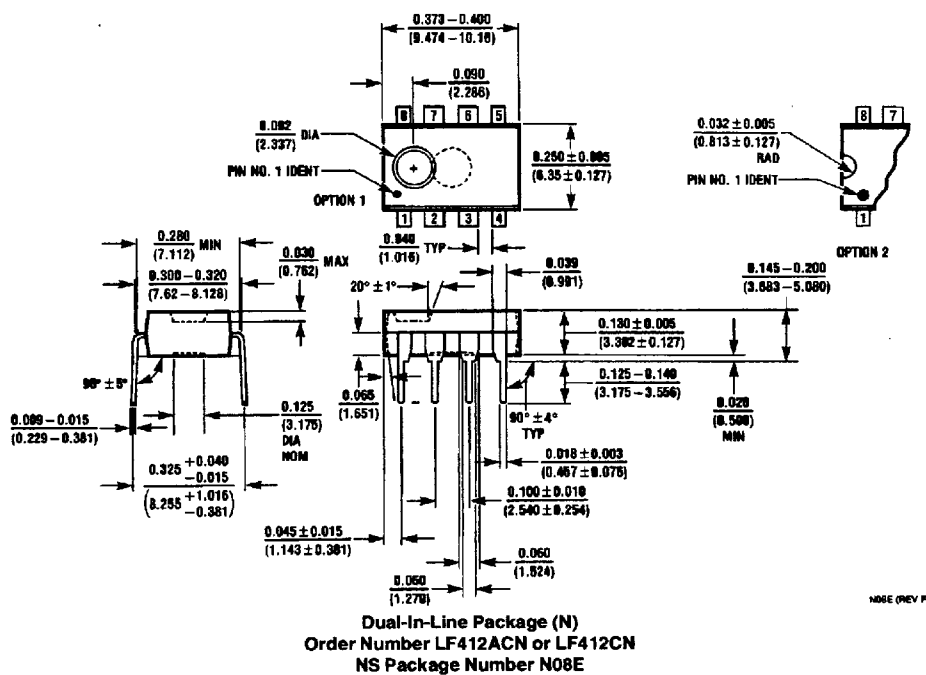
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.