



Dual 36V Op Amp for 18-Bit SAR ADC Front-End

General Description

The MAX9633 is a low-noise, low-distortion operational amplifier that is optimized to drive ADCs for use in applications from DC to a few MHz. The MAX9633 features low noise (3nV/ $\sqrt{\text{Hz}}$ at 1kHz and 3.5nV/ $\sqrt{\text{Hz}}$ at 100Hz) and low distortion (130dB at 10kHz), making it suitable for industrial, medical, and test applications.

The exceptionally fast settling-time and low input offset voltage makes the IC an excellent solution to drive high-resolution 12-bit to 18-bit SAR ADCs.

The IC operates from a wide supply voltage range up to 36V with only 3.5mA of quiescent current per amplifier.

The IC is offered in an 8-pin, 3mm x 3mm TDFN package for operation over the -40°C to +125°C temperature range.

Applications

ADC Drivers
Data Acquisition and Instrumentation
Power Grid Systems
Motor Control
Test and Measurement Equipments
Imaging Systems
High-Performance Audio Circuitry

Features

- ♦ Low-Noise (3nV/ $\sqrt{\text{Hz}}$ at 1kHz) and Low-Distortion (130dB at 10kHz) ADC Driver
- ♦ Very Fast 750ns Settling Time to 16-Bit Accuracy
- ♦ Low Input Voltage Offset 200 μV (max)
- ♦ Low 0.9 $\mu\text{V}/^\circ\text{C}$ Input Offset Temperature Coefficient
- ♦ Gain-Bandwidth Product 27MHz
- ♦ 4.5V to 36V Wide Supply Range
- ♦ Unity Gain Stable
- ♦ $\pm 5\text{kV}$ ESD Protection HBM
- ♦ 8-Pin TDFN and SO Packages

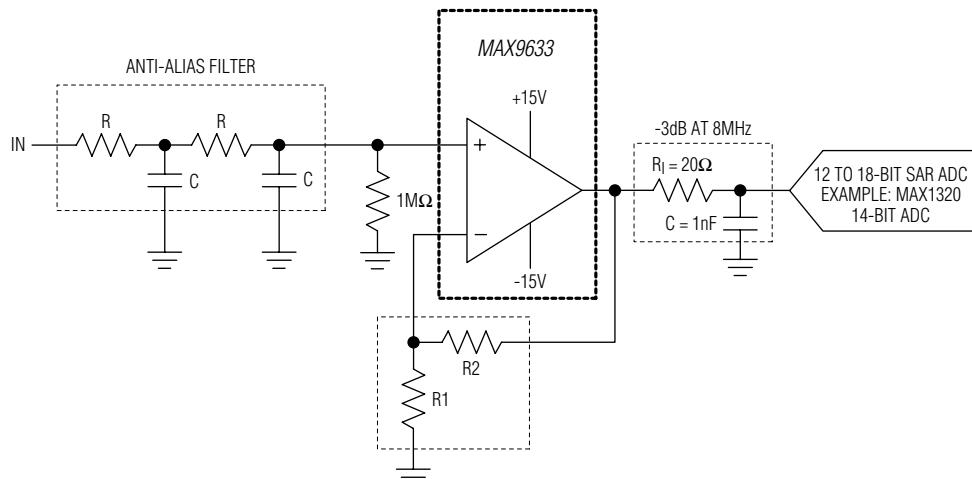
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9633ASA+	-40°C to +125°C	8 SO-EP*	—
MAX9633ATA+	-40°C to +125°C	8 TDFN-EP*	BMM

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC to VEE).....	-0.3V to +40V
All Other Pins.....	(VEE - 0.3V) to (VCC + 0.3V)
Short-Circuit Duration of OUTA, OUTB	10s
Continuous Input Current (any pins).....	$\pm 20\text{mA}$
Continuous Power Dissipation (TA = +70°C)	
SO (derate 24.4mW/°C above +70°C)	
Multilayer Board	1951.2mW

TDFN (derate 24.4mW/°C above +70°C)	
Multilayer Board	1905mW
Operating Temperature Range.....	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range.....	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SO-EP

Junction-to-Ambient Thermal Resistance (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	7°C/W

TDFN-EP

Junction-to-Ambient Thermal Resistance (θ_{JA})	42°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +15V, VEE = -15V, VCM = 0V, RL = 10k Ω to VGND = 0V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	VCC - VEE	Guaranteed by PSRR	4.5	36		V
Supply Current	I _{CC}	Per amplifier	TA = +25°C	3.5	5	mA
			-40°C \leq TA \leq +85°C	6		
			-40°C \leq TA \leq +125°C	6.5		
Power-Supply Rejection Ratio	PSRR	+4.5V \leq (VCC - VEE) \leq +36V	TA = +25°C	112	135	dB
			-40°C \leq TA \leq +125°C	110		
DC SPECIFICATIONS						
Input Offset Voltage	V _{OS}	TA = +25°C		± 70	± 200	μV
		-40°C \leq TA \leq +125°C			± 290	
Input Offset Voltage Drift (Note 3)	ΔV_{OS}	-40°C \leq TA \leq +125°C		0.2	0.9	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I _B	(VEE + 0.45V) \leq V _{CM} \leq (VCC - 1.8V)		± 42	± 400	nA
		VEE \leq V _{CM} \leq (VCC - 1.8V)		4.5	22	μA
Input Offset Current	I _{OS}	(VEE + 0.45V) \leq V _{CM} \leq (VCC - 1.8V)		± 30	± 300	nA
		VEE \leq V _{CM} \leq (VCC - 1.8V)		± 200	± 2000	
Input Voltage Range	V _{IN+} , V _{IN-}	Guaranteed by CMRR	TA = +25°C	V _{EE}	V _{CC} - 1.7	V
			-40°C \leq TA \leq +125°C	V _{EE}	V _{CC} - 1.8	
Common-Mode Rejection Ratio	CMRR	V _{EE} \leq V _{CM} \leq (VCC - 1.7V), TA = +25°C		106	130	dB
		V _{EE} \leq V _{CM} \leq (VCC - 1.8V), -40°C \leq TA \leq +125°C		105	130	

**Dual 36V Op Amp for 18-Bit
SAR ADC Front-End****ELECTRICAL CHARACTERISTICS (continued)**

($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to $V_{GND} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Open-Loop Gain	AVOL	$(V_{EE} + 0.3V) \leq V_{OUT} \leq (V_{CC} - 2V)$, $R_L = 10k\Omega$	118	140		dB
		$(V_{EE} + 0.45V) \leq V_{OUT} \leq (V_{CC} - 2.1V)$, $R_L = 1k\Omega$	115	138		
Output Voltage Swing	VOH	$V_{CC} - V_{OUT}$	$R_L = 10k\Omega$	1.6	1.9	V
			$R_L = 1k\Omega$	1.7	2.0	
	VOL	$V_{OUT} - V_{EE}$	$R_L = 10k\Omega$	70	150	mV
			$R_L = 1k\Omega$	170	300	
			$R_L = 10k\Omega$ to V_{EE}	20	100	
			$R_L = 1k\Omega$ to V_{EE}	20	100	
Short-Circuit Current	ISC	$T_A = +25^\circ C$		50		mA
AC SPECIFICATIONS						
Gain Bandwidth	GBWP		27			MHz
Slew Rate	SR	5V step, $R_S = 20\Omega$, $C_L = 1nF$, $AV = 1V/V$	18			V/ μ s
Output Transient Recovery Time	tTR	To 0.001%, $\Delta V_{OUT} = 200mV$, $R_S = 20\Omega$, $C_L = 1nF$, $AV = +1V/V$	500			ns
Settling Time	tS	To 0.001%, 5V step, $AV = -1V/V$	$R_S = 100\Omega$, $C_L = 30pF$	750		ns
			$R_S = 20\Omega$, $C_L = 1nF$	750		
Total Harmonic Distortion	THD	$V_{OUT} = 10V_{P-P}$, $R_S = 20\Omega$, $C_L = 1nF$, $AV = +1V/V$	$f = 1kHz$	145		dB
			$f = 10kHz$	130		
			$f = 100kHz$	-100		
Crosstalk		$V_{OUT} = 10V_{P-P}$, $R_S = 20\Omega$, $C_L = 1nF$	$f = 1kHz$	-100		dB
			$f = 10kHz$	-90		
Input Voltage Noise Density	e _n	$f = 100Hz$		3.5		nV/ \sqrt{Hz}
			$f = 1kHz$	3		
Input Voltage Noise		$0.1Hz \leq f \leq 10Hz$		250		nV _{P-P}
Input Current Noise Density	i _n	$f = 100Hz$		12		pA/ \sqrt{Hz}
			$f = 1kHz$	10		
Capacitive Loading	C _L	No sustained oscillation, $AV = +1V/V$		50		pF

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

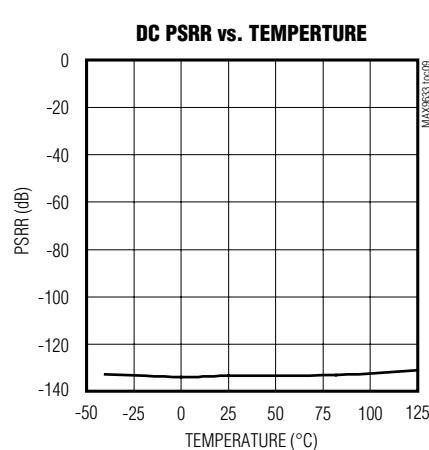
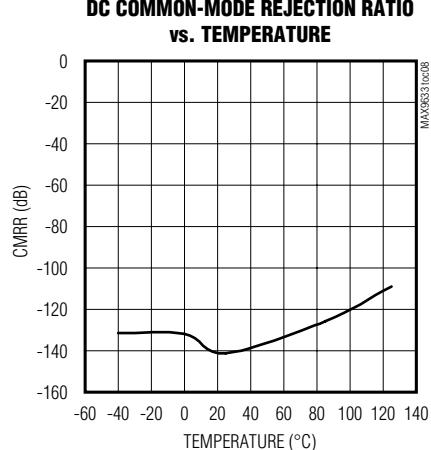
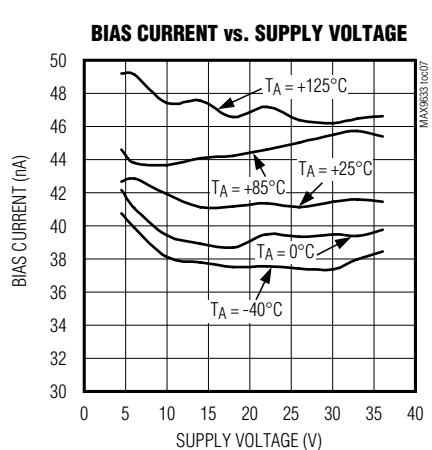
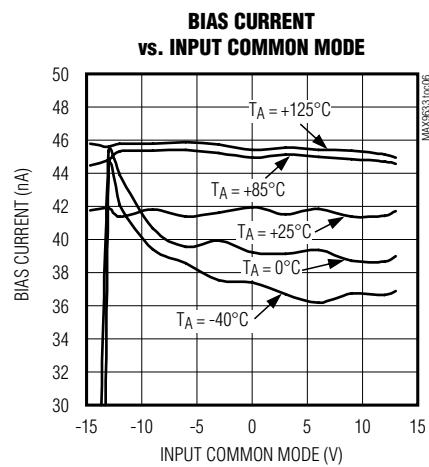
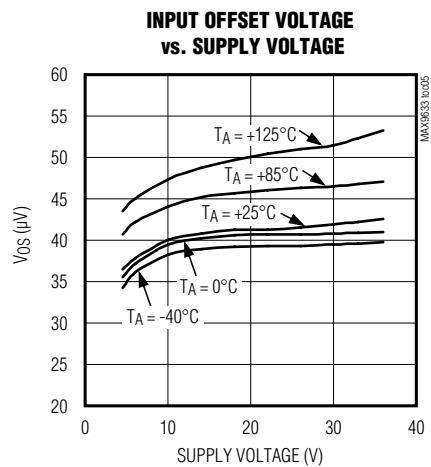
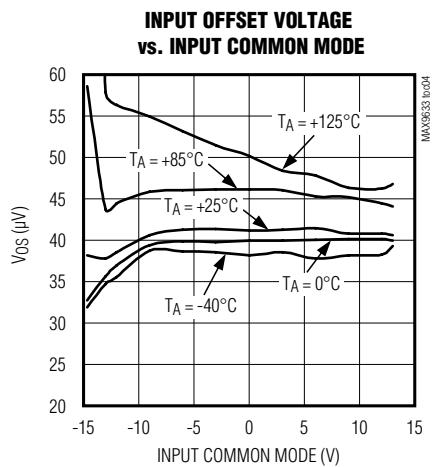
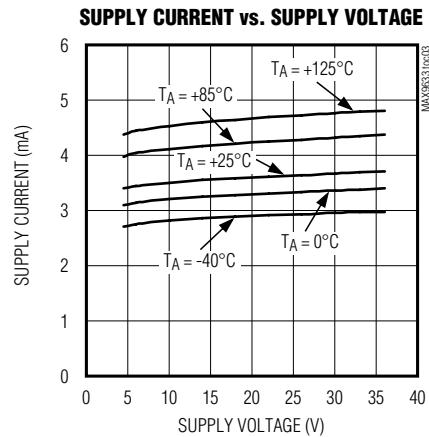
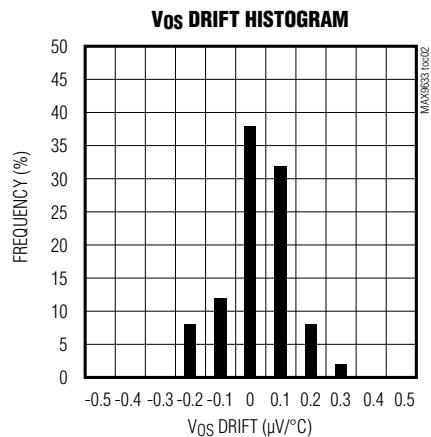
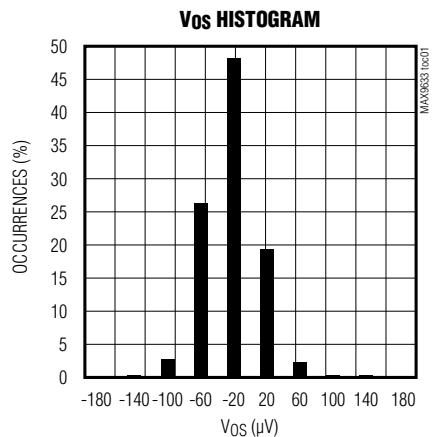
Note 3: Guaranteed by design.

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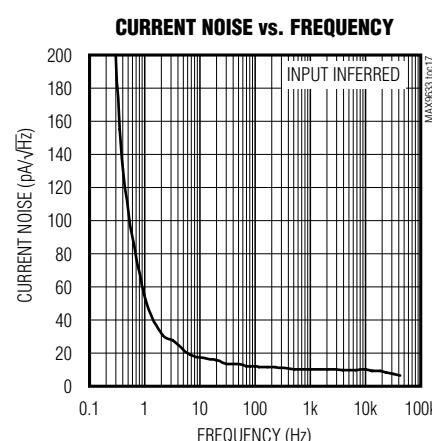
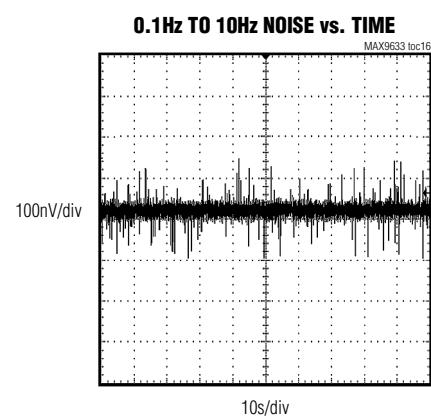
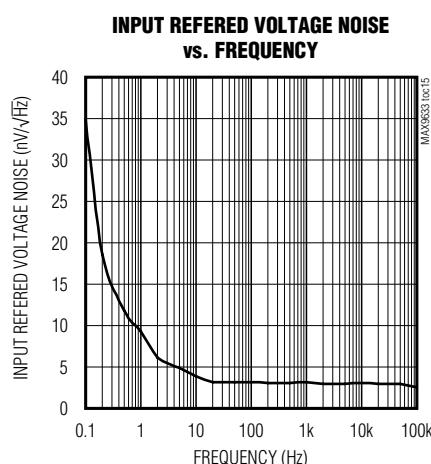
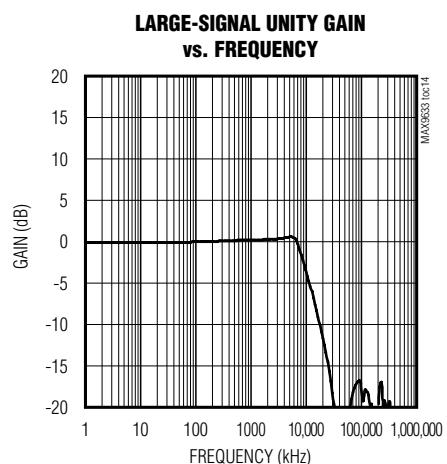
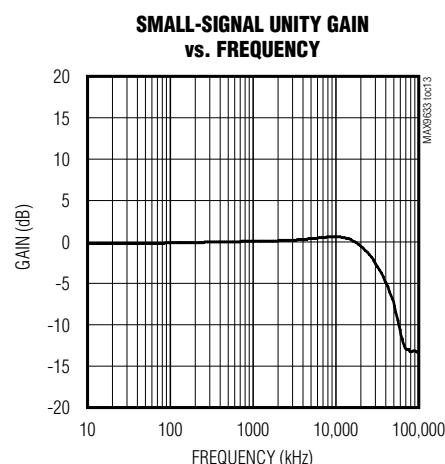
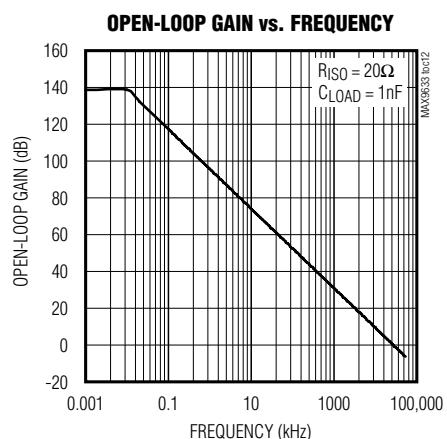
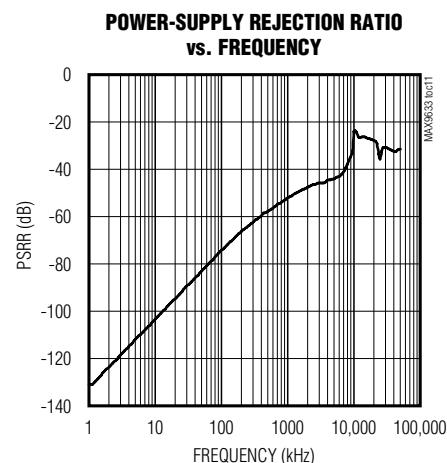
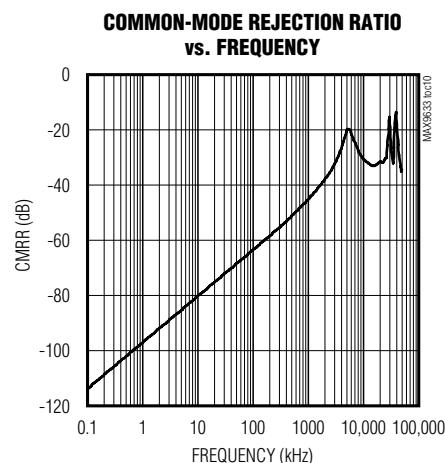
Typical Operating Characteristics

($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, outputs have $R_L = 10k\Omega$ connected to $V_{GND} = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



Dual 36V Op Amp for 18-Bit SAR ADC Front-End**Typical Operating Characteristics (continued)**

($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, outputs have $R_L = 10k\Omega$ connected to $V_{GND} = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



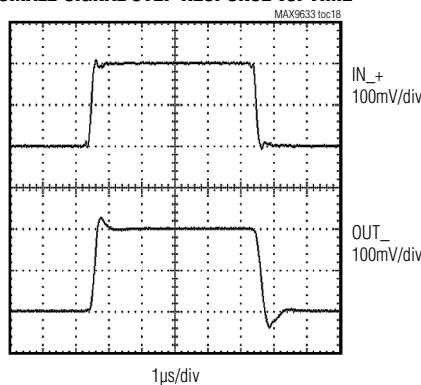
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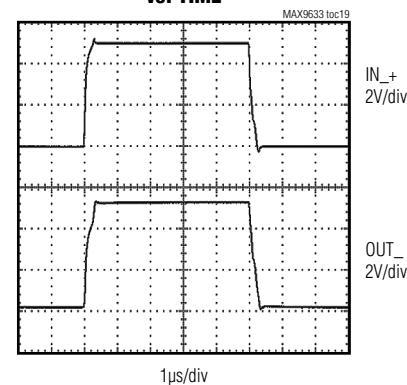
Typical Operating Characteristics (continued)

($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, outputs have $R_L = 10k\Omega$ connected to $V_{GND} = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

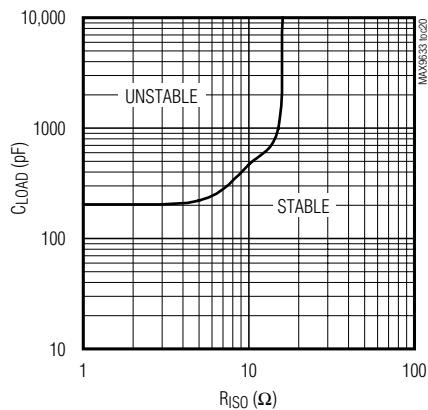
SMALL-SIGNAL STEP RESPONSE vs. TIME



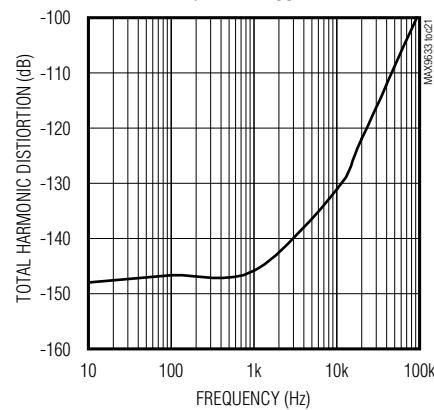
LARGE-SIGNAL STEP RESPONSE vs. TIME



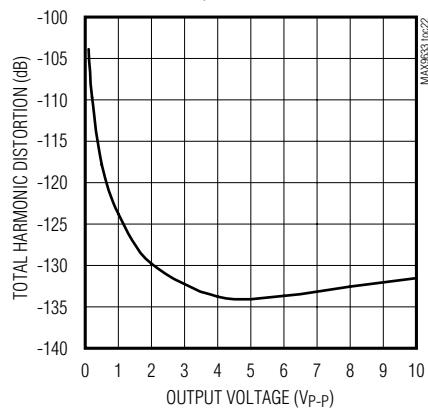
CAPACITIVE LOAD vs. ISOLATION RESISTOR



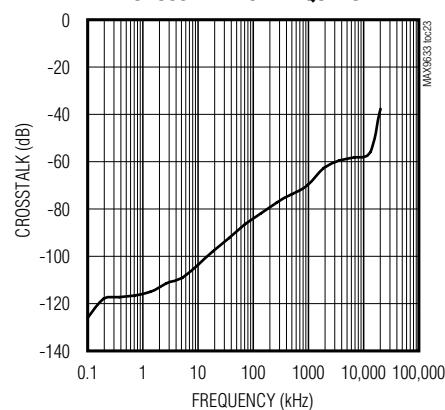
TOTAL HARMONIC DISTORTION vs. FREQUENCY $V_{OUT} = 10V_{P-P}$



THD vs. OUTPUT VOLTAGE FREQUENCY = 10kHz



CROSSTALK vs. FREQUENCY

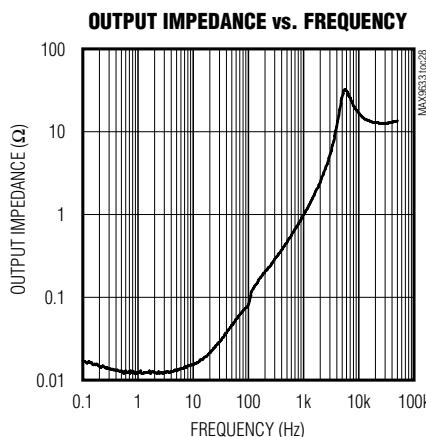
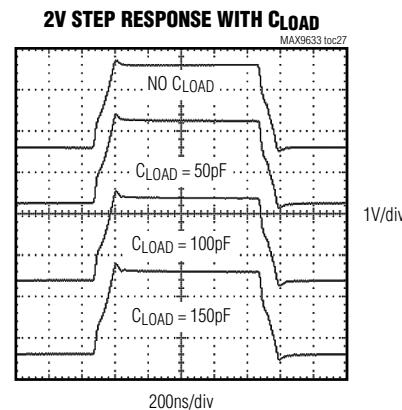
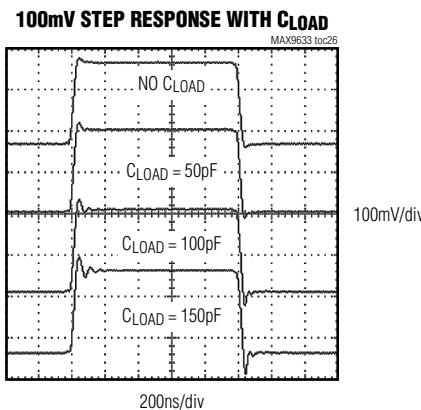
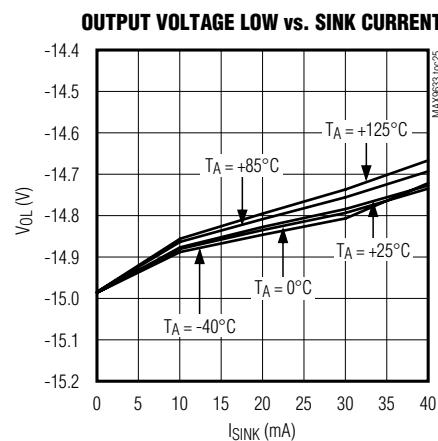
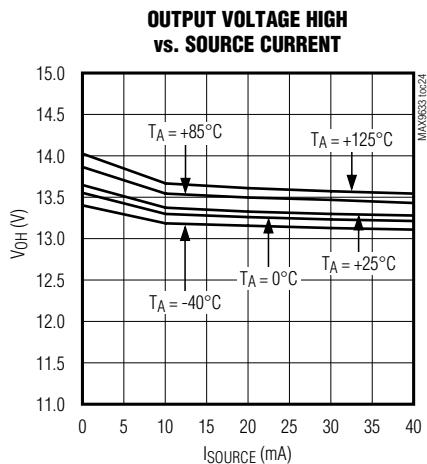


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Typical Operating Characteristics (continued)

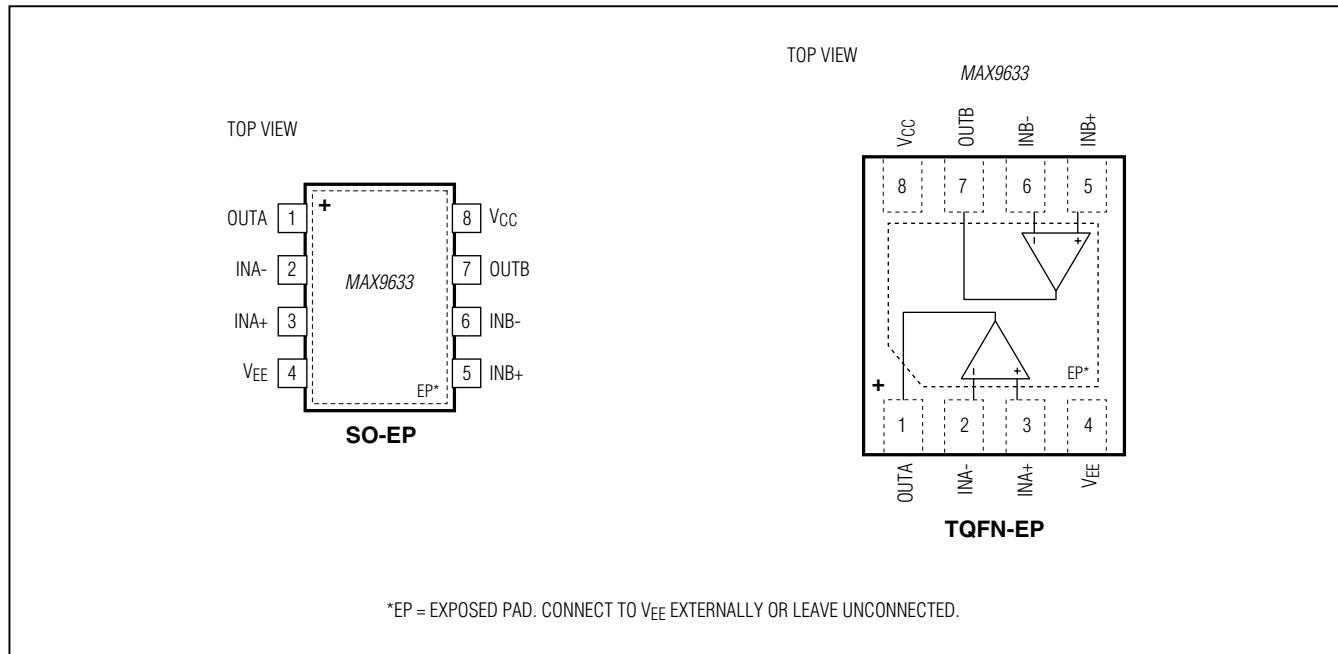
($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, outputs have $R_L = 10k\Omega$ connected to $V_{GND} = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	OUTA	Output A
2	INA-	Negative Input A
3	INA+	Positive Input A
4	VEE	Negative Supply Voltage. Bypass with a 0.1 μ F capacitor to ground.
5	INB+	Positive Input B
6	INB-	Negative Input B
7	OUTB	Output B
8	VCC	Positive Supply Voltage. Bypass with a 0.1 μ F capacitor to ground.
—	EP	Exposed Pad. Connect to VEE externally or leave unconnected.

Dual 36V Op Amp for 18-Bit SAR ADC Front-End

Detailed Description

The MAX9633 is designed in a new 36V, high-speed complementary BiCMOS process that is optimized for excellent AC dynamic performance combined with high-voltage operation.

The exceptionally fast settling time, low noise, low distortion, high bandwidth, and low input offset voltage make the IC an excellent solution to drive (up to 18-bit) high-resolution and fast SAR ADCs.

The MAX9633 is unity gain stable and operates either with a single supply voltage up to 36V or with dual supplies up to $\pm 18V$.

Applications Information

Driving High-Resolution SAR ADCs

High-resolution SAR ADCs typically switch an input capacitor in the order of tens of pF during the track and hold phases. Such capacitor switching can cause a voltage glitch at the input of the ADC that behaves as a load-transient condition for the driving amplifier. In many applications, this glitch is avoided by placing an external capacitor at the ADC input that is in the order of 20 to 50 times the ADC input capacitor. If the ADC input capacitor ranges from 15pF to 30pF, then the external capacitor is anything between 300pF to 1.5nF, depending on the application. An isolation resistor can be placed in series between the amplifier's output and the external capacitor, as shown in the *Typical Application Circuit*.

During the load-transient condition described, the driving amplifier must be able to settle to $0.5 \times \text{LSB}$ within the ADC acquisition time (t_{ACQ}). Assuming a first order approximation, the number of time constants required to settle to $0.5 \times \text{LSB}$ is a logarithm function of the number N of bits:

$$1) \quad k = \ln(2^{N+1})$$

The external RC time constant must be such that:

$$2) \quad k \times R_L \times C < t_{\text{ACQ}}$$

As an example, consider a 16-bit SAR ADC with 500ns acquisition time and 20pF input capacitor.

From 1): $k = 12$

Assuming a factor of 50 for the external capacitor:

$$C = 1\text{nF}$$

Finally, formula 2) gives: $R_L \leq 40\Omega$

The IC is optimized for very fast load-transient recovery with big capacitive loads and small isolation resistors.

This makes it ideal to drive high-resolution and fast SAR ADCs.

Recommended SAR ADCs

The MAX9633's wide supply range and fast settling make it ideal for driving high-resolution SAR ADCs, such as the MAX1320. The MAX1320 is a 14-bit, 8-channel, simultaneous-sampling ADC that measures analog inputs up to $\pm 5V$. Sampling up to 250ksps per channel for eight channels, the MAX1320 achieves 77dB SNR, 90dBc SFDR, and -86dB THD. The MAX1320's fast sample rate and typical input resistance of $8.6k\Omega$ often make it necessary to have a low-noise op amp, such as the MAX9633, driving its inputs. The MAX9633 is also a good fit for an anti-aliasing active filter prior to the MAX1320 as shown in the *Typical Application Circuit*.

The MAX1320 is part of a family of simultaneous sampling ADCs (MAX1316–MAX1326). Other options include ADCs that measure 0V to 5V inputs, or $\pm 10V$ inputs, and two 4 or 8 simultaneous input channels. The MAX1320's high speed and resolution make it a fit for multiphase motor control and power-grid monitoring.

The MAX9633 is also well-suited to drive the 16-bit MAX11046 8-channel, simultaneous-sampling, SAR ADC. The MAX11046 is rated for up to 250ksps. An input driver is typically not necessary at sampling rates below 100ksps. For applications that require $> 100\text{ksps}$ sample rates, the MAX9633 offers small size, high bandwidth, and ultra-low -100dB THD at 100kHz.

Low Noise and Low Distortion

The MAX9633 is designed for applications that require very low voltage noise, making it ideal for low source impedance. When driving 16-bit SAR ADCs with a $\pm 5V$ full-scale input, such as the MAX11046, the MAX9633 very low input voltage noise density specification guarantees 16-bit resolution up to 10MHz of signal bandwidth.

The MAX9633 is also designed for ultra-low distortion performance. THD specifications in the *Electrical Characteristics* and *Typical Operating Characteristics* is calculated up to the 5th harmonic. Even when driving high voltage swing up to 10Vp-P, the MAX9633 maintains excellent low distortion operation up and beyond 100kHz of bandwidth.

Besides driving high-resolution and high-bandwidth SAR ADCs, applications that benefit for low-noise and low-distortion applications can be found in industrial power-grid and smart-grid, industrial motor-control, medical imaging, automated test equipment, instrumentation, and professional audio equipment.

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Input Common Mode and Output Swing

The IC's input common-mode range as well as the output range can swing to the negative rail VEE. These two features are very important for applications where the MAX9633 is used with a single supply (VEE connected to ground). In such a case, being able to swing the input common-mode to the negative rail offers ground-sensing capability.

Input Differential Voltage Protection

During normal op-amp operation, the inverting and non-inverting inputs of the IC are at essentially the same voltage. However, either due to fast input voltage transients or due to other fault conditions, these pins can be forced to be at two different voltages.

Internal back-to-back diodes protect the inputs from an excessive differential voltage (Figure 1). Therefore, IN+ and IN- can be any voltage within the range shown in the *Absolute Maximum Ratings*. Note the protection time is still dependent on the package thermal limits.

If the input signal is fast enough to create the internal diode's forward bias condition (0.7), the input signal current must be limited to 20mA or less. If the input signal current is not inherently limited, an external input series resistor can be used to limit the signal input current. Care should be taken in choosing the input series resistor value, since it degrades the low-noise performance of the device.

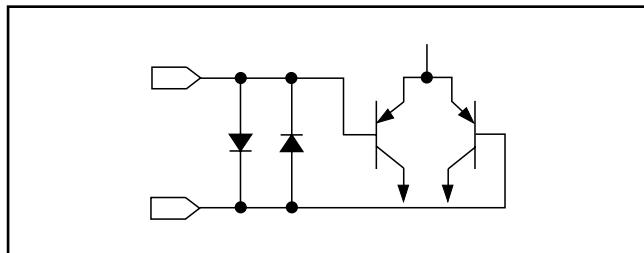


Figure 1. Input Protection Circuit

Electrostatic Discharge (ESD)

The IC has built-in circuits to protect from electrostatic discharge (ESD) events. An ESD event produces a short, high-voltage pulse that is transformed into a short current pulse once it discharges through the device. The built-in protection circuit provides a current path around the op amp that prevents it from being damaged. The energy absorbed by the protection circuit is dissipated as heat. ESD protection is guaranteed up to 5kV with the Human Body Model (HBM).

The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive device. A common example of this phenomenon is when a person accumulates static charge by walking across a carpet and then transfers all of the charge to an ESD-sensitive device by touching it.

Power Supplies and Layout

The IC can operate with dual supplies from $\pm 2.25V$ to $\pm 18V$ or with a single supply from $+4.5V$ to $+36V$ with respect to ground. When used with dual supplies, bypass both VCC and VEE with their own $0.1\mu F$ capacitor to ground. When used with a single supply, bypass VCC with a $0.1\mu F$ capacitor to ground. Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

For high-frequency designs, ground vias are critical to provide a ground return path for high-frequency signals and should be placed around the signal traces and near the decoupling capacitors. Signal routing should be short and direct to avoid parasitic effects. Avoid using right angle connectors since they may introduce a capacitive discontinuity and ultimately limit the frequency response.

Chip Information

PROCESS: BiCMOS

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Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO-EP	S8E+14	21-0111	90-0151
8 TDFN-EP	T833+3	21-0137	90-0060

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	1/11	Added SO-EP package	1, 2, 8, 11
2	5/14	Corrected Package Information	11
3	8/14	Corrected ESD Protection in Features and <i>Electrostatic Discharge (ESD)</i> sections	1, 10



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