TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM3455

30V P-Channel MOSFET

SOT-26

Pin Definition:
1. Drain 6. Drain
2. Drain 5, Drain
3. Gate 4. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-30	100 @ V_{GS} = -10V	-3.5
	170 @ V_{GS} = -4.5V	-2.7

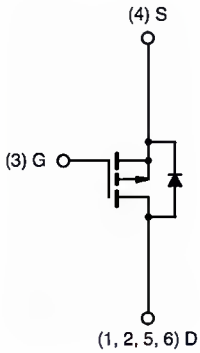
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM3455CX6 RF	SOT-26	3Kpcs / 7" Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	-3.5	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-1.7	A
Maximum Power Dissipation	Ta = 25°C	P_D	2.0	W
	Ta = 75°C		1.3	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JF}$	62.5	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	110	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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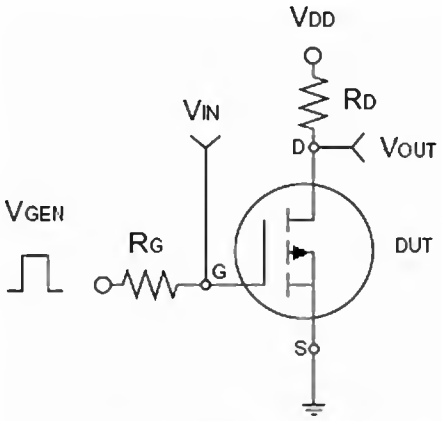
30V P-Channel MOSFET

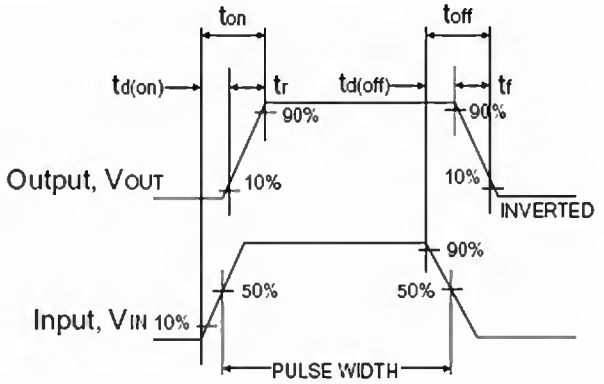
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250uA	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-1	--	-3	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -30V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	μA
On-State Drain Current[a]	V_{DS} ≤-5V, V_{GS} = -10V	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance[a]	V_{GS} = -10V, I_D = -3.5A	$R_{DS(ON)}$	--	80	100	mΩ
	V_{GS} = -4.5V, I_D = -2.7A		--	140	170	
Forward Transconductance[a]	V_{DS} = -15V, I_D = -3.5A	g_{fs}	--	6	--	S
Diode Forward Voltage	I_S = -1.7A, V_{GS} = 0V	V_{SD}	--	--	-1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = -15V, I_D = -3.5A, V_{GS} = -10V	Q_g	--	10	15	nC
Gate-Source Charge		Q_{gs}	--	1.9	--	
Gate-Drain Charge		Q_{gd}	--	2	--	
Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	565	--	pF
Output Capacitance		C_{oss}	--	126	--	
Reverse Transfer Capacitance		C_{rss}	--	75	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = -15V, R_L = 15Ω, I_D = -1A, V_{GEN} = -10V, R_G = 6Ω	$t_{d(on)}$	--	10	20	nS
Turn-On Rise Time		t_r	--	9	20	
Turn-Off Delay Time		$t_{d(off)}$	--	27	50	
Turn-Off Fall Time		t_f	--	7	16	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.

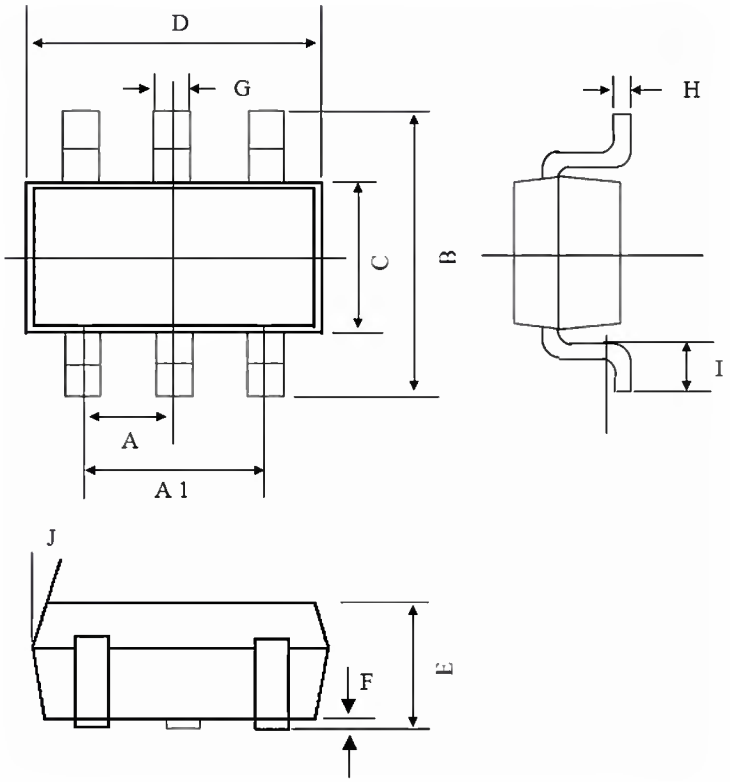


Switching Test Circuit



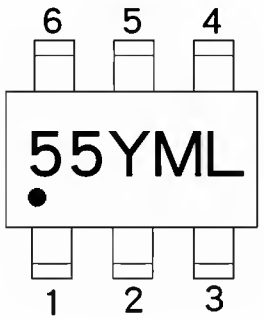
Switchin Waveforms

SOT-26 Mechanical Drawing



SOT-26 DIMENSION						
DIM	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.95 BSC			0.0374 BSC		
A1	1.9 BSC			0.0748 BSC		
B	2.60	2.80	3.00	0.1024	0.1102	0.1181
C	1.40	1.50	1.70	0.0551	0.0591	0.0669
D	2.80	2.90	3.10	0.1101	0.1142	0.1220
E	1.00	1.10	1.20	0.0394	0.0433	0.0472
F	0.00	--	0.10	0.00		0.0039
G	0.35	0.40	0.50	0.0138	0.0157	0.0197
H	0.10	0.15	0.20	0.0039	0.0059	0.0079
I	0.30	--	0.60	0.0118	--	0.0236
J	5°	--	10°	5°	--	10°

Marking Diagram



55 = Device Code
Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

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