

3:1 Active Switch for HDMI™ Signals with Optimized Equalization for Enhanced Signal Integrity

Features

- Supply voltage, $V_{DD} = 3.3V \pm 5\%$
- Each of the three input ports can support HDMI™ or DVI signals
- Supports both AC-coupled and DC-coupled inputs
- Supports DeepColor™
- High Performance, up to 2.5 Gbps per channel
- Switching support for 3 side band signals (SCL, SDA and HPD)
- 5V Tolerance on all side band signals
- SCL, SDA, and HPD pins are the only pins that can support HOT INSERTION
- Integrated 50-ohm ($\pm 10\%$) termination resistors at each high speed signal input
- TMDS input termination control on all high speed inputs
- HDCP reset circuitry for quick communication when switching from one port to another
- Configurable output swing control
- Configurable Pre-Emphasis levels
- Configurable De-Emphasis
- Optimized Equalization
Single default setting will support all cable lengths
- 8kV Contact ESD protection on all input data/clock channels per IEC61000-4-2
- Propagation delay $\leq 2\text{ns}$
- High Impedance Outputs when disabled
- Packaging (Pb-free & Green):
 - 80-pin LQFP (FF80)
 - 64-pin TQFN (ZL64)

Description

Pericom Semiconductor's PI3HDMI301 3:1 active switch circuit is targeted for high-resolution video networks that are based on DVI/HDMI™ standards and TMDS signal processing. The PI3HDMI301 is an active 3 TMDS to 1 TMDS receiver switch with Hi-Z outputs. The device receives differential signals from selected video components and drives the video display unit. It provides controllable output swings, as well as provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

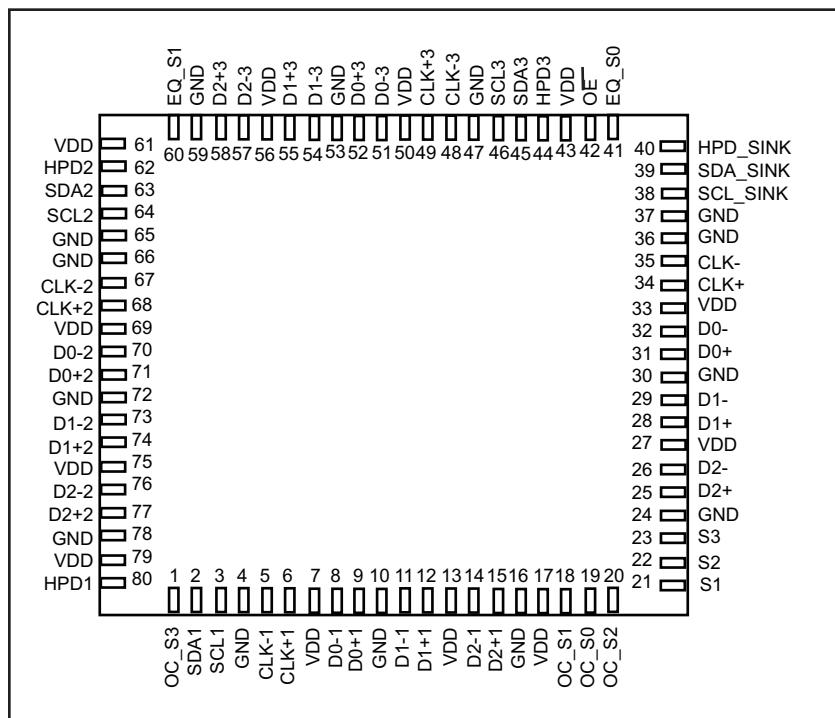
Each complete HDMI/DVI channel also has slower speed, side band signals, that are required to be switched. Pericom's solution provides a complete solution by integrating the side band switch together with the high speed switch in a single solution. Using Equalization at the input of each of the high speed channels, Pericom can successfully eliminate deterministic jitter caused by long cables from the source to the sink. The elimination of the deterministic jitter allows the user to use much longer cables (up to 25 meters).

The maximum DVI/HDMI Bandwidth of 2.5 Gbps provides 36-bit Deep Color™ support, which is offered by HDMI™ revision 1.3. Due to its active uni-directional feature, this switch is designed for usage only for the video receiver's side. For consumer video networks, the device sits at the receiver's side to switch between multiple video components, such as PC, DVD, STB, D-VHS, etc. The PI3HDMI301 also provides enhanced robust ESD/EOS protection of 8kV, which is required by many consumer video networks today.

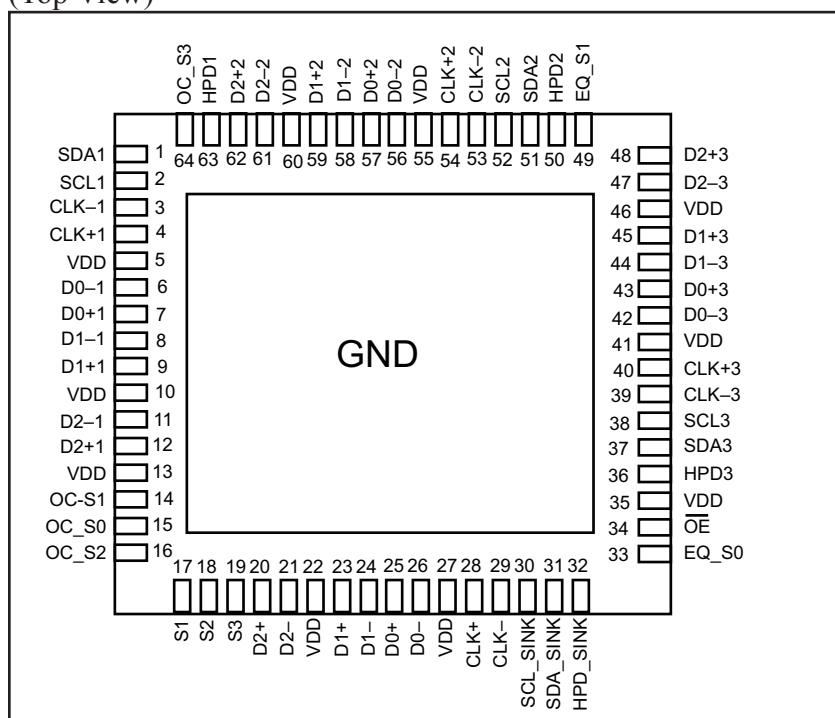
The Optimized Equalization provides the user a single optimal setting that can provide passing results for HDMI jitter tests for all cable lengths: 1meter to 20meters with DeepColor support up to 36bits.

Pericom also offers the ability to fine tune the equalization settings in situations where cable length is known. For example, if 25meter cable length is required, Pericom's solution can be adjusted to 16dB EQ to accept 25meter cable length.

Pin Configuration (Top View)

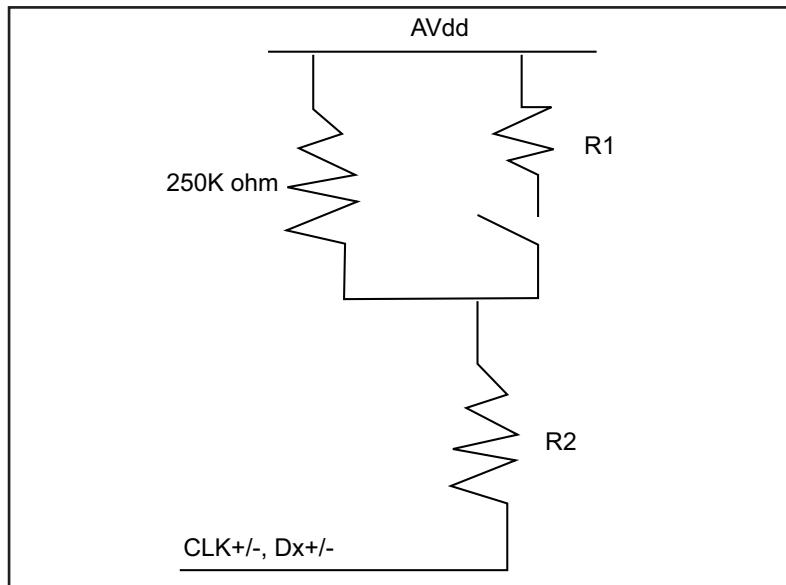


(Top View)



Receiver Block¹

Each input has integrated equalization that can eliminate deterministic jitter caused by 25meter 24AWG cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, 1 HPD signals, and DDC signals. TMDS Channels have following termination scheme for Rx Sense support.

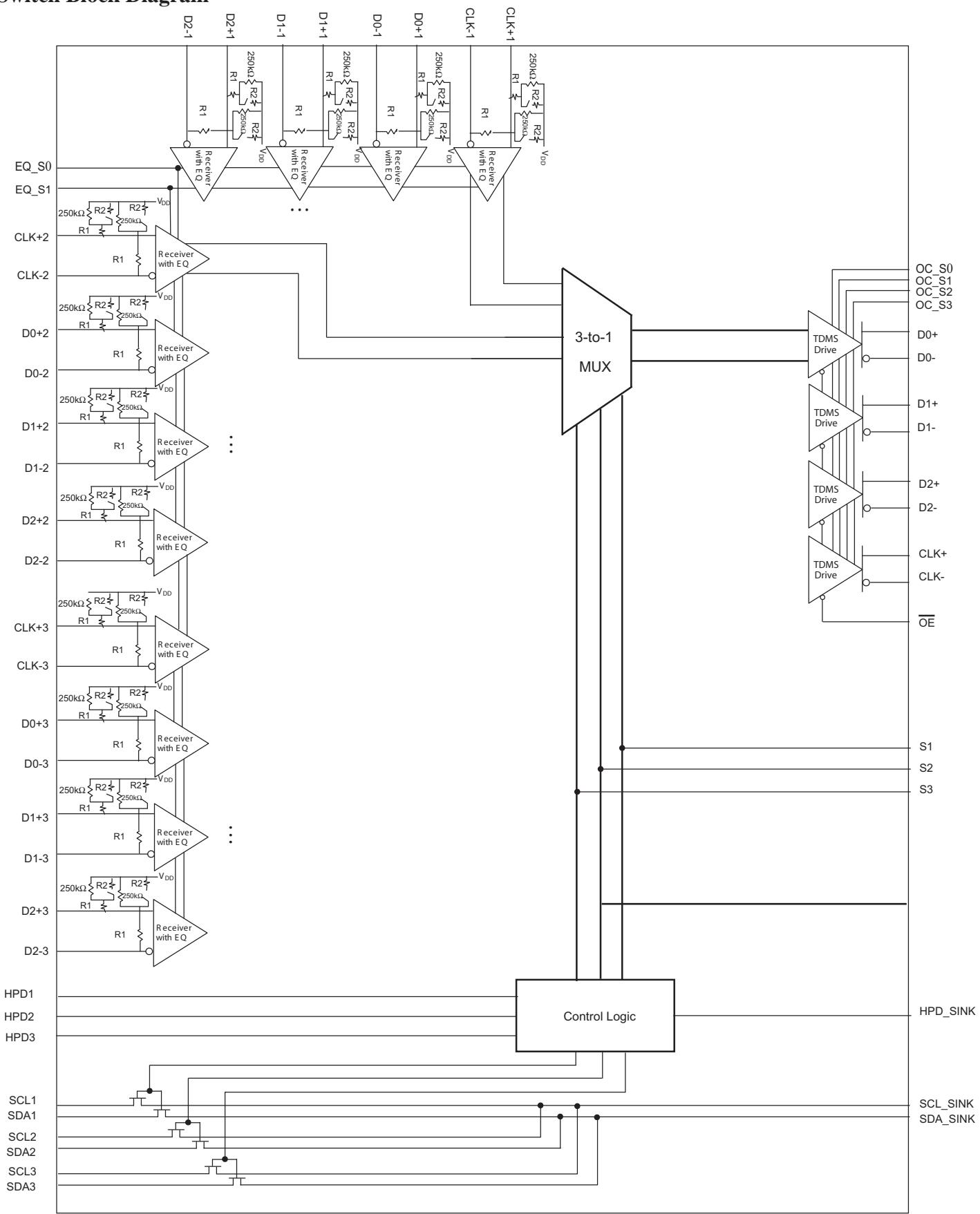


Note:

1. $R_1 + R_2 = 50 \Omega$

Pin Description

80 LQFP Pin #	64 TQFN Pin #	Pin Name	I/O	Description
9, 12, 15, 6	7, 9, 12, 4	D ₀ +1, D ₁ +1, D ₂ +1, CLK+1	I	Port 1 TMDS Positive inputs
71, 74, 77, 68	57, 59, 62, 54	D ₀ +2, D ₁ +2, D ₂ +2, CLK+2	I	Port 2 TMDS Positive inputs
52, 55, 58, 49	43, 45, 48, 40	D ₀ +3, D ₁ +3, D ₂ +3, CLK+3	I	Port 3 TMDS Positive inputs
8, 11, 14, 5	6, 8, 11, 3	D ₀ -1, D ₁ -1, D ₂ -1, CLK-1	I	Port 1 TMDS Negative inputs
70, 73, 76, 67	56, 58, 61, 53	D ₀ -2, D ₁ -2, D ₂ -2, CLK-2	I	Port 2 TMDS Negative inputs
51, 54, 57, 48	42, 44, 47, 39	D ₀ -3, D ₁ -3, D ₂ -3, CLK-3	I	Port 3 TMDS Negative inputs
4, 10, 16, 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78		GND		Ground
80	63	HPD1	O	Port 1 HPD output
62	50	HPD2	O	Port 2 HPD output
44	36	HPD3	O	Port 3 HPD output
40	32	HPD_Sink	I	Sink side hot plug detector input. High: 5-V power signal asserted from source to sink and EDID is ready. Low: No 5-V power signal asserted from source to sink, or EDID is not ready.
42	34	OE	I	Output Enable, Active LOW
3	2	SCL1	I/O	Port 1 DDC Clock
64	52	SCL2	I/O	Port 2 DDC Clock
46	38	SCL3	I/O	Port 3 DDC Clock
38	31	SCL_Sink	I/O	Sink Side DDC Clock
2	1	SDA1	I/O	Port 1 DDC Data
63	51	SDA2	I/O	Port 2 DDC Data
45	37	SDA3	I/O	Port 3 DDC Data
39	31	SDA_Sink	I/O	Sink Side DDC Data
21, 22, 23	17, 18, 19	S1, S2, S3	I	Source Input Control
7, 13, 17, 27, 33, 43, 50, 56, 61, 69, 75, 79	5, 10, 22, 27, 35, 41, 46, 55, 60	V _{DD}		3.3V Power Supply
31, 28, 25, 34	25, 23, 20, 28	D ₀ +, D ₁ +, D ₂ +, CLK+	O	TMDS positive outputs
32, 29, 26, 35	26, 24, 21, 29	D ₀ -, D ₁ -, D ₂ -, CLK-	O	TMDS negative outputs
41, 60	33, 49	EQ_S0, EQ_S1	I	Equalizer controls, both controls have internal pull-ups
19, 18, 20, 1	15, 14, 16, 64	OC_S0, OC_S1, OC_S2, OC_S3	I	Output buffer controls, all control bits have internal pull-ups

Switch Block Diagram


Truth Table

Control Pins				I/O Selected		Hot Plug Detect Status		
\overline{OE}	S1	S2	S3	TMDS outputs	SCL_Sink SDA_Sink	HPD1	HPD2	HPD3
L	H	x	x	Port1	SCL1 SDA1	HPD_Sink	L	L
L	L	H	x	Port2	SCL2 SDA2	L	HPD_Sink	L
L	L	L	H	Port3	SCL3 SDA3	L	L	HPD_Sink
L	L	L	L	None (Hi-Z)	None (Hi-Z)	L	L	L
H	X	X	X	None (Hi-Z)	Follow S1, S2, S3	Follow S1, S2, S3		

OC Setting Value Logic Table

0 Input Control Pins				Setting Value	
OC_S3 ⁽¹⁾	OC_S2 ⁽¹⁾	OC_S1 ⁽¹⁾	OC_S0 ⁽¹⁾	Vswing (mV)	Pre-emphasis/De-emphasis (dB)
0	0	0	0	333	-9.5
0	0	0	1	500	-6
0	0	1	0	666	-3.5
0	0	1	1	1000	0
0	1	0	0	160	-9
0	1	0	1	270	-6
0	1	1	0	340	-3.5
0	1	1	1	500	0
1	0	0	0	500	6
1	0	0	1	500	3.5
1	0	1	0	500	1.5
1	0	1	1	500	0
1	1	0	0	600	0
1	1	0	1	1000	0
1	1	1	0	750	0
1	1	1	1	500	0

EQ Setting Value Logic Table for high speed data bits (TMDS CLK input is left at 3dB default always)

EQ_S1 ⁽¹⁾	EQ_S0 ⁽¹⁾	Setting Value
0	0	15dB on all high speed data inputs
0	1	3dB on all high speed data inputs
1	0	8dB on all high speed data inputs
1	1	Optimized Equalization on all high speed data inputs (Default setting which can support all cable lengths from 1meter to 20meters)

Notes:

1) Integrated internal pull-ups

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential.....	−0.5V to +4.0V
DC Input Voltage	−0.5V to V _{DD}
DC Output Current.....	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{DD}	Supply Voltage	3.135	3.3	3.465	V
T _A	Operating free-air temperature	0		70	°C

TMDS Differential Pins

V _{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V _{IC}	Input common mode voltage	2		V _{DD} + 0.01	V
V _{DD}	TMDS output termination voltage	3.135	3.3	3.465	V
R _T	Termination resistance	45	50	55	ohm
	Signaling rate	0.25		2.5	Gbps

Control Pins (OC_Sx, EQ_Sx, Sx, OE)

V _{IH}	LVTTL High-level input voltage	2		V _{DD}	V
V _{IL}	LVTTL Low-level input voltage	GND		0.8	

DDC Pins (SCLx, SCL_SINK, SDAx, SDA_SINK)

V _{I(DDC)}	Input voltage	GND		5.5	V
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Status Pins (HPD_SINK)

V _{IH}	LVTTL High-level input voltage	2		5.3	V
V _{IL}	LVTTL Low-level input voltage	GND		0.8	

TMDS Compliance Test Results

Item	HDMI™ 1.3 Spec	Pericom Product Spec
Operating Conditions		
Termination Supply Voltage, VDD	$3.3V \leq 5\%$	$3.30 \pm 5\%$
Terminal Resistance	$50\text{-ohm} \pm 10\%$	45 to 55-ohm
Source DC Characteristics at TP1		
Single-ended high level output voltage, VH	$V_{DD} \pm 10\text{mV}$	$V_{DD} \pm 10\text{mV}$
Single-ended low level output voltage, VL	$(V_{DD} - 600\text{mV}) \leq VL \leq (V_{DD} - 400\text{mV})$	$(V_{DD} - 600\text{mV}) \leq VL \leq (V_{DD} - 400\text{mV})$
Single-ended output swing voltage, Vswing	$400\text{mV} \leq V_{swing} \leq 600\text{mV}$	$400\text{mV} \leq V_{swing} \leq 600\text{mV}$
Single-ended standby (off) output voltage, Voff	$V_{DD} \pm 10\text{mV}$	$V_{DD} \pm 10\text{mV}$
Transmitter AC Characteristics at TP1		
Risetime/Falltime (20%-80%)	$75\text{ps} \leq \text{Risetime/Falltime} \leq 0.4 \text{ Tbit}$ ($75\text{ps} \leq tr/tf \leq 242\text{ps}$) @ 1.65 Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65 Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65 Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65 Gbps)	82ps max
Sink Operating DC Characteristics at TP2		
Input Differential Voltage Level, Vdiff	$150 \leq V_{diff} \leq 1200\text{mV}$	$150\text{mV} \leq V_{DIFF} \leq 1200\text{mV}$
Input Common Mode Voltage Level, V _{ICM}	$(V_{DD} - 300\text{mV}) \leq V_{icm} \leq (V_{DD} - 37.5\text{mV})$ Or $V_{DD} \pm 10\%$	$(V_{DD} - 300\text{mV}) \leq V_{icm} \leq (V_{DD} - 37.5\text{mV})$ Or $V_{DD} \pm 10\%$
Sink DC Characteristics When Source Disabled or Disconnected at TP2		
Differential Voltage Level	$V_{DD} \pm 10\text{mV}$	$V_{DD} \pm 10\text{mV}$

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
I _{CC}	Supply Current	V _{IH} = V _{DD} , V _{IL} = V _{DD} - 0.4V, R _T = 50-ohm, V _{DD} = 3.3V Data Input = 1.65 Gbps HDMI™ data pattern CLK Input = 165 MHz clock		200		mA
P _D	Power Dissipation			660		mW
I _{CCQ}	Standby Current	OE = HIGH, S1 = S2 = S3 = LOW		8		mA
TMDS Differential Pins						
V _{OH}	Single-ended high-level output voltage	V _{DD} = 3.3V, R _T = 50-ohm Pre-emphasis/De-emphasis = 0dB	V _{DD} - 10		V _{DD} + 10	mV
V _{OL}	Single-ended low-level output voltage		V _{DD} - 600		V _{DD} - 400	
V _{swing}	Single-ended output swing voltage		400		600	
V _{OD(O)}	Overshoot of output differential voltage			6%	15%	2x V _{swing}
V _{OD(U)}	Undershoot of output differential voltage			12%	25%	
ΔV _{OCS}	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
I _(OS)	Short circuit output current				12	mA
V _{ODE(SS)}	Steady state output differential voltage	OC_Sx = GND, Data Input = 250 Mbps HDMI™ data pattern CLK Input = 25 MHz clock x = 0, 1, 2, 3	560		840	mVp-p
V _{ODE(PP)}	Peak-to-peak output differential voltage		800		1200	
V _{I(open)}	Single-ended input voltage under high impedance input or open input	I _I = 10µA	V _{DD} - 10		V _{DD} + 10	mV
R _{INT}	Input termination resistance	V _{IN} = 2.9V	45	50	55	ohm
DDC I/O Pins (SCLx, SCL_SINK, SDAX, SDA_SINK)						
I _{lk}	Input leakage current	V _I = 5.5V	-50		50	µA
		V _I = V _{DD}	-10		10	
C _{IO}	Input/output capacitance	V _I = 0V		7.5		pF
R _{ON}	Switch resistance	I _O = 3mA, V _O = 0.4V		25	50	ohm
V _{PASS}	Switch output voltage	V _I = 3.3V, I _I = 100µA	1.5 ⁽²⁾	2.0	2.5 ⁽³⁾	V
Status Pins (HPD)						
V _{OH(TTL)}	TTL High-level output voltage	I _{OH} = -4mA	2.4			V
V _{OL(TTL)}	TTL Low-level output voltage	I _{OL} = 4mA			0.4	V

(Table Continued)

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
Control Pins (OC_Sx, EQ_Sx, Sx, \overline{OE})						
I _{IH}	High-level digital input current	V _{IH} = 2.0V or V _{DD}	-10		10	μ A
I _{IL}	Low-level digital input current	V _{IL} = GND or 0.8V	-10		10	
Status Pins (HPD_SINK)						
I _{IH}	High-level digital input current	V _{IH} = 5.3V	-50		50	μ A
		V _{IH} = 2.0V or V _{DD}	-10		10	
I _{IL}	Low-level digital input current	V _{IL} = GND or 0.8V	-10		10	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. The value is tested in full temperature range at 3.0V.
3. The value is tested in full temperature range at 3.6V.

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
TMDS Differential Pins						
tpd	Propagation delay	V _{DD} = 3.3V, R _T = 50-ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t _r	Differential output signal rise time (20% - 80%)		75		140	
t _f	Differential output signal fall time (20% - 80%)		75		140	
t _{sk(p)}	Pulse skew			10	50	
t _{sk(D)}	Intra-pair differential skew			23	50	
t _{sk(o)}	Inter-pair differential skew ⁽²⁾				100	
TCLK _{jit(pp)}	Peak-to-peak output jitter from TMDS CLK channel residual jitter			15	30	
TDATA _{jit(pp)}	Peak-to-peak output jitter from TMDS data residual jitter			18	50	
t _{DE}	De-emphasis duration			240		
t _{sx}	Select to switch output				10	ns
t _{en}	Enable time				200	
t _{dis}	Disable time				10	
DDC I/O Pins (SCLx, SCL_SINK, SDAX, SDA_SINK)						
t _{pd(DDC)}	Propagation delay from SCLn to SCL_SINK or SDAX to SDA_SINK or SDA_SINK to SDAX	C _L = 10pF		0.4	2.5	ns
Control and Status Pins (OC_SX, EQ_SX, Sx, HPD_SINK, HPDx)						
t _{pd(HPD)}	Propagation delay (from HPD_SINK to the active port of HPDx)	C _L = 10pF		2	6.0	ns
t _{sx(HPD)}	Switch time (from port select to the latest valid status of HPDx)			3	6.5	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. t_{sk(o)} is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.

Application Information
Supply Voltage

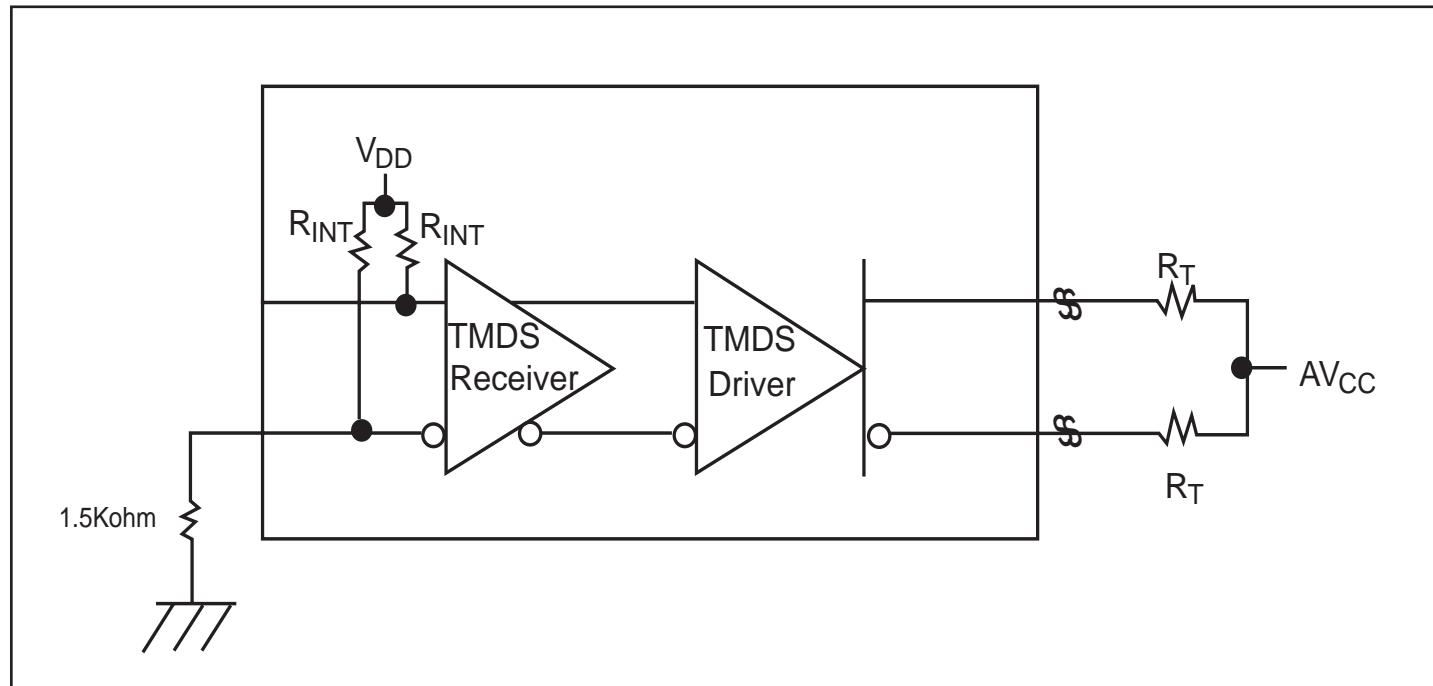
All V_{DD} pins are recommended to have a 0.01μF capacitor tied from V_{DD} to GND to filter supply noise

TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI301 device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. One pin will be pulled high to V_{DD} with the other grounded through a 1.5K-Ohm resistor as shown.



TMDS Input Fail-Safe Recommendation

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put $0.1\mu\text{F}$ decoupling capacitors on each V_{DD} pins of our part, there are four $0.1\mu\text{F}$ decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of $0.1\mu\text{F}$ decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of $0.1\mu\text{F}$ decoupling capacitors on each V_{DD} pins, it is recommended to put a $10\mu\text{F}$ decoupling capacitor near our part's V_{DD} , it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

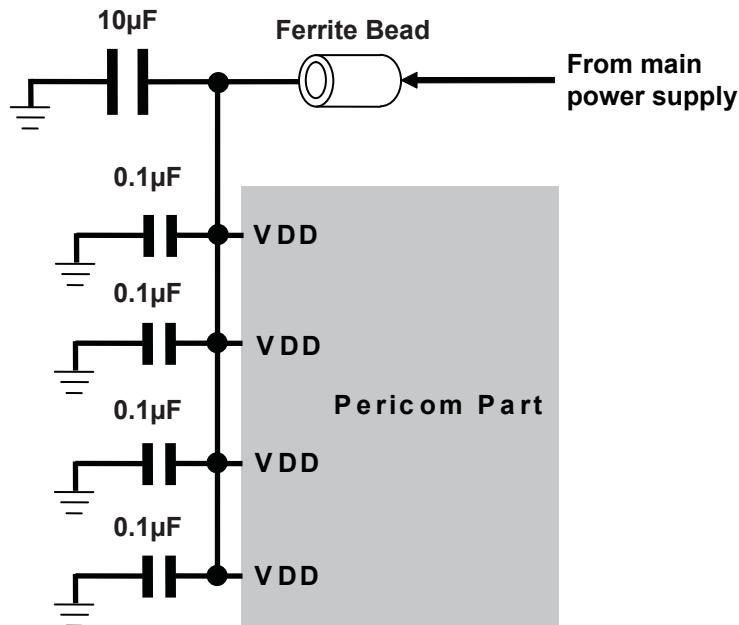


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling Capacitor Placement Consideration

- i. Each $0.1\mu\text{F}$ decoupling capacitor should be placed as close as possible to each VDD pin.
- ii. VDD and GND planes should be used to provide a low impedance path for power and ground.
- iii. Via holes should be placed to connect to VDD and GND planes directly.
- iv. Trace should be as wide as possible
- v. Trace should be as short as possible.
- vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- vii. $10\mu\text{F}$ capacitor should also be placed closed to our part and should be placed in the middle location of $0.1\mu\text{F}$ capacitors.
- viii. Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.

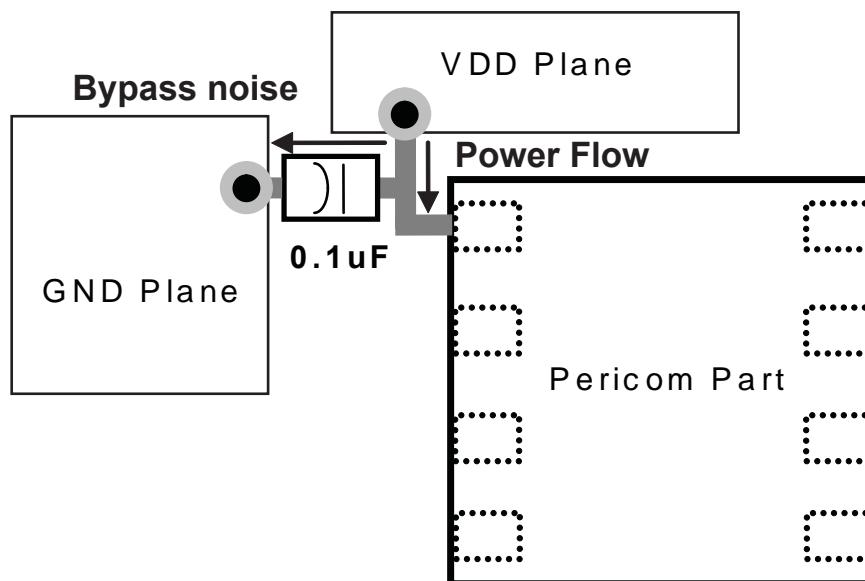
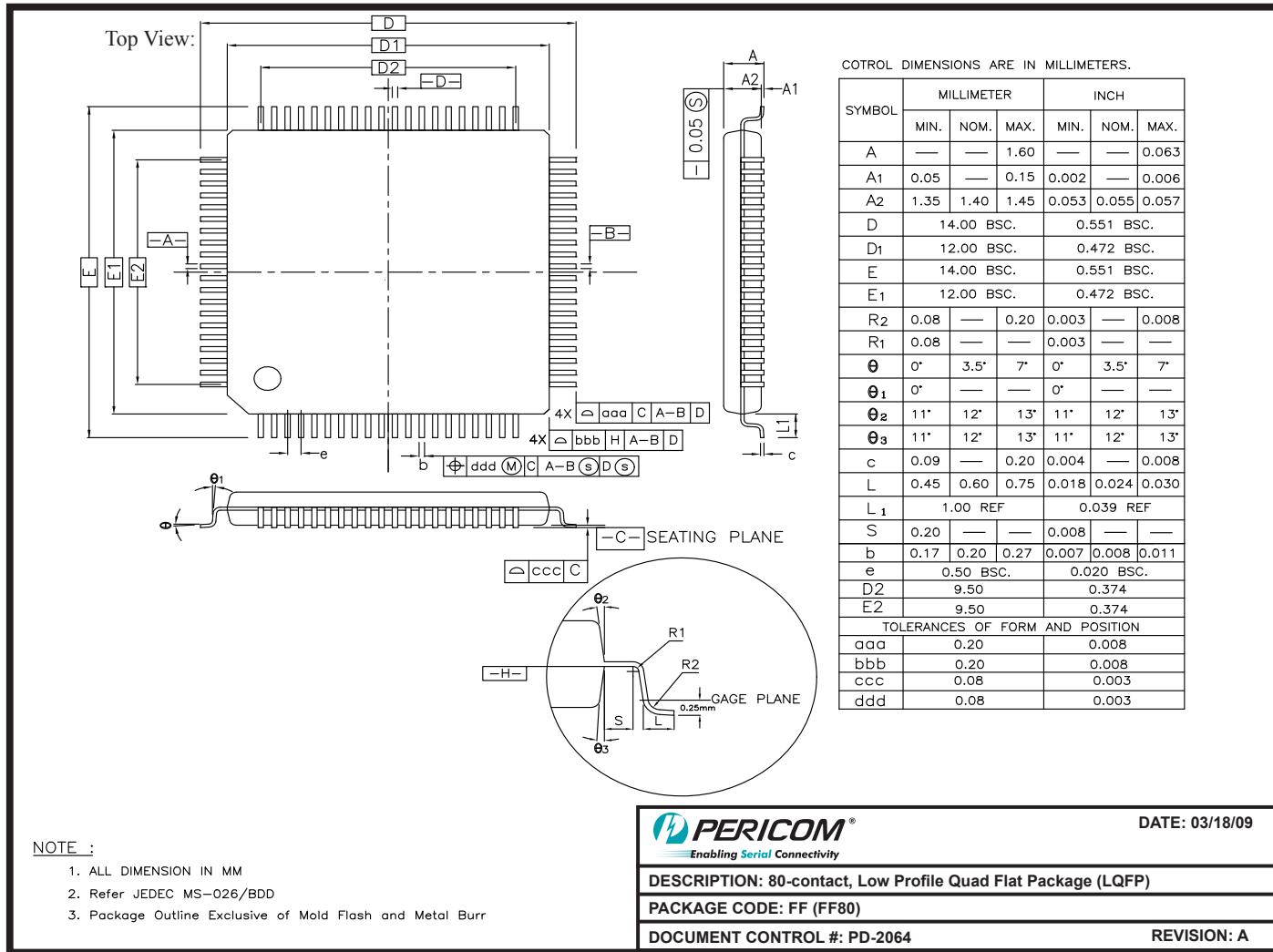


Figure 2 Layout and Decoupling Capacitor Placement Diagram

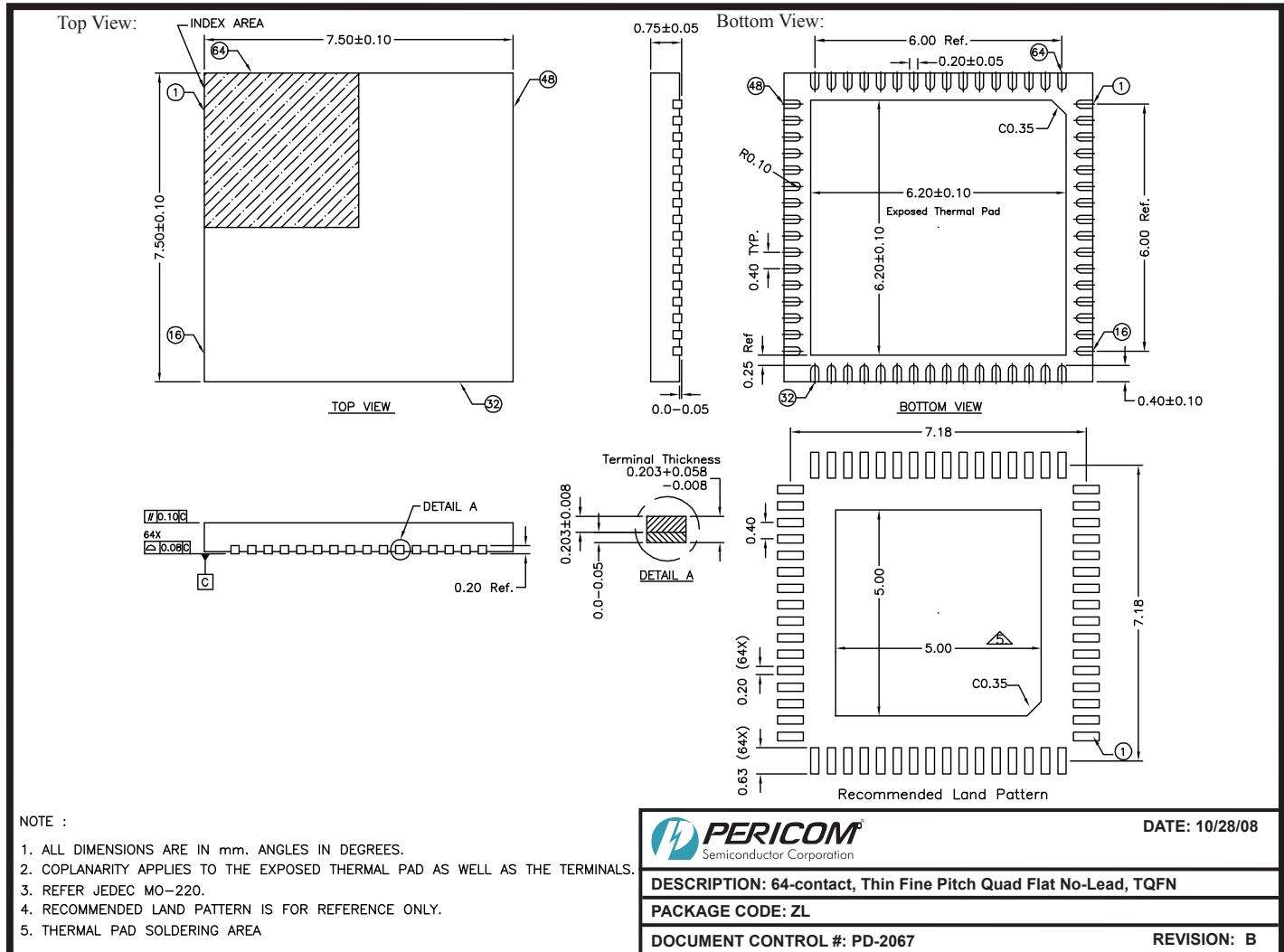
Package Mechanical: 80-pin, Low Profile Quad Flat Package (FF80)



07-0100

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Package Mechanical: 64-pin, Quad Flat Package (ZL64)


08-0530

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI301FFE	FF	80-pin, Pb-free & Green LQFP
PI3HDMI301ZLE	ZL	64-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel