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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM62W8512B Series

4 M SRAM (512-kword $\times$ 8-bit)



ADE-203-904F (Z)

Rev. 5.0

Mar. 15, 2000

Description

The Hitachi HM62W8512B is a 4-Mbit static RAM organized 512-kword $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 μ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II is available for high density mounting. The HM62W8512B is suitable for battery backup system.

Features

- Single 3.3 V supply: 3.3 V $\pm$ 0.3 V
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 16.5 mW/MHz (typ)
 - Standby: 3.3 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly LV-TTL compatible: All inputs and outputs
- Battery backup operation

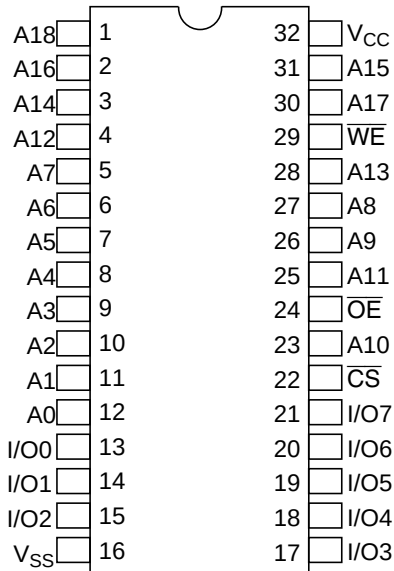
HM62W8512B Series

Ordering Information

Type No.	Access time	Package
HM62W8512BLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W8512BLFP-7	70 ns	
HM62W8512BLFP-5SL	55 ns	
HM62W8512BLFP-7SL	70 ns	
HM62W8512BLFP-5UL	55 ns	
HM62W8512BLFP-7UL	70 ns	
HM62W8512BLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM62W8512BLTT-7	70 ns	
HM62W8512BLTT-5SL	55 ns	
HM62W8512BLTT-7SL	70 ns	
HM62W8512BLTT-5UL	55 ns	
HM62W8512BLTT-7UL	70 ns	
HM62W8512BLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM62W8512BLRR-7	70 ns	
HM62W8512BLRR-5SL	55 ns	
HM62W8512BLRR-7SL	70 ns	
HM62W8512BLRR-5UL	55 ns	
HM62W8512BLRR-7UL	70 ns	

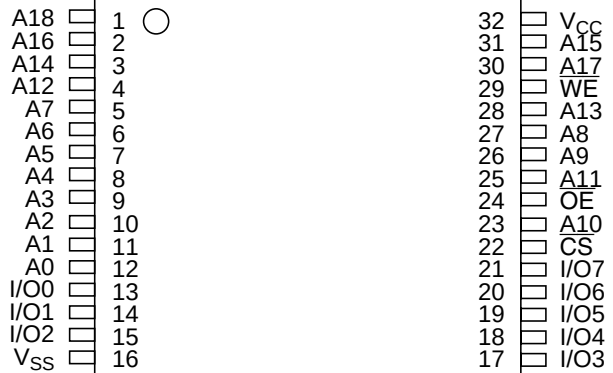
Pin Arrangement

HM62W8512BLFP Series



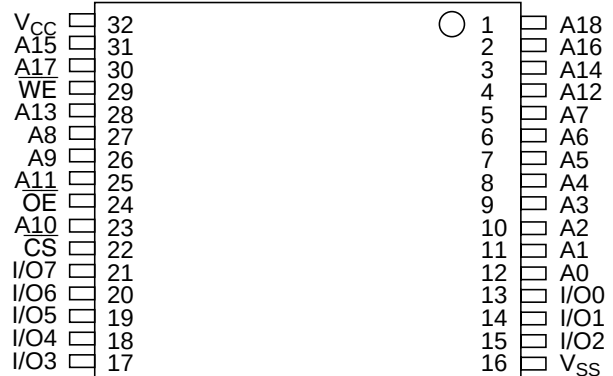
(Top view)

HM62W8512BLTT Series



(Top view)

HM62W8512BLRR Series

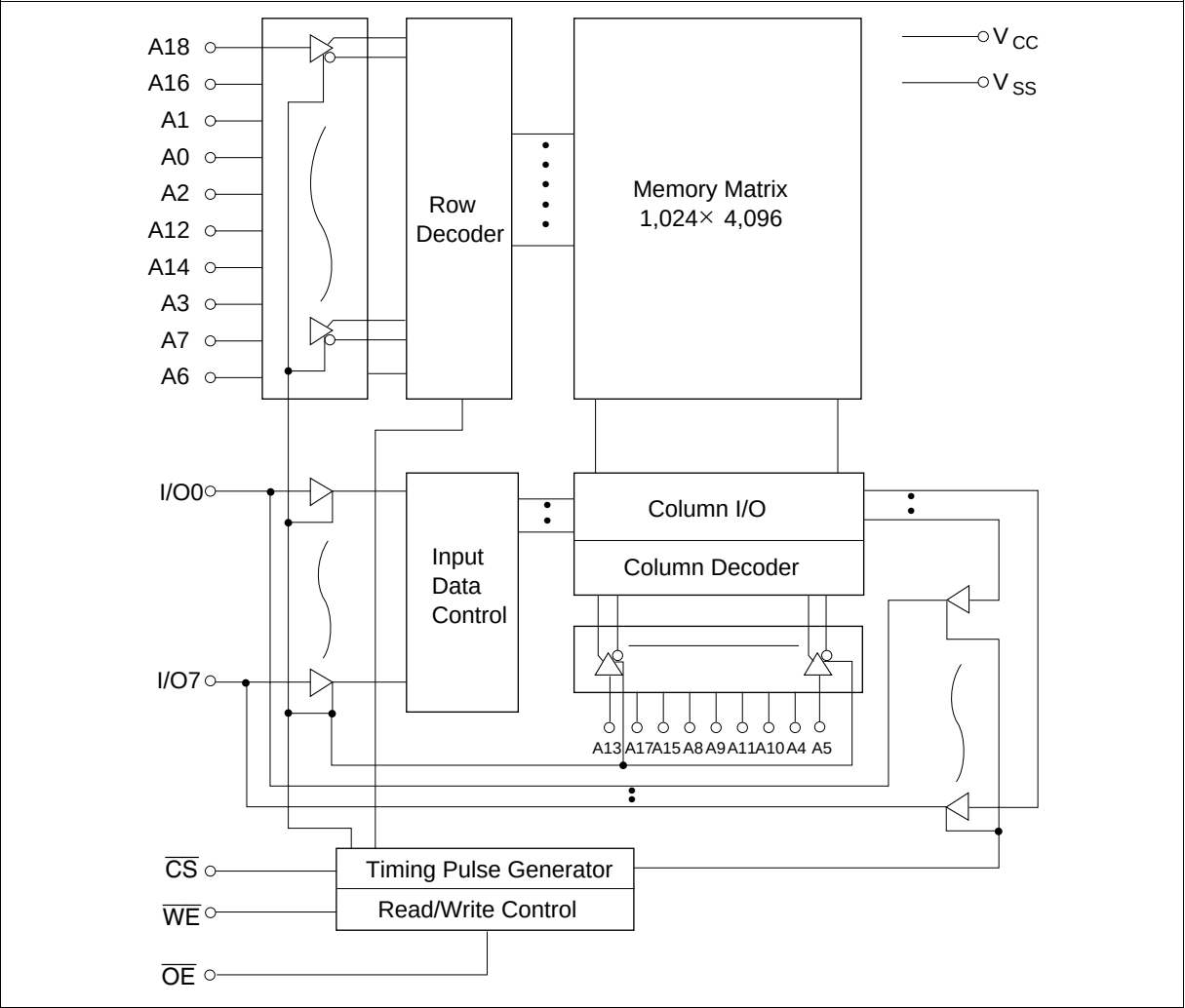


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	−0.5* ¹ to $V_{CC} + 0.5$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	−20 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−20 to +85	°C

Notes: 1. −3.0 V for pulse half-width ≤ 30 ns

2. Maximum voltage is 4.6 V

Recommended DC Operating Conditions ($T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	−0.3* ¹	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

HM62W8512B Series

DC Characteristics (Ta = -20 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{IL}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	—	10	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	HM62W8512B-5 I _{CC1}	—	—	45	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{I/O} = 0 mA
	HM62W8512B-7 I _{CC1}	—	—	40	mA	
Operating power supply current	I _{CC2}	—	5	10	mA	Cycle time = 1 μs, duty = 100% I _{I/O} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	0.1	0.3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I _{SB1}	—	1* ²	40* ²	μA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	1* ³	20* ³	μA	
		—	1* ⁴	5* ⁴	μA	
		—	—	—	—	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.0 mA
		—	—	0.2	V	I _{OL} = 100 μA
Output high voltage	V _{OH}	V _{CC} - 0.2	—	—	V	I _{OH} = -100 μA
		2.4	—	—	V	I _{OH} = -2.0 mA

Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

4. This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

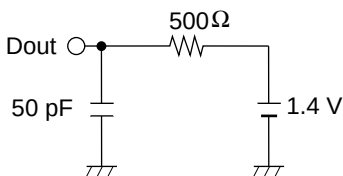
Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -20$ to $+70^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference level: 1.4 V/1.4 V(HM62W8512B-5)
0.8 V/2.0 V(HM62W8512B-7)
- Output load (Including scope & jig)



Read Cycle

HM62W8512B

	-5	-7
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Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{CO}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	30	—	35	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{HZ}	0	20	0	30	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	20	0	30	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

Write Cycle

HM62W8512B

Parameter	Symbol	-5		-7		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	70	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Write pulse width	t_{WP}	40	—	50	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	20	0	30	ns	1, 2, 7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	30	ns	1, 2, 7

Notes: 1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

4. t_{CW} is measured from $\overline{CS}$ going low to the end of write.

5. t_{AS} is measured from the address valid to the beginning of write.

6. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

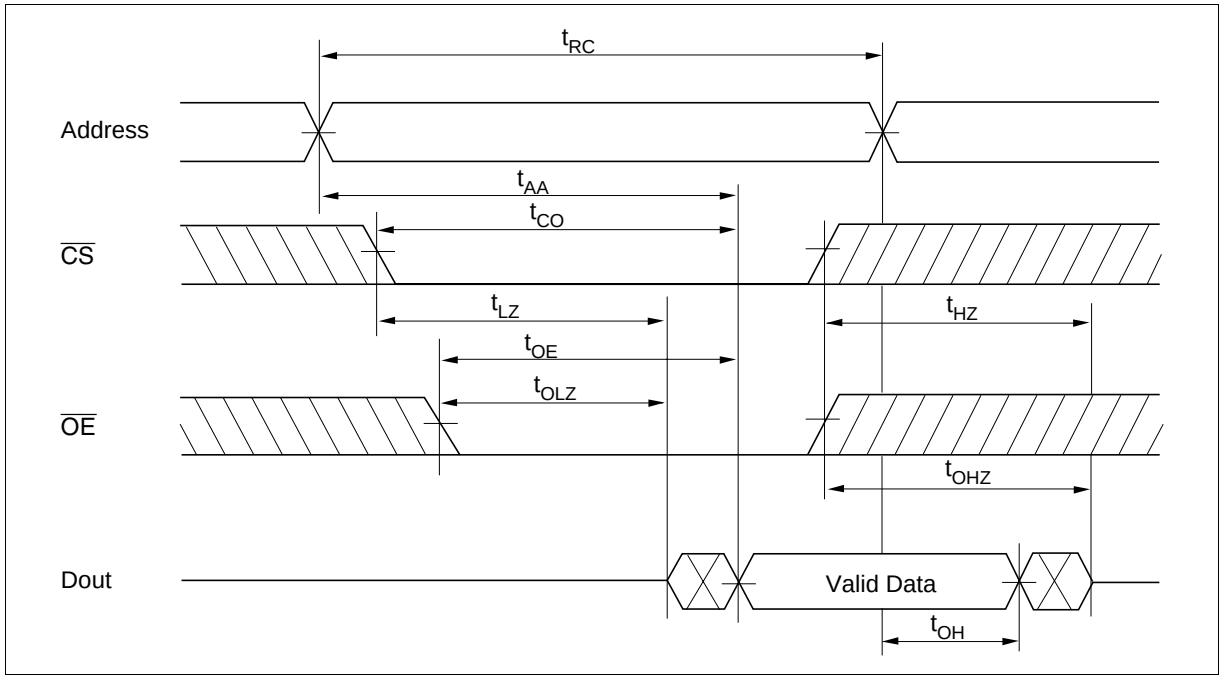
10. Dout is the read data of next address.

11. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

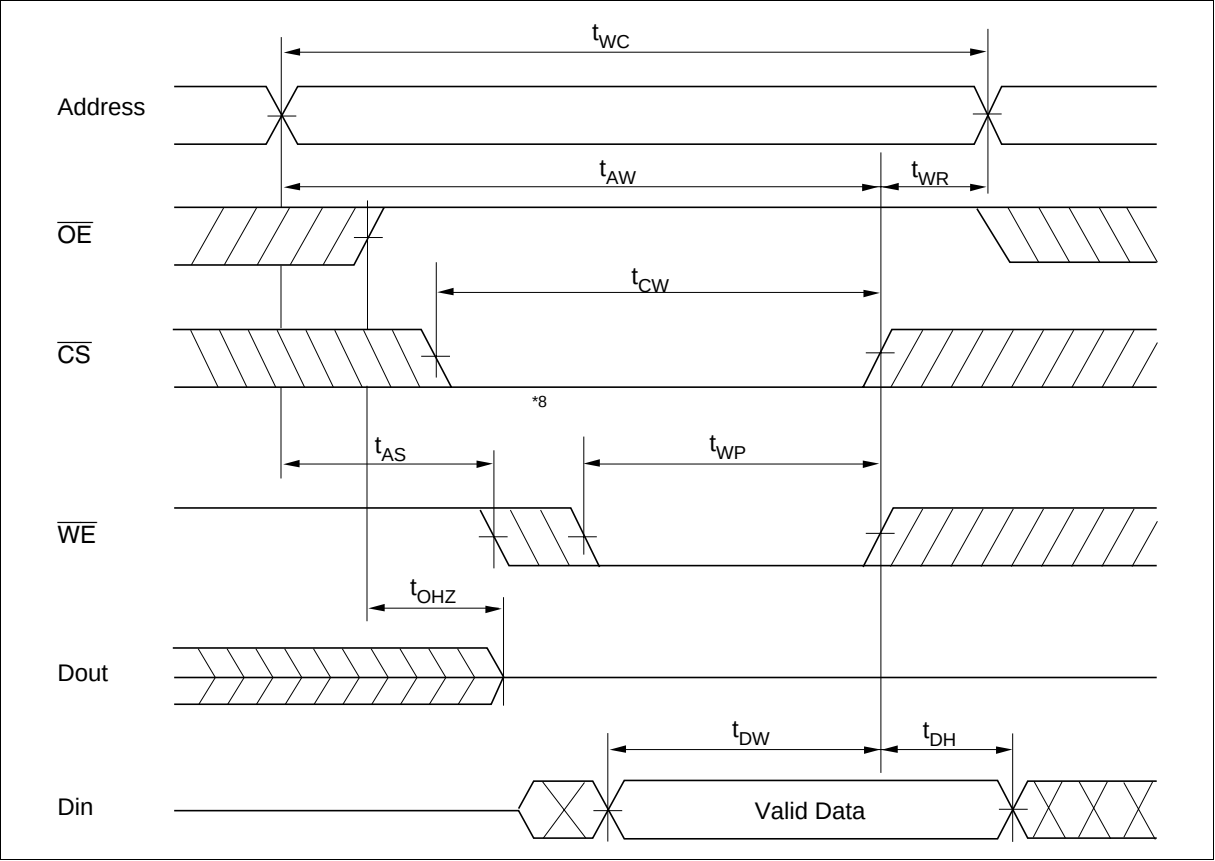
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

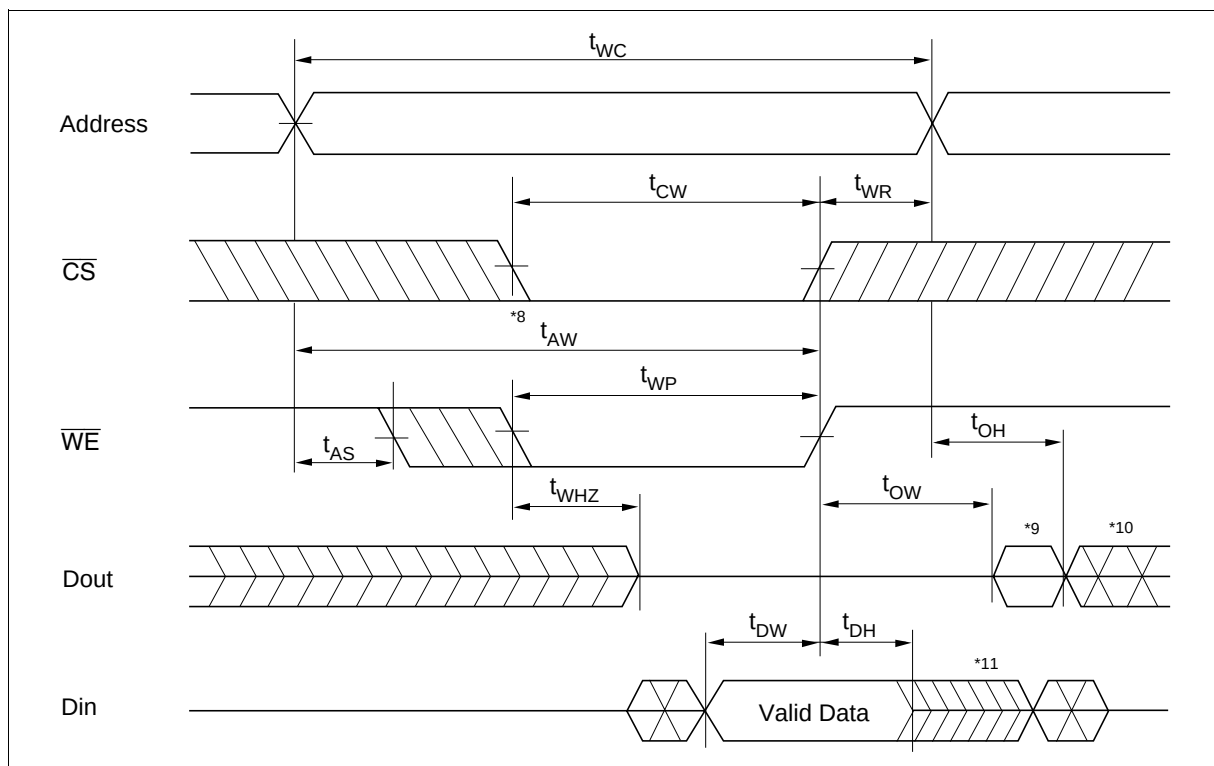
Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)



Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



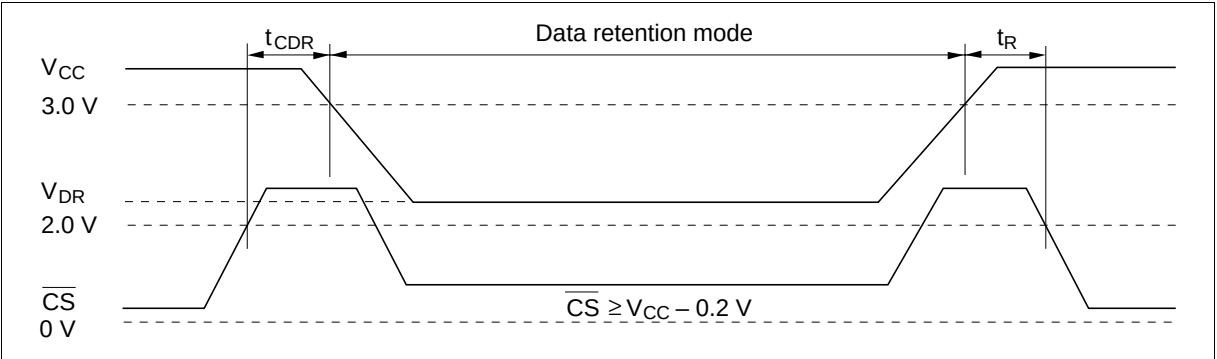
Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

Low V_{CC} Data Retention Characteristics (Ta = -20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*4
V _{CC} for data retention	V _{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, Vin ≥ 0 V
Data retention current	I _{CDDR}	—	0.8*5	20*1	μA	$V_{CC} = 3.0\text{ V}$, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	0.8*5	10*2	μA	
		—	0.8*5	2*3	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	t _{RC} *6	—	—	ns	

- Notes: 1. For L-version and 10 μA (max.) at Ta = -20 to +40°C.
2. For L-SL-version and 3 μA (max.) at Ta = -20 to +40°C.
3. For L-UL-version and 2 μA (max.) at Ta = -20 to +40°C.
4. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
5. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
6. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



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