30V, N-Channel NexFET™ Power MOSFETs

1 Features

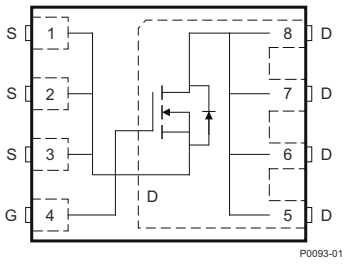
- Ultralow Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb free terminal plating
- RoHS compliant
- Halogen Free
- SON 5mm × 6mm plastic package

2 Applications

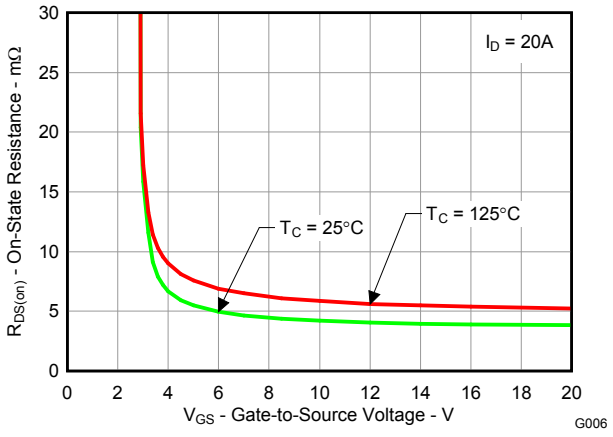
- Point-of-load synchronous buck in networking, telecom, and computing systems
- Optimized for control and synchronous FET applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



Top View



$R_{DS(on)}$ vs V_{GS}

Product Summary

V_{DS}	Drain to Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	6.4		nC
Q_{gd}	Gate Charge Gate to Drain	1.9		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	5.4	mΩ
		V_{GS} = 10V	4.1	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

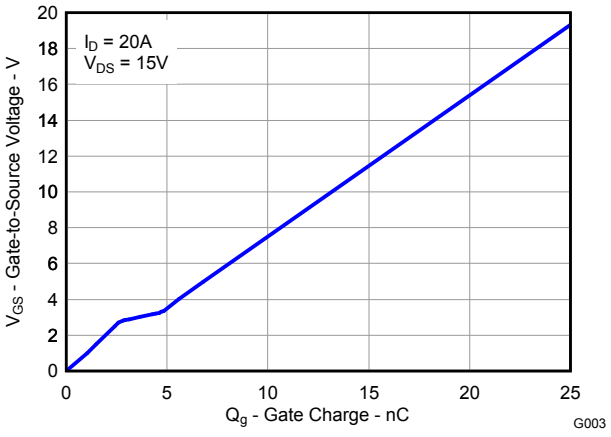
Ordering Information

Device	Package	Media	Qty	Ship
CSD17510Q5A	SON 5mm × 6mm Plastic Package	13-Inch Reel	2500	Tape and Reel

Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current, T_C = 25°C	55	A
	Continuous Drain Current(1)	20	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	129	A
P_D	Power Dissipation(1)	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 54A, L = 0.1mH, R_G = 25Ω	146	mJ

(1) Typical $R_{\theta JA}$ = 41°C/W on 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu pad on a 0.06-inch (1.52mm) thick FR4 PCB.
(2) Pulse duration ≤300µs, duty cycle ≤2%



GATE CHARGE

Table of Contents

4 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250µA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	1	1.5	2.1	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_{DS} = 20A		5.4	7.3	mΩ
		V_{GS} = 10V, I_{DS} = 20A		4.1	5.2	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 20A		59		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		960	1250	pF
C_{oss}	Output Capacitance			630	820	pF
C_{rss}	Reverse Transfer Capacitance			51	66	pF
R_G	Series Gate Resistance			0.85	1.7	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_{DS} = 20A		6.4	8.3	nC
Q_{gd}	Gate Charge Gate to Drain			1.9		nC
Q_{gs}	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at Vth			1.5		nC
Q_{oss}	Output Charge	V_{DS} = 13.5V, V_{GS} = 0V		16		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 20A,R_G = 2Ω		7		ns
t_r	Rise Time			11		ns
$t_{d(off)}$	Turn Off Delay Time			9		ns
t_f	Fall Time			4.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 20A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 13.5V, I_F = 20A, di/dt = 300A/µs		25		nC
t_{rr}	Reverse Recovery Time			24		ns

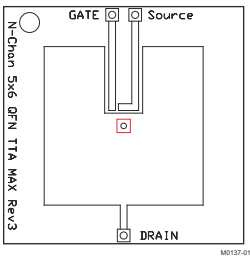
5 Thermal Characteristics

(T_A = 25°C unless otherwise stated)

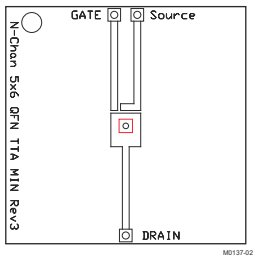
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.6	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81cm × 3.81cm), 0.06-inch (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45cm^2) of 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

6 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

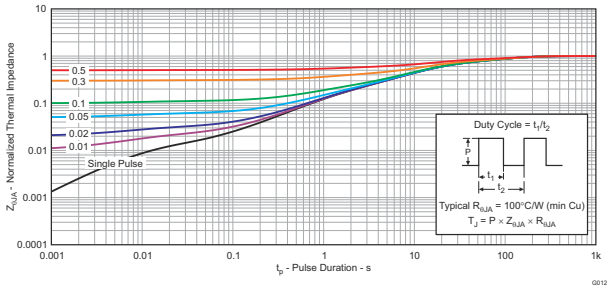


Figure 6-1. Transient Thermal Impedance

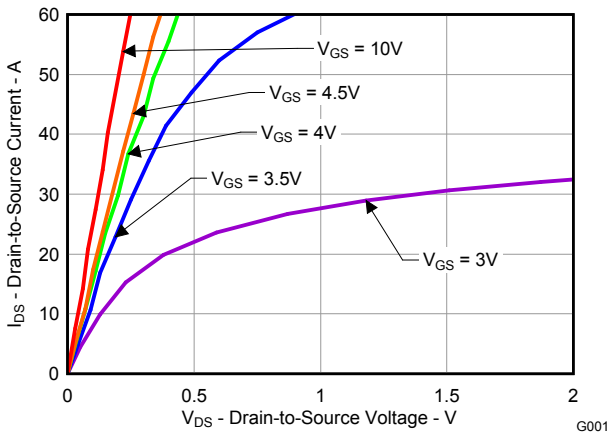


Figure 6-2. Saturation Characteristics

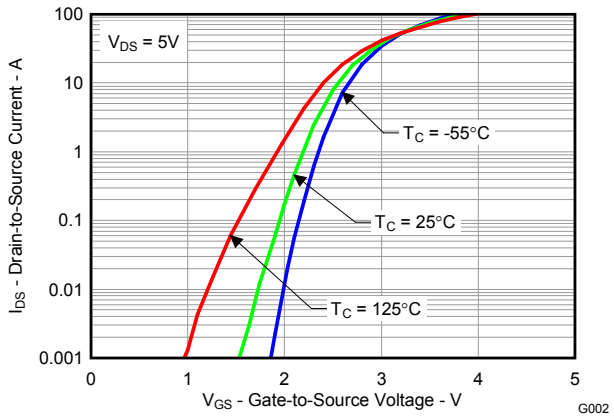


Figure 6-3. Transfer Characteristics

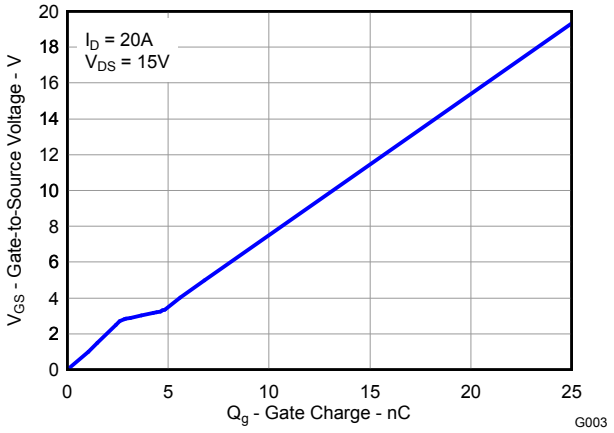


Figure 6-4. Gate Charge

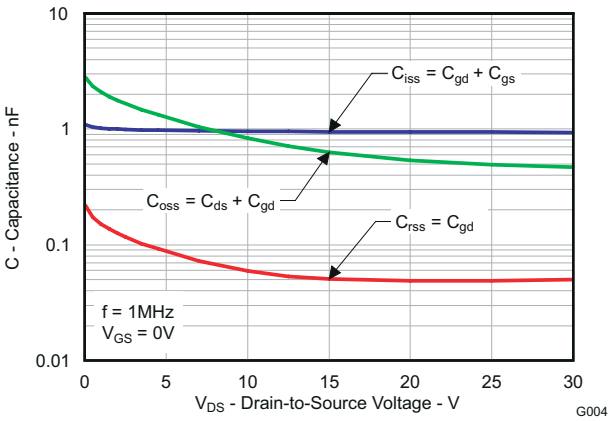


Figure 6-5. Capacitance

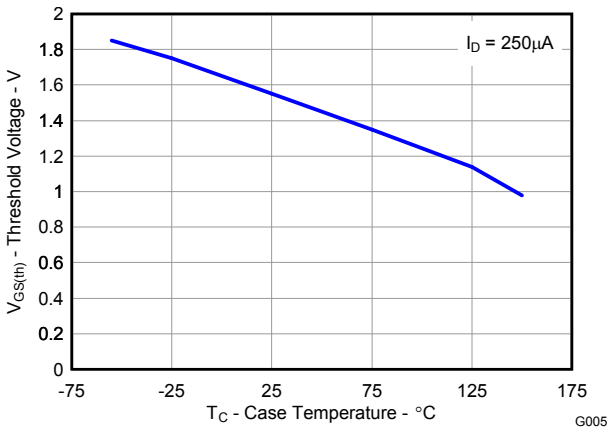


Figure 6-6. Threshold Voltage vs. Temperature

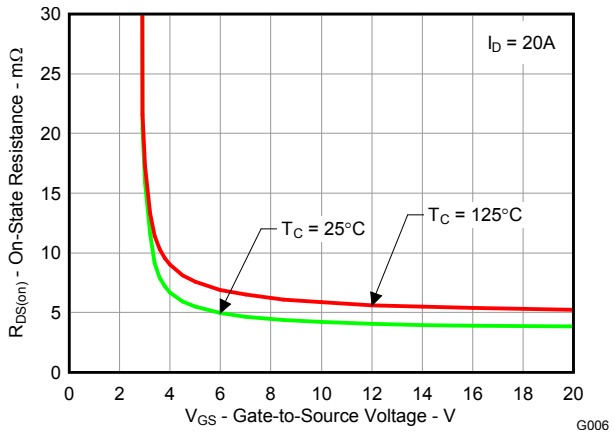


Figure 6-7. On-State Resistance vs. Gate-to-Source Voltage

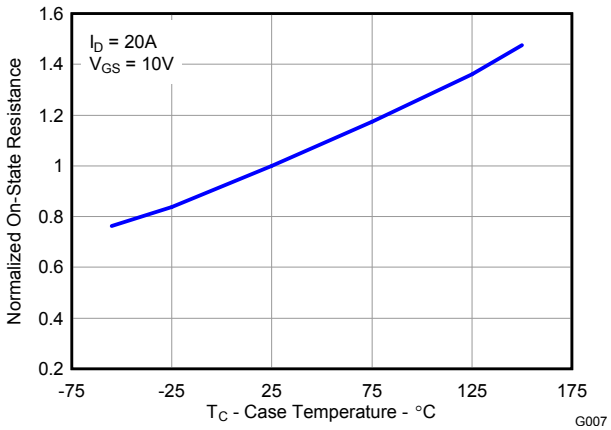


Figure 6-8. Normalized On-State Resistance vs. Temperature

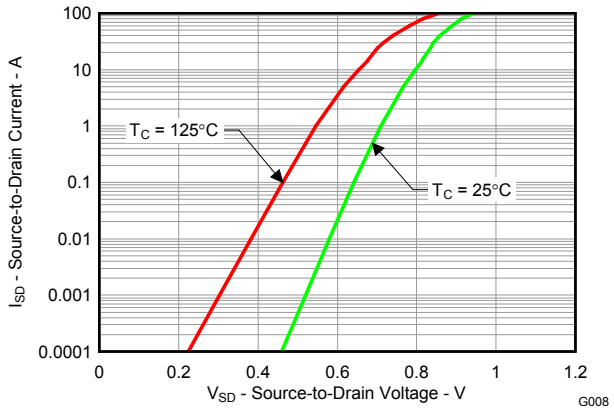


Figure 6-9. Typical Diode Forward Voltage

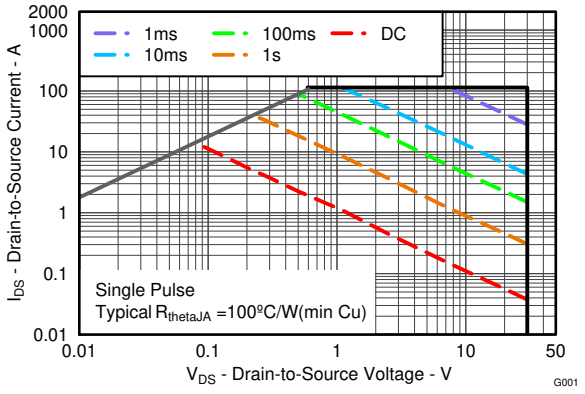


Figure 6-10. Maximum Safe Operating Area

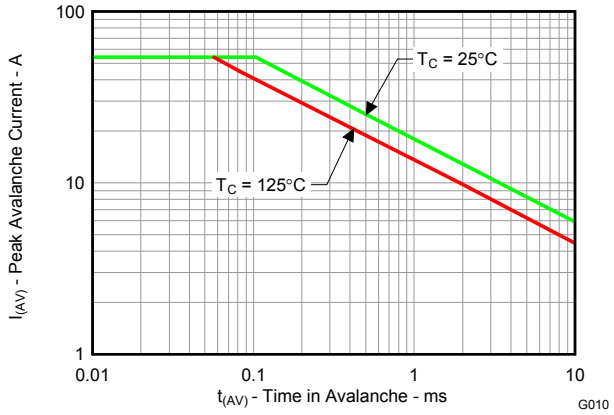


Figure 6-11. Single Pulse Unclamped Inductive Switching

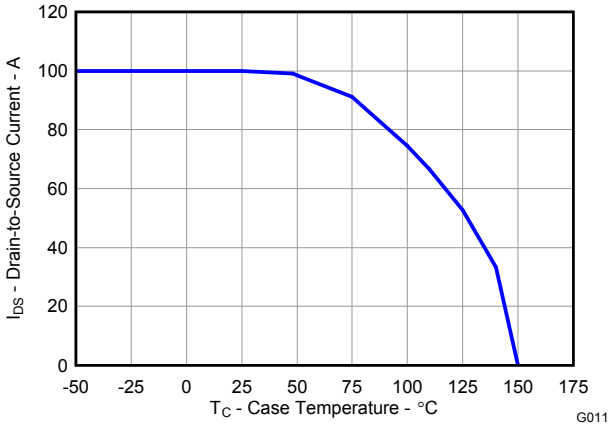


Figure 6-12. Maximum Drain Current vs. Temperature

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Third-Party Products Disclaimer

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7.2 Documentation Support

7.2.1 Related Documentation

7.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.4 Support Resources

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7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2012) to Revision H (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (July 2010) to Revision A ()	Page
• Changed the Y axis scale for Figure 6-5	4

Changes from Revision F (October 2011) to Revision G (September 2012)	Page
• Changed Figure 6-10	4

Changes from Revision E (July 2011) to Revision F (October 2011)	Page
• Changed the I_D Continuous Drain Current, T_C = 25°C value From: 100A To: 55A	1
• Changed Figure 6-10	4

Changes from Revision A (August 2010) to Revision B ()	Page
• Changed $R_{DS(on)}$ Test Conditions From V_{GS} = 8V To: V_{GS} = 10V	3

Changes from Revision B (September 2010) to Revision C ()	Page
• Absolute Maximum Ratings, changed the E_{AS} value from 45 to 146mJ	1

Changes from Revision C (September 2010) to Revision D ()	Page

Changes from Revision D (November 2010) to Revision E ()	Page
• Changed V_{GS} in the Abs Max Ratings table From: +20/-12V To: ±20V	1
• Changed from +20/-12V to 20V	3

9 Mechanical Data

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17510Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17510
CSD17510Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

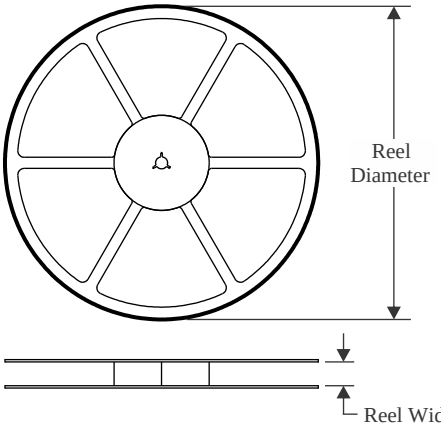
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

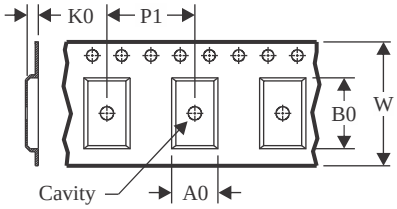
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

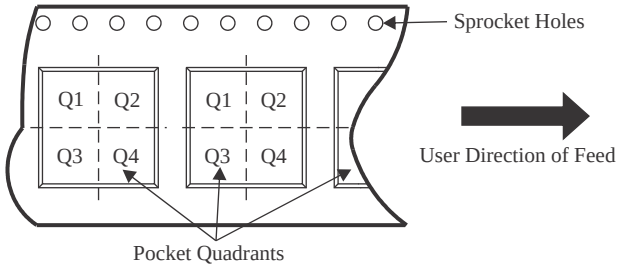


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

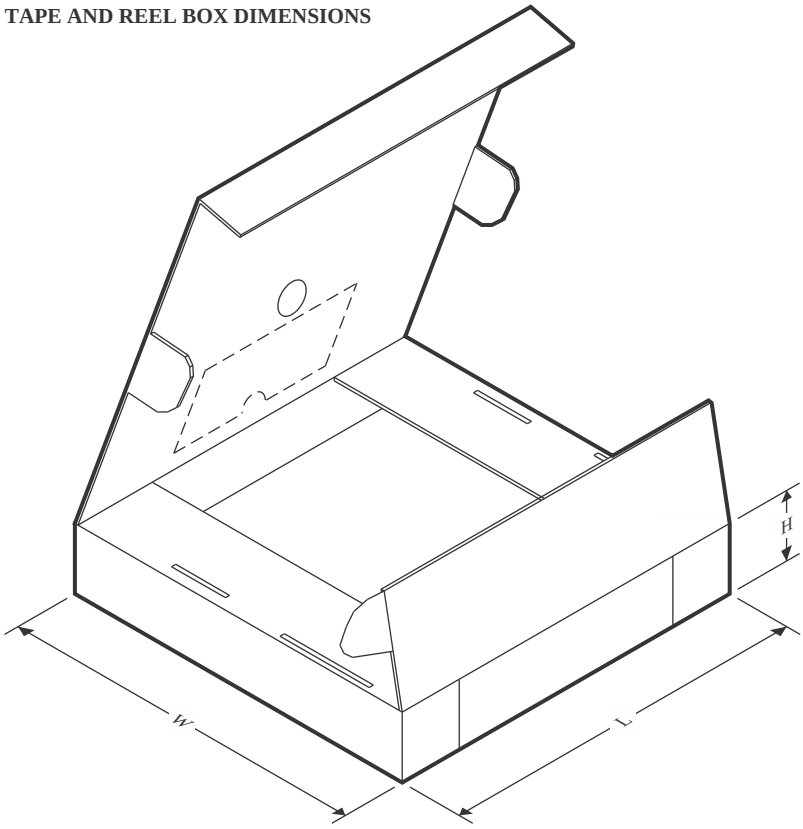
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

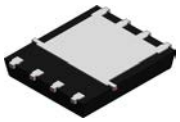
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17510Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17510Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

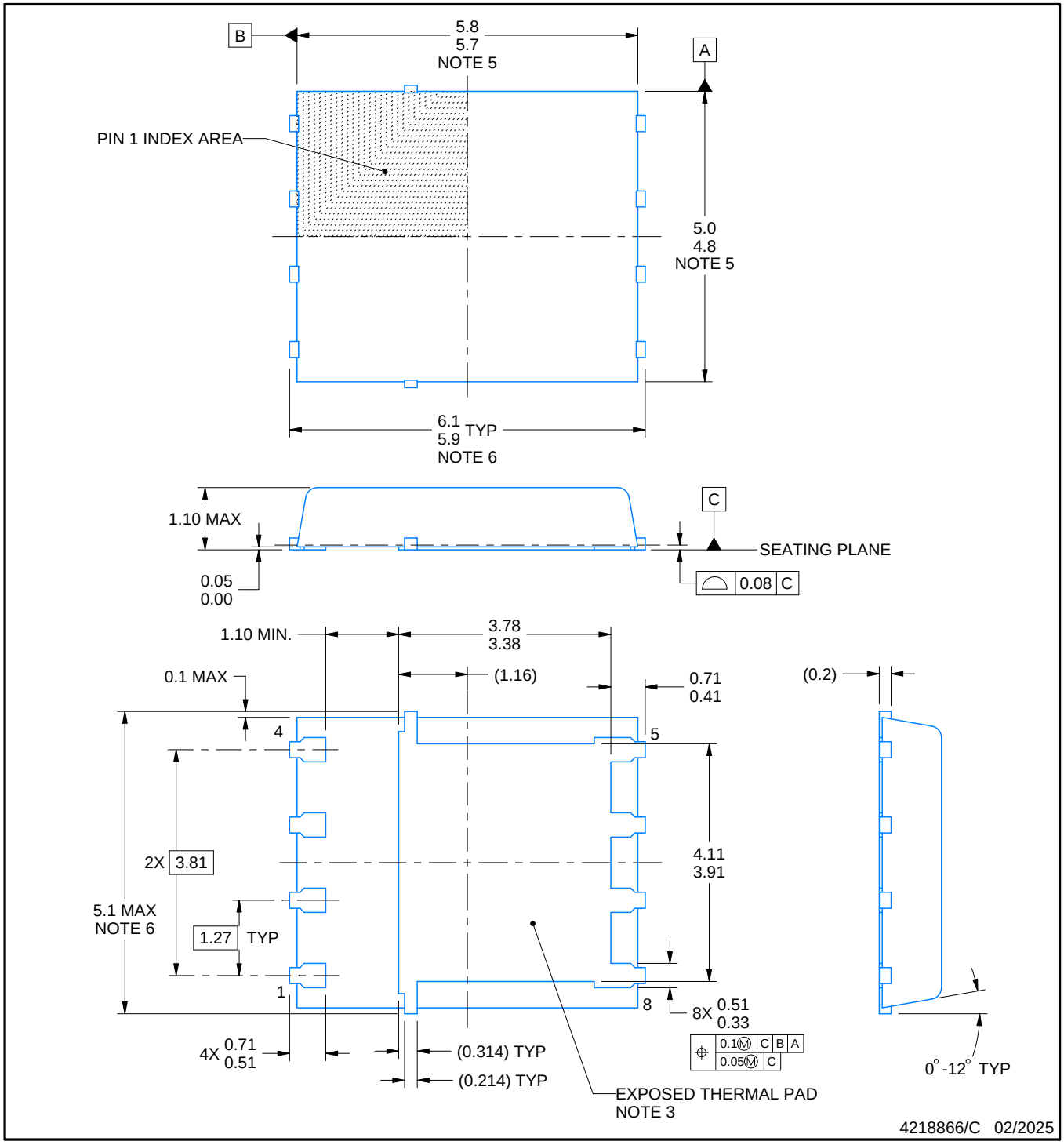


PACKAGE OUTLINE

DQJ0008A

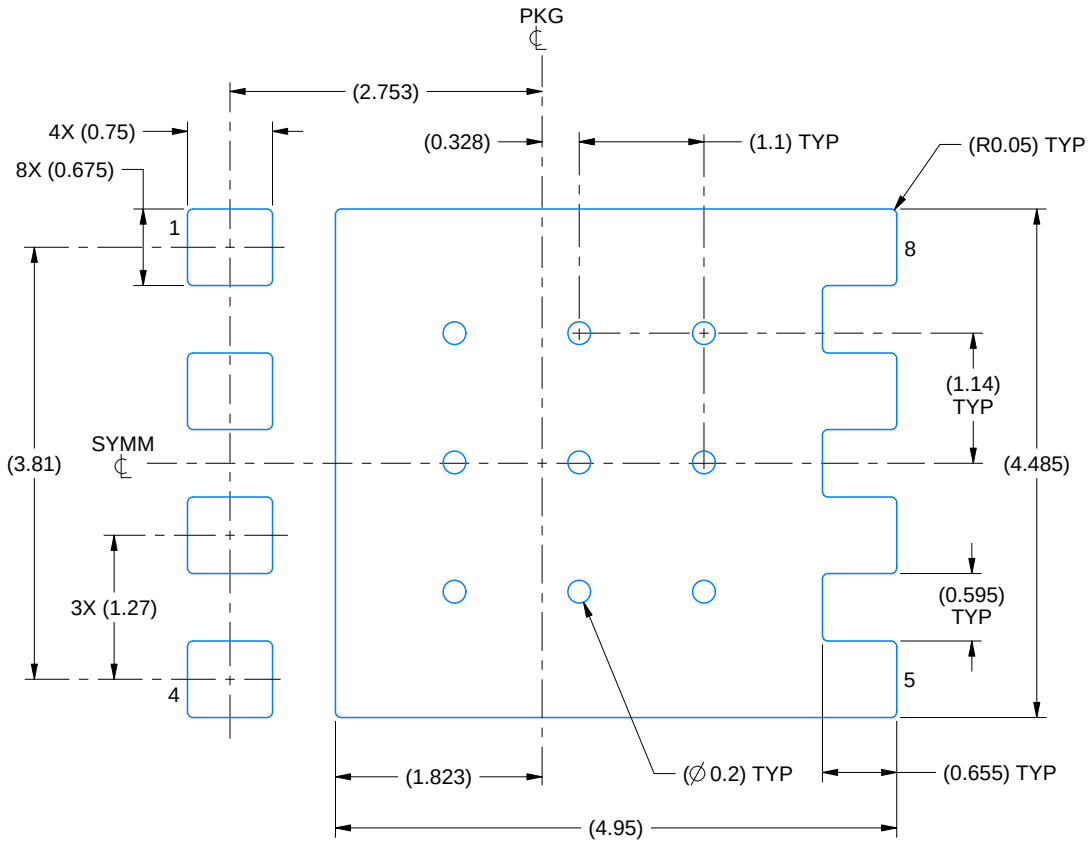
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

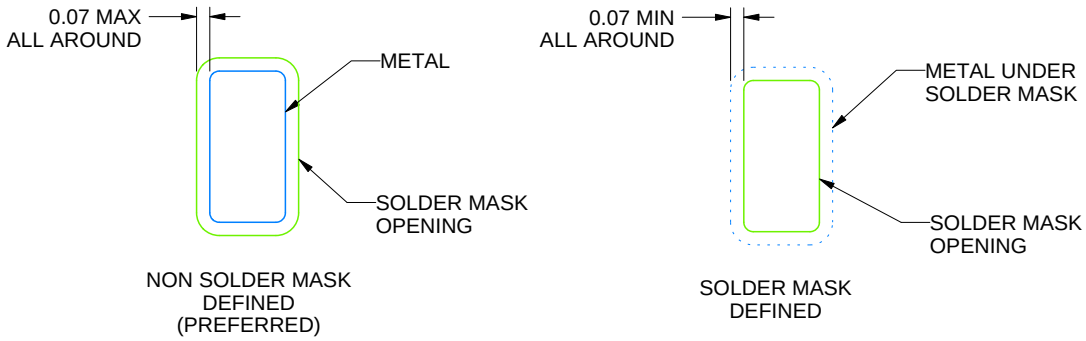


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

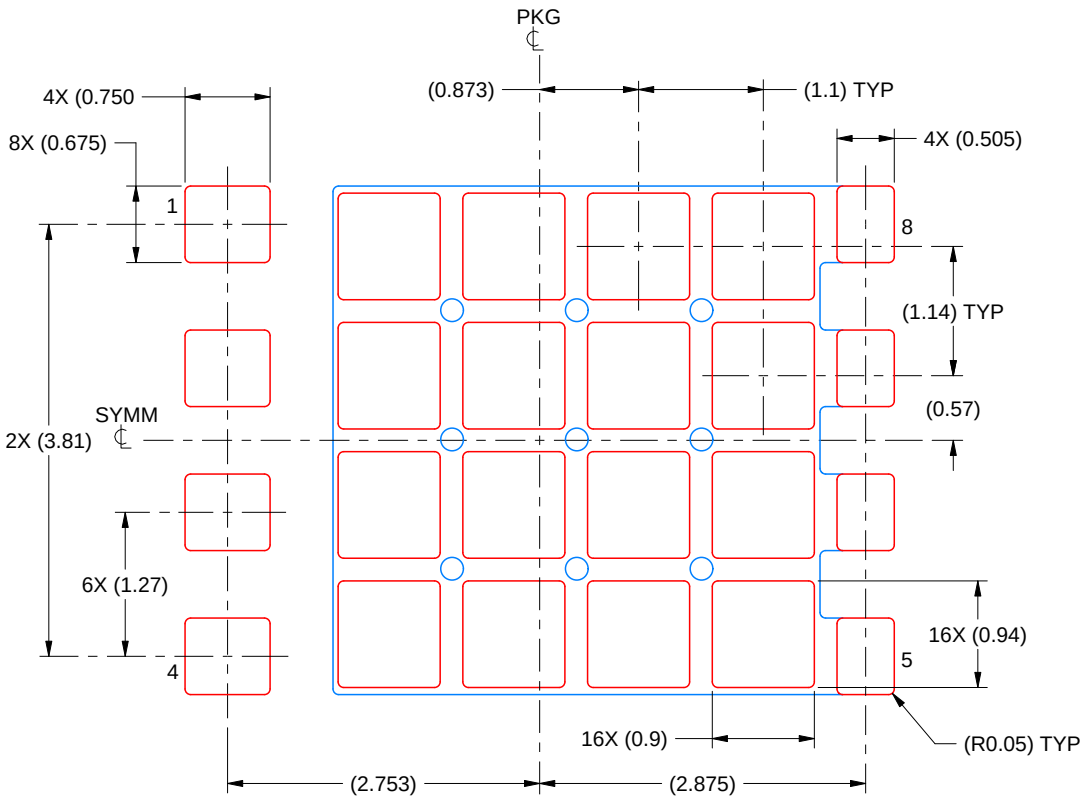


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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