

FDFS2P103A

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

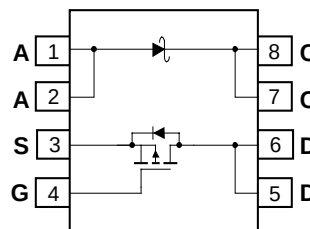
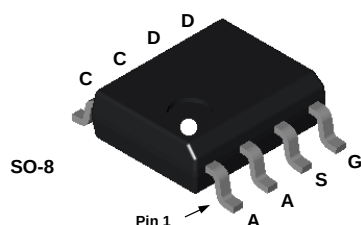
General Description

The FDFS2P103A combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

Features

- -5.3 A , -30 V $R_{DS(ON)} = 59\text{ m}\Omega$ @ $V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 92\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$
- $V_F < 0.35\text{ V}$ @ 1 A ($T_J = 125^\circ\text{C}$)
 $V_F < 0.25\text{ V}$ @ 1 A ($T_J = 25^\circ\text{C}$)
- Schottky and MOSFET incorporated into single power surface mount SO-8 package
- Electrically independent Schottky and MOSFET pinout for design flexibility



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	MOSFET Drain-Source Voltage	-30	V
V_{GSS}	MOSFET Gate-Source Voltage	± 25	V
I_D	Drain Current – Continuous (Note 1a)	-5.3	A
	– Pulsed	-20	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$
V_{RRM}	Schottky Repetitive Peak Reverse Voltage	30	V
I_O	Schottky Average Forward Current (Note 1a)	1	A

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDFS2P103A	FDFS2P103A	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		-22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		4.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -5.3\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -5.3\text{ A}, T_J = 125^\circ\text{C}$		50 76 68	59 92 88	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -5.3\text{ A}$		8.9		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		535		pF
C_{oss}	Output Capacitance			135		pF
C_{rss}	Reverse Transfer Capacitance			75		pF
R_G	Gate Resistance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		4.7		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		11	21	ns
t_r	Turn–On Rise Time			16	28	ns
$t_{d(off)}$	Turn–Off Delay Time			15	26	ns
t_f	Turn–Off Fall Time			10	19	ns
Q_g	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -5.3\text{ A},$ $V_{GS} = -5\text{ V}$		5.7	8	nC
Q_{gs}	Gate–Source Charge			1.8		nC
Q_{gd}	Gate–Drain Charge			2.4		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				-1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.8	-1.2	V

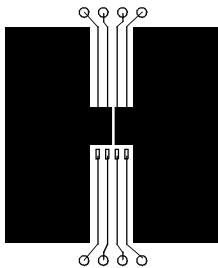
Schottky Diode Characteristics

I_R	Reverse Leakage	$V_R = 30\text{ V}$			160	500	μA
V_F	Forward Voltage	$I_F = 0.1\text{ A}$	$T_J = 25^\circ\text{C}$		225	280	mV
			$T_J = 125^\circ\text{C}$		80	250	mV
		$I_F = 1\text{ A}$	$T_J = 25^\circ\text{C}$		305	350	mV
			$T_J = 125^\circ\text{C}$		185	250	mV
		$I_F = 3\text{ A}$	$T_J = 25^\circ\text{C}$		380	420	mV

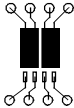
Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	135	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	$^{\circ}\text{C/W}$

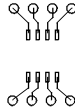
Notes:
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78 $^{\circ}\text{C/W}$ when mounted on a 0.5in² pad of 2 oz copper



b) 125 $^{\circ}\text{C/W}$ when mounted on a 0.02 in² pad of 2 oz copper



c) 135 $^{\circ}\text{C/W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

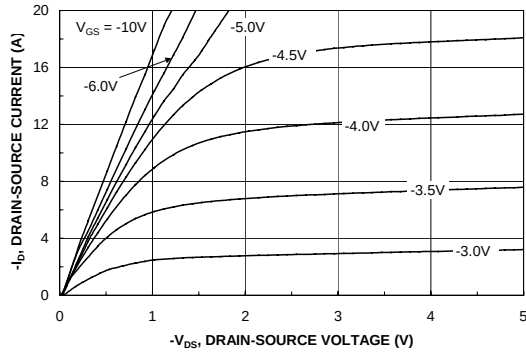


Figure 1. On-Region Characteristics.

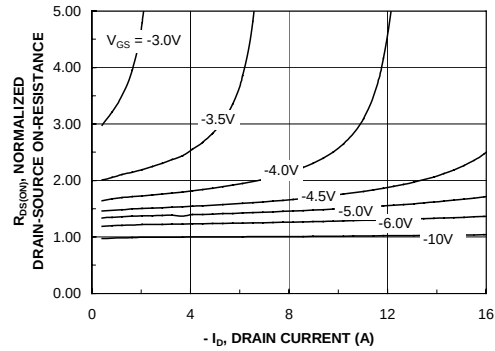


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

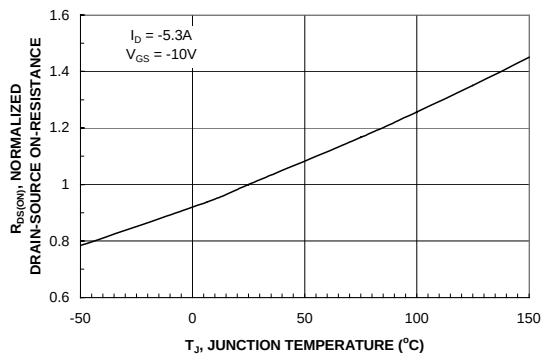


Figure 3. On-Resistance Variation with Temperature.

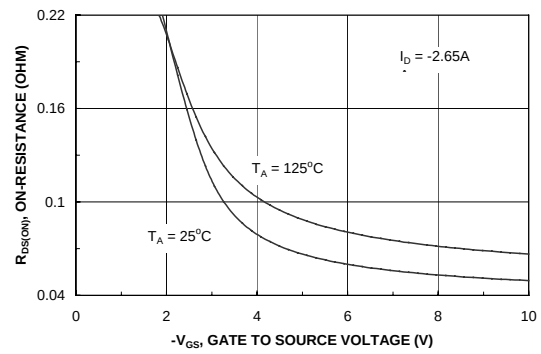


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

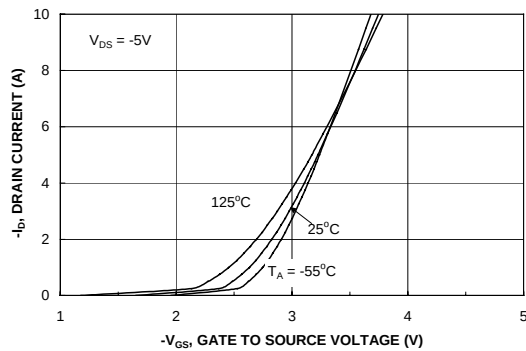


Figure 5. Transfer Characteristics.

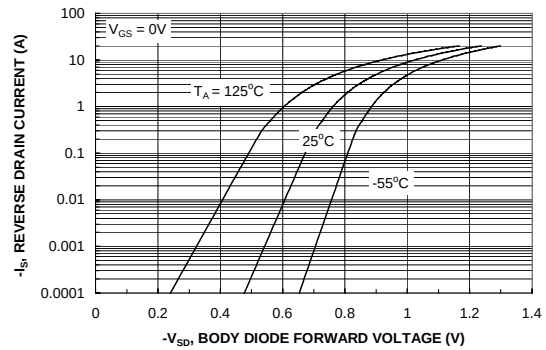


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

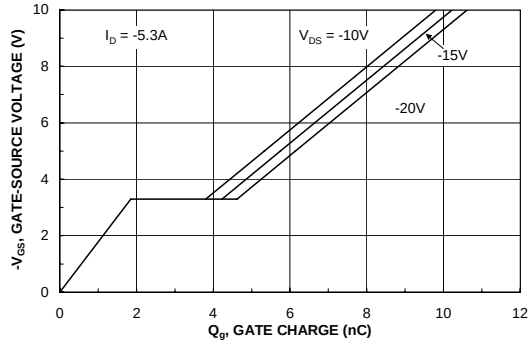


Figure 7. Gate Charge Characteristics.

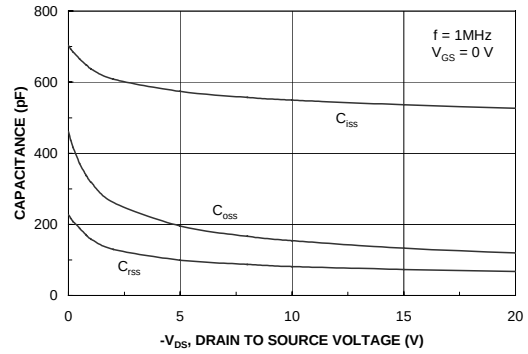


Figure 8. Capacitance Characteristics.

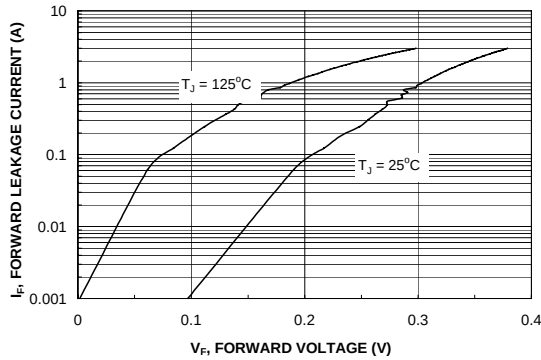


Figure 9. Schottky Diode Forward Voltage.

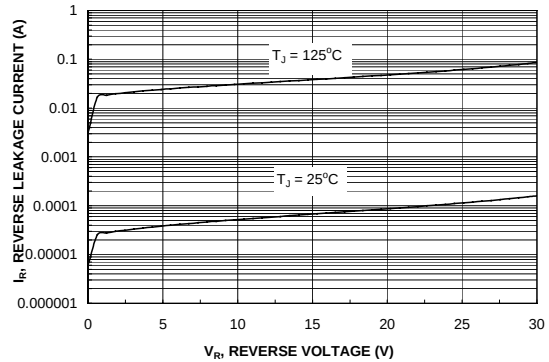


Figure 10. Schottky Diode Reverse Current.

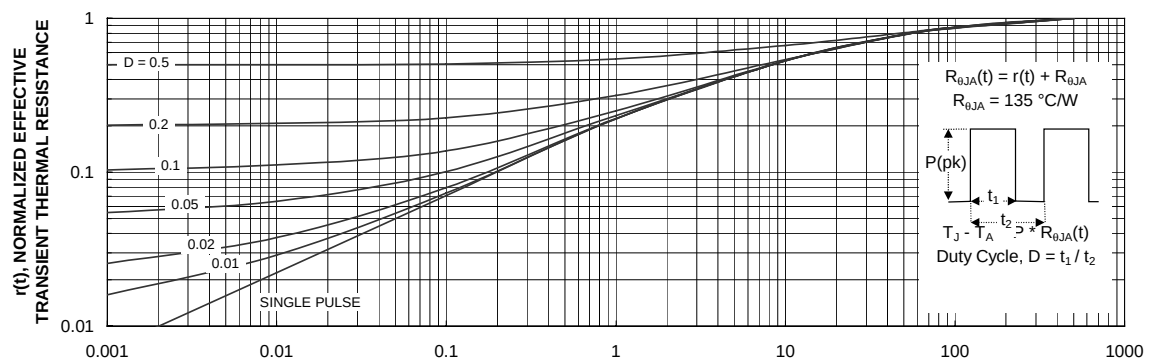


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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