

IS31AP4990D

1.2W AUDIO POWER AMPLIFIER WITH ACTIVE-LOW SHUTDOWN MODE

June 2014

DESCRIPTION

The IS31AP4990D has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

It is capable of delivering 1.2W of continuous RMS output power into an 8Ω load @ 5V.

An externally-controlled shutdown mode reduces the supply current to less than 1μA. It also includes internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

FEATURES

- Operating from $V_{CC} = 2.7V \sim 5.5V$
- 1.2W output power @ $V_{CC} = 5V$, THD+N= 1%,
 $f = 1kHz$, with 8Ω load
- Ultra-low consumption in shutdown mode (1μA)
- Near-zero pop & click
- Ultra-low distortion
- Unity gain stable
- UTQFN-9L (1.5mm × 1.5mm) package

APPLICATIONS

- Mobile phones
- PDAs
- Portable electronic devices
- Notebook computer

TYPICAL APPLICATION CIRCUIT

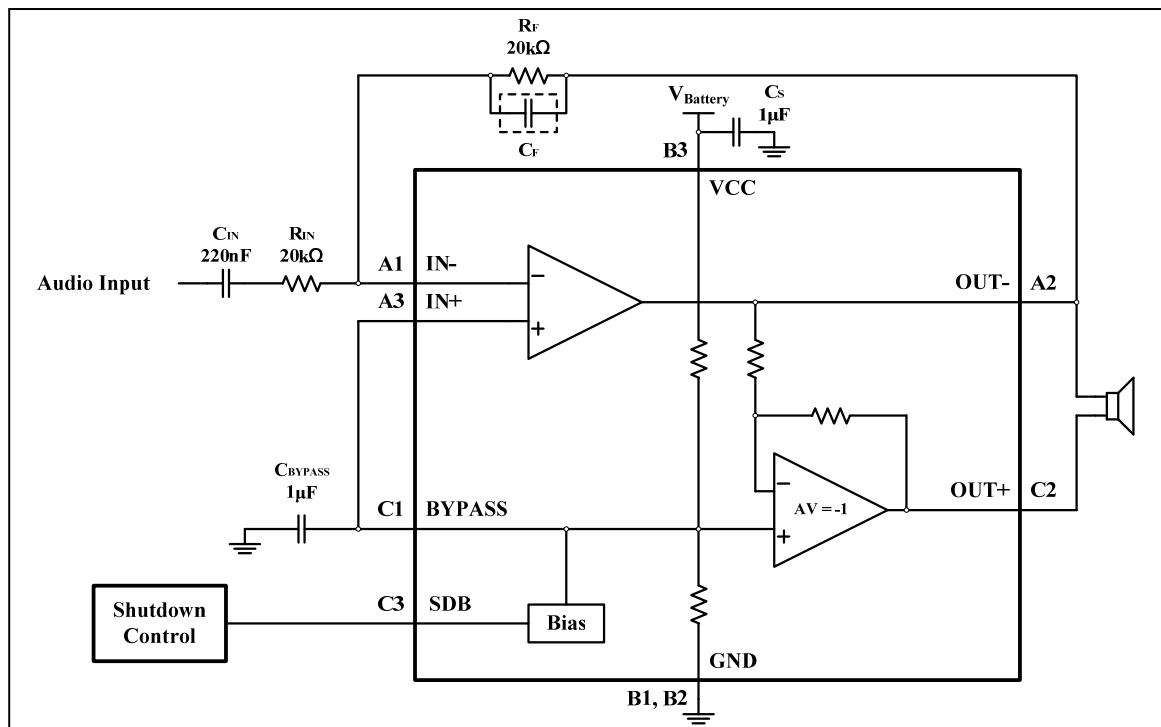


Figure 1 Typical Application Circuit (Single-ended Input)

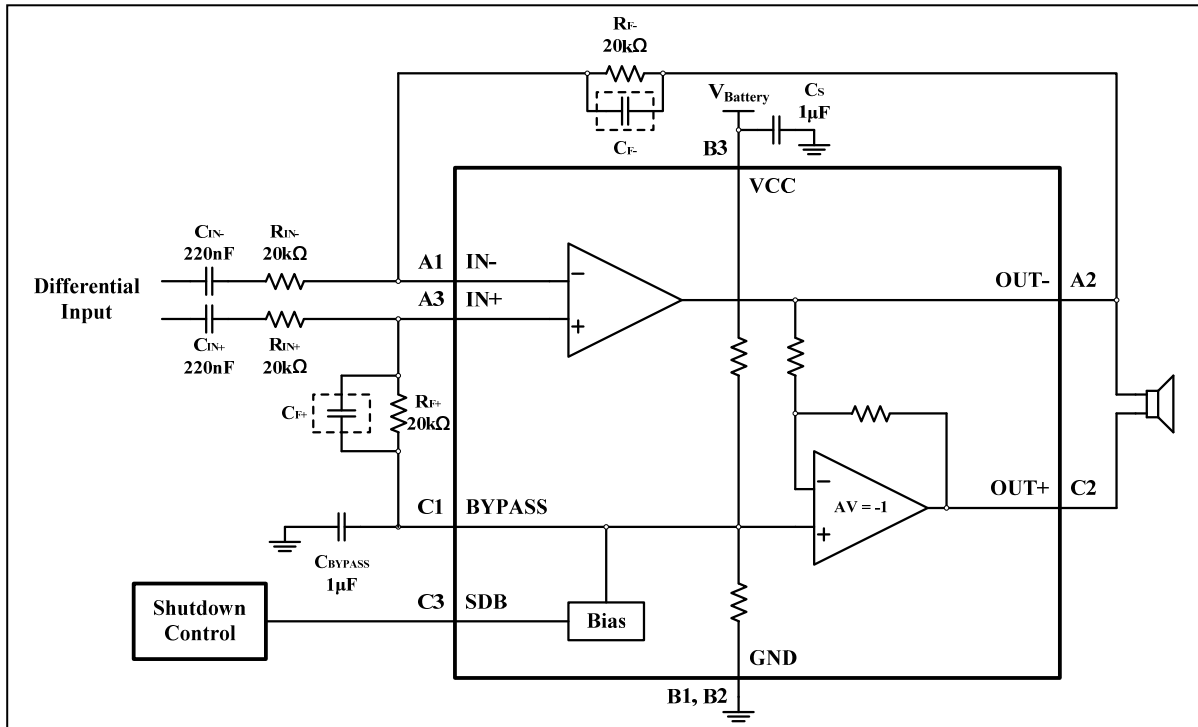
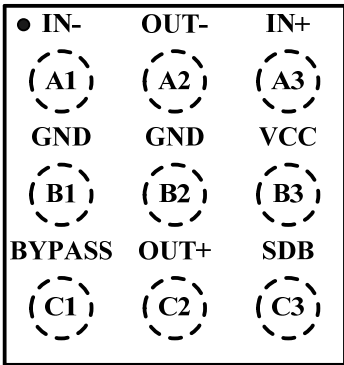


Figure 2 Typical Application Circuit (Differential Input)

IS31AP4990D

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UTQFN-9L	

PIN DESCRIPTION

No.	Pin	Function Description
A1	IN-	Negative input of the first amplifier. Connected to the feedback resistor R_{F-} and to the input resistor R_{IN-} .
A2	OUT-	Negative output. Connected to the load and to the feedback resistor R_{F-} .
A3	IN+	Positive input of the first amplifier.
B1,B2	GND	Ground.
B3	VCC	Supply voltage.
C1	BYPASS	Bypass capacitor pin which provides the common mode voltage ($V_{CC}/2$).
C2	OUT+	Positive output. Connected to the load.
C3	SDB	The device enters in shutdown mode when a low level is applied on this pin.



IS31AP4990D

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4990D-UTLS2-TR	UTQFN-9, Lead-free	3000

Copyright © 2014 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products. Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

IS31AP4990D

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.3V$
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
ESD (HBM)	7kV
ESD (CDM)	500V

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$, $V_{CC} = 2.7V \sim 5.5V$, unless otherwise noted. Typical value are $T_A = +25^{\circ}\text{C}$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Power supply		2.7		5.5	V
I_{CC}	Quiescent current	$V_{CC} = 5V$, $V_{IN} = 0V$, $I_O = 0A$, no load		3.8	6.4	mA
		$V_{CC} = 3V$, $V_{IN} = 0V$, $I_O = 0A$, no load		2.8	5.1	
I_{SD}	Shutdown current	$V_{SDB} = GND$, no load			1	μA
V_{IH}	Shutdown voltage input high		1.4			V
V_{IL}	Shutdown voltage input low				0.4	V
V_{OS}	Output offset voltage				25	mV
P_o	Output power (8 Ω)	$V_{CC} = 5V$	THD+N = 1%, f = 1kHz	1.20		W
			THD+N = 10%, f = 1kHz	1.50		
		$V_{CC} = 3V$	THD+N = 1%, f = 1kHz	0.418		
			THD+N = 10%, f = 1kHz	0.525		
t_{WU}	Wake-up time (Note 1)	$V_{CC} = 5V$, $C_{BYPASS} = 1\mu F$		115		ms
		$V_{CC} = 3V$, $C_{BYPASS} = 1\mu F$		102		
THD+N	Total harmonic distortion + noise (Note 1)	$V_{CC} = 5V$, $P_o = 0.5W_{rms}$, f = 1kHz		0.23		%
		$V_{CC} = 3V$, $P_o = 0.3W_{rms}$, f = 1kHz		0.15		
PSRR	Power supply rejection ratio (Note 1)	$V_{CC} = 5V$ $V_{Ripple\ p-p} = 200mV$ Input grounded	f = 217Hz	61		dB
			f = 1kHz	65		
		$V_{CC} = 3.6V, 4.2V$ $V_{Ripple\ p-p} = 200mV$ Input grounded	f = 217Hz	62		
			f = 1kHz	66		

Note 1: Guaranteed by design.

IS31AP4990D

TYPICAL PERFORMANCE CHARACTERISTIC

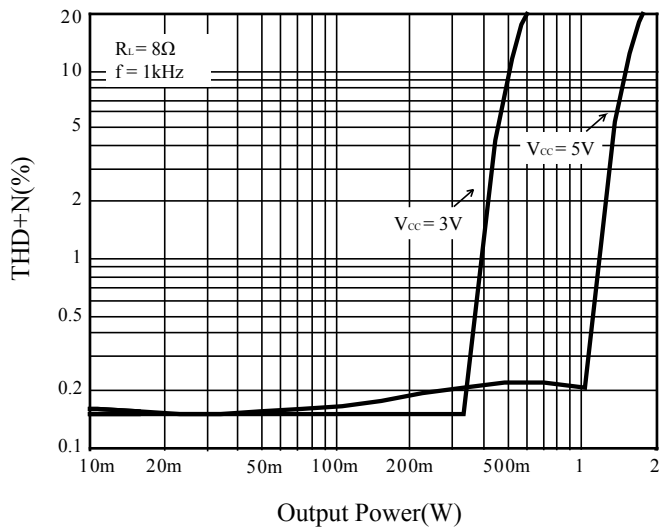


Figure 3 THD+N vs. Output Power

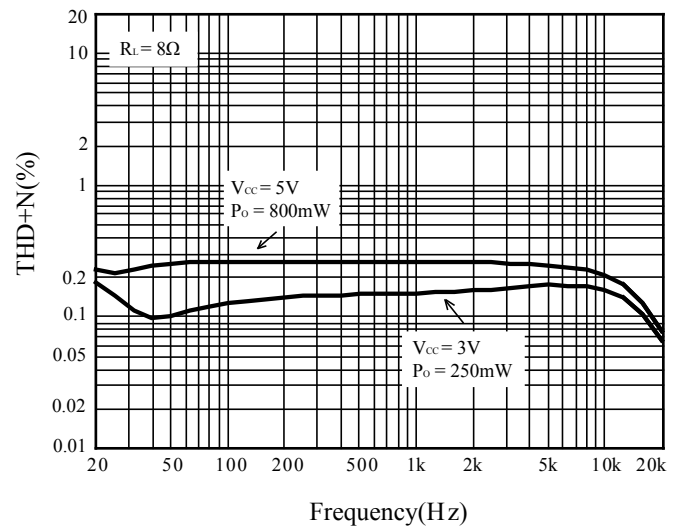


Figure 4 THD+N vs. Frequency

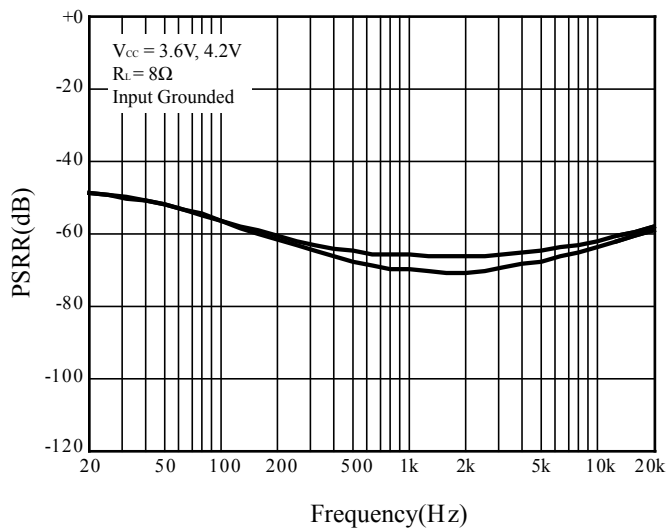


Figure 5 PSRR vs. Frequency

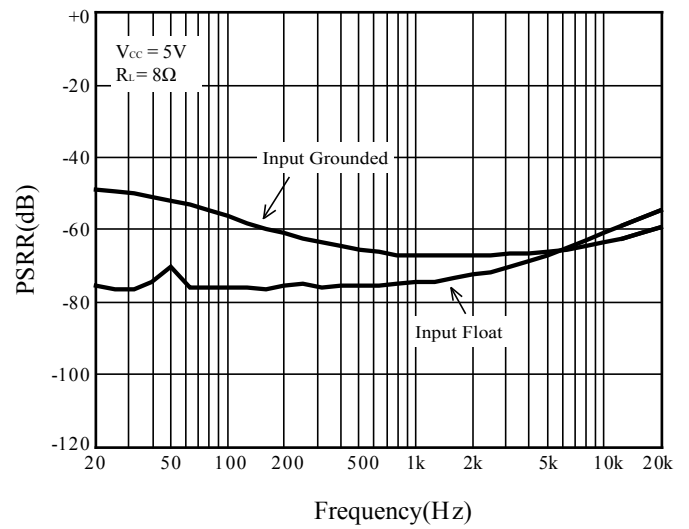


Figure 6 PSRR vs. Frequency

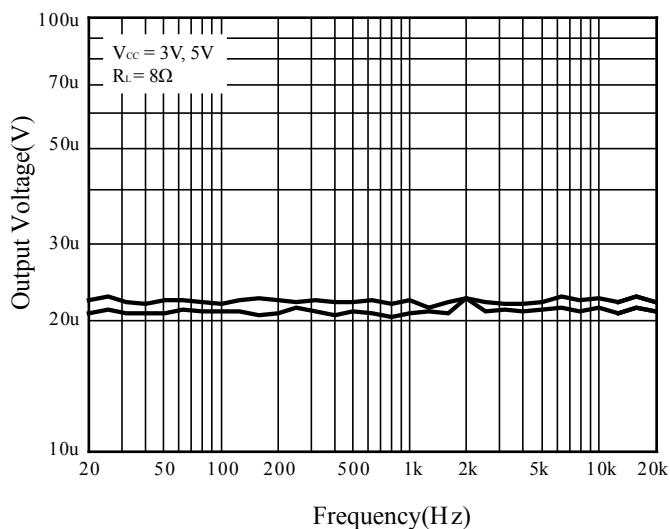


Figure 7 Noise Floor

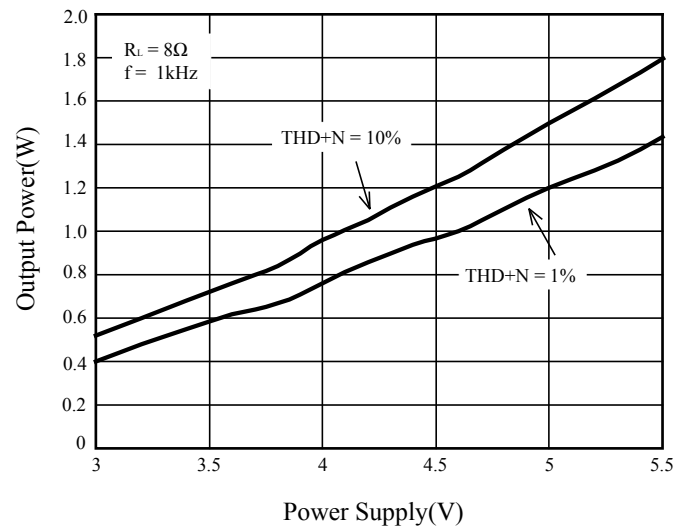


Figure 8 Output Power vs. Power Supply

IS31AP4990D

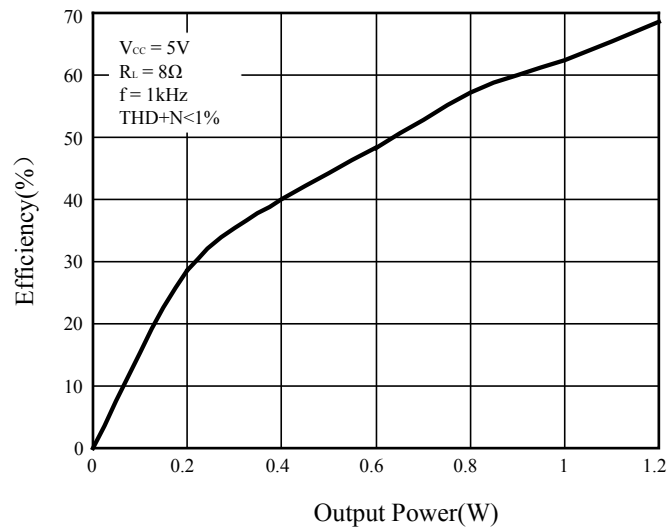


Figure 9 Efficiency vs. Output Power

IS31AP4990D

APPLICATION INFORMATION

BTL CONFIGURATION PRINCIPLE

The IS31AP4990D is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

$$\text{Single-ended output 1} = V_{OUT+} = V_{OUT} \text{ (V)}$$

$$\text{Single ended output 2} = V_{OUT-} = -V_{OUT} \text{ (V)}$$

$$\text{and } V_{OUT+} - V_{OUT-} = 2V_{OUT} \text{ (V)}$$

The output power is:

$$P_{OUT} = \frac{(2V_{OUT_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

GAIN IN A TYPICAL APPLICATION SCHEMATIC

The typical application schematic is shown in Figure 1 on page 1.

In the flat region (no C_{IN} effect), the output voltage of the first stage is (in Volts):

$$V_{OUT-} = (-V_{IN}) \frac{R_F}{R_{IN}}$$

For the second stage: $V_{OUT+} = -V_{OUT-}$ (V)

The differential output voltage is (in Volts):

$$V_{OUT+} - V_{OUT-} = 2V_{IN} \frac{R_F}{R_{IN}}$$

The differential gain, G_v , in shourt, is given by:

$$G_v = \frac{V_{OUT+} - V_{OUT-}}{V_{IN}} = 2 \frac{R_F}{R_{IN}}$$

V_{OUT+} is in phase with V_{IN} and V_{OUT-} is phased 180° with V_{IN} . This means that the positive terminal of the loudspeaker should be connected to V_{OUT+} and the negative to V_{OUT-} .

LOW AND HIGH FREQUENCY RESPONSE

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} a high-pass filter with a -3dB cut-off frequency. f_{CL} is in Hz.

$$f_{CL} = \frac{1}{2\pi R_{IN} C_{IN}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_F) in parallel with R_F . It forms a low-pass filter with a -3dB cut-off frequency. f_{CH} is in Hz.

$$f_{CH} = \frac{1}{2\pi R_F C_F}$$

DECOUPLING OF THE CIRCUIT

Two capacitors are needed to correctly bypass the IS31AP4990D: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_{BYPASS} .

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of $1\mu F$, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_S is lower than $1\mu F$, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than $1\mu F$, those disturbances on the power supply rail are more filtered.

C_{BYPASS} has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_{BYPASS} is lower than $1\mu F$, THD+N increases at lower frequencies and PSRR worsens.

If C_{BYPASS} is higher than $1\mu F$, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN} , the higher the PSRR is.

WAKE-UP TIME (t_{WU})

When the SDB pin is released to put the device ON, the bypass capacitor C_{BYPASS} will not be charged immediately. As C_{BYPASS} is directly linked to the bias of the amplifier, the bias will not work properly until the C_{BYPASS} voltage is correct. The time to reach this voltage is called wake-up time or t_{WU} and specified in the electrical characteristics table with $C_{BYPASS} = 1\mu F$.

POP PERFORMANCE

Pop performance is intimately linked with the size of the input capacitor C_{IN} and the bias voltage bypass capacitor C_{BYPASS} .

The size of C_{IN} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_{BYPASS} is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_{BYPASS} determines the speed with which the amplifier turns ON.

IS31AP4990D

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

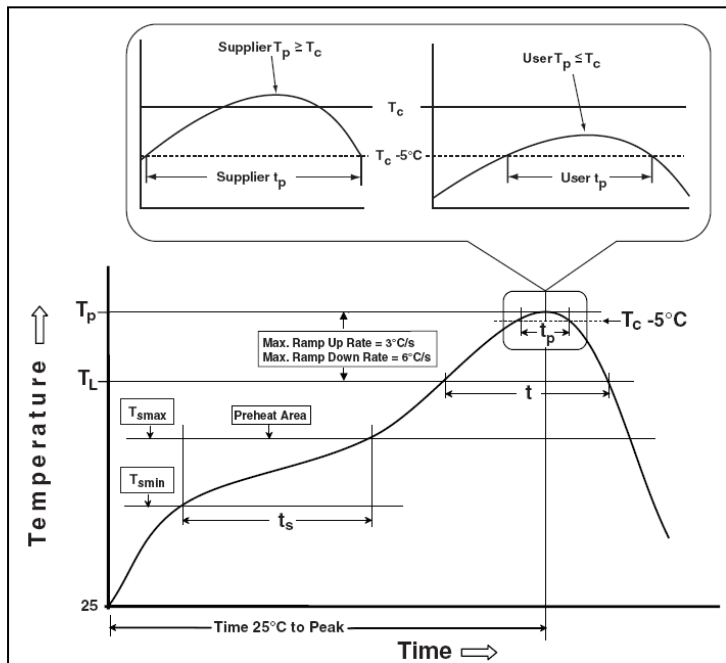
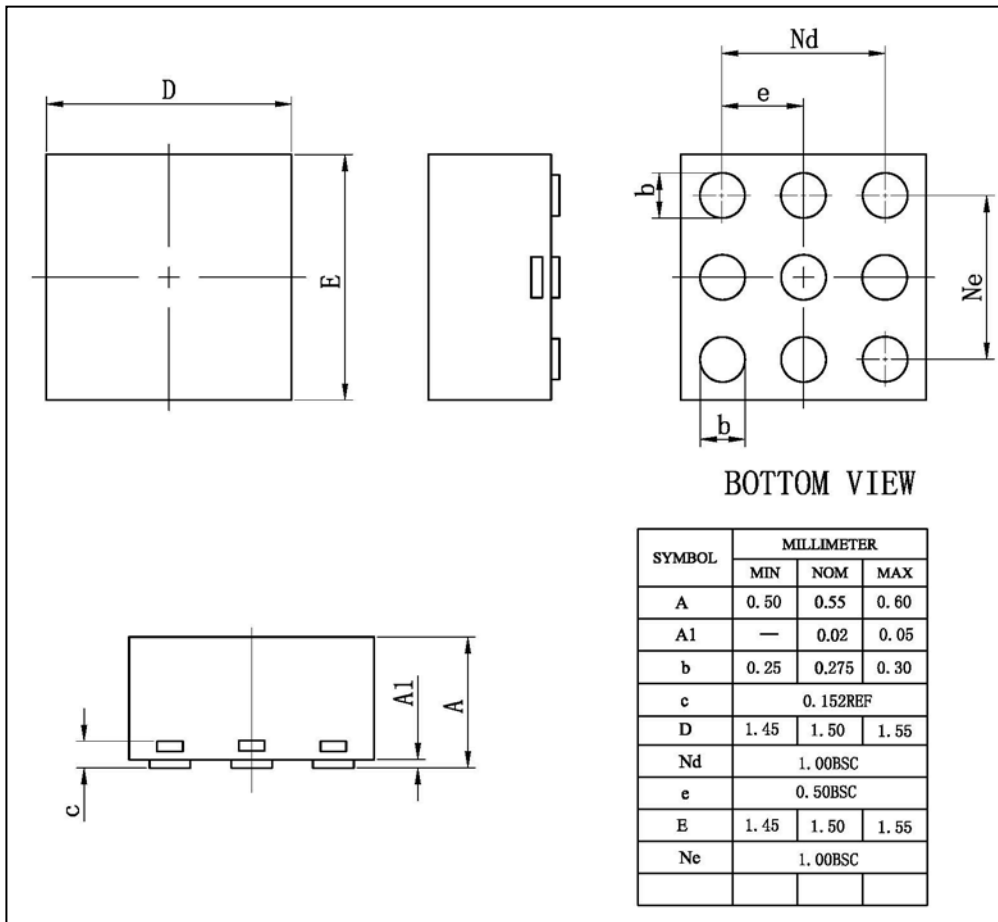


Figure 10 Classification Profile

IS31AP4990D

PACKAGING INFORMATION

UTQFN-9L



Note: All dimensions in millimeters unless otherwise stated.