



LOW INPUT VOLTAGE SYNCHRONOUS BOOST CONVERTER WITH 1.3-A SWITCHES

FEATURES

- More than 90% Efficiency at
 - 300 mA Output Current at 3.3 V (VIN \geq 2.4 V)
 - 600 mA Output Current at 5 V (VIN \geq 3 V)
- Automatic Transition between Boost Mode and Down Conversion Mode
- Device Quiescent Current less than 55 μ A
- Startup into Full Load at 0.5 V Input Voltage
- Operating Input Voltage Range from 0.3 V to 5.5 V
- Programmable Undervoltage Lockout Threshold
- Output Short Circuit Protection Under all Operating Conditions
- Fixed and Adjustable Output Voltage Options from 1.8 V to 5.5 V

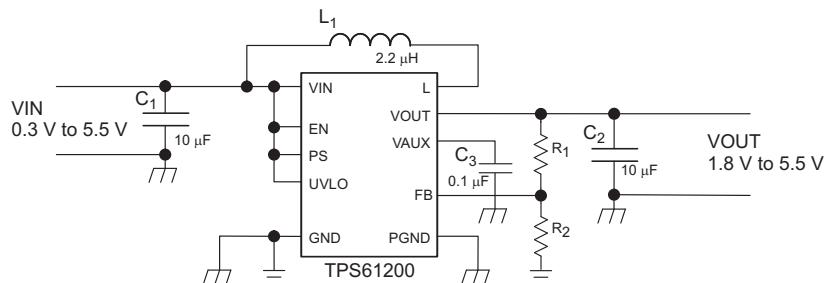
- Power Save Mode for Improved Efficiency at Low Output Power
- Forced fixed Frequency Operation possible
- Load Disconnect During Shutdown
- Overtemperature Protection
- Small 3 mm x 3 mm QFN-10 Package

APPLICATIONS

- All Single-Cell, Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products
- Fuel Cell And Solar Cell Powered Products
- Portable Audio Players
- PDAs
- Cellular Phones
- Personal Medical Products
- White LED's

DESCRIPTION

The TPS6120x devices provide a power supply solution for products powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. It is also used in fuel cell or solar cell powered devices where the capability of handling low input voltages is essential. Possible output currents are depending on the input to output voltage ratio. The devices provides output currents up to 600 mA at a 5-V output while using a single-cell Li-Ion or Li-Polymer battery, and discharge it down to 2.5 V. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters the Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average input current is limited to a value of 1500 mA. The output voltage can be programmed by an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. The device is packaged in a 10-pin QFN PowerPAD™ package (DRC) measuring 3 mm x 3 mm.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS⁽¹⁾

| T _A | OUTPUT VOLTAGE DC/DC | PACKAGE MARKING | PACKAGE ⁽²⁾ | PART NUMBER ⁽³⁾ |
|----------------|----------------------|-----------------|------------------------|----------------------------|
| –40°C to 85°C | Adjustable | BRR | 10-Pin QFN | TPS61200DRC |
| | 3.3 V | BRS | | TPS61201DRC |
| | 5 V | BRT | | TPS61202DRC |
| | 5 V | CER | | TPS61202DSC |

- (1) Contact the factory to check availability of other fixed output voltage versions.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) The DRC and the DSC package are available taped and reeled. Add R suffix to device type (e.g., TPS61200DRCR or TPS61202DSCR) to order quantities of 3000 devices per reel. It is also available in minireels. Add a T suffix to the device type (i.e. TPS61200DRCT or TPS61202DSCT) to order quantities of 250 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | TPS6120x | UNIT |
|------------------|---|------------|------|
| V _I | Input voltage range on VIN, L, VAUX, VOUT, PS, EN, FB, UVLO | –0.3 to 7 | V |
| T _J | Operating junction temperature range | –40 to 150 | °C |
| T _{stg} | Storage temperature range | –65 to 150 | °C |
| ESD | Human Body Model (HBM) ⁽²⁾ | 4 | kV |
| | Machine Model (MM) ⁽²⁾ | 200 | V |
| | Charged Device Model (CDM) ⁽²⁾ | 1.5 | kV |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) ESD testing is performed according to the respective JESD22 JEDEC standard.

DISSIPATION RATINGS TABLE

| PACKAGE | THERMAL RESISTANCE Θ _{JA} | POWER RATING T _A ≤ 25°C | DERATING FACTOR ABOVE T _A = 25°C |
|---------|------------------------------------|------------------------------------|---|
| DRC | 48.7 °C/W | 2054 mW | 21 mW/°C |

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-----------------|--|-----|-----|-----|------|
| V _{SS} | Supply voltage at VIN | 0.3 | 5.5 | 5.5 | V |
| T _A | Operating free air temperature range | –40 | 85 | 85 | °C |
| T _J | Operating virtual junction temperature range | –40 | 125 | 125 | °C |

ELECTRICAL CHARACTERISTICS

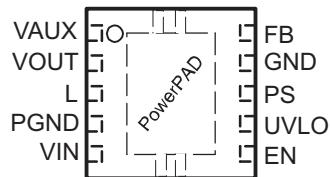
over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

| DC/DC STAGE | | | | | | | |
|-------------------|----------------------------------|--|--|------|------|------|------------------|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| V_I | Input voltage range | | | 0.3 | 5.5 | 5.5 | V |
| V_I | Minimum input voltage at startup | | | | | 0.5 | V |
| V_O | TPS61200 output voltage range | | | 1.8 | 5.5 | 5.5 | V |
| V_{FB} | TPS61200 feedback voltage | | | 495 | 500 | 505 | mV |
| V_{OUT} | TPS61201 output voltage | $V_{IN} < V_{OUT}$, PS = 1 | | 3.27 | 3.3 | 3.33 | V |
| V_{OUT} | TPS61202 output voltage | $V_{IN} < V_{OUT}$, PS = 1 | | 4.95 | 5.0 | 5.05 | V |
| f | Oscillator frequency | | | 1250 | 1650 | 1650 | kHz |
| I_{SW} | average switch current limit | $V_{OUT} = 3.3$ V | | 1200 | 1350 | 1500 | mA |
| | Rectifying switch on resistance | $V_{OUT} = 3.3$ V | | | 180 | | $\text{m}\Omega$ |
| | Main switch on resistance | $V_{OUT} = 3.3$ V | | | 150 | | $\text{m}\Omega$ |
| | Line regulation | $V_{IN} < V_{OUT}$, PS = 1 | | | 0.1% | 0.5% | |
| | Load regulation | $V_{IN} < V_{OUT}$, PS = 1 | | | 0.1% | 0.5% | |
| Quiescent current | V_{IN} | $I_O = 0$ mA, $V_{EN} = V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V, $V_{AUX} = 3.3$ V PS = 0 | | 1 | 2 | 2 | μA |
| | V_{OUT} | | | 50 | 70 | 70 | μA |
| | V_{AUX} | | | 4 | 6 | 6 | μA |
| Shutdown current | V_{IN} | $V_{EN} = 0$ V, $V_{IN} = 1.2$ V | | 0.5 | 1.5 | 1.5 | μA |
| | V_{AUX} | | | 1 | 2 | 2 | μA |
| | Leakage current into L | $V_{EN} = 0$ V, $V_{IN} = 1.2$ V, $V_L = 1.2$ V | | | 0.01 | 1 | μA |

| CONTROL STAGE | | | | | | | |
|----------------------|---|--|--|---------------------|---------------------|-----|---------------|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| V_{AUX} | Auxiliary Output Voltage | | | 2.4 | 5.5 | 5.5 | V |
| V_{IL} | EN input low voltage | $V_{IN} < 0.8$ V | | | 0.1 $\times V_{IN}$ | | V |
| V_{IH} | EN input high voltage | $V_{IN} < 0.8$ V | | 0.9 $\times V_{IN}$ | | | V |
| V_{IL} | EN input low voltage | $0.8 \text{ V} \leq V_{IN} \leq 1.5$ V | | | 0.2 $\times V_{IN}$ | | V |
| V_{IH} | EN input high voltage | $0.8 \text{ V} \leq V_{IN} \leq 1.5$ V | | 0.8 $\times V_{IN}$ | | | V |
| V_{IL} | EN input low voltage | $V_{IN} > 1.5$ V | | | 0.4 | 0.4 | V |
| V_{IH} | EN input high voltage | $V_{IN} > 1.5$ V | | 1.2 | | | V |
| V_{IL} | PS input low voltage | | | | 0.4 | 0.4 | V |
| V_{IH} | PS input high voltage | | | 1.2 | | | V |
| EN, PS input current | | Clamped on GND or V_{IN} ($V_{IN} < 1.5$ V) | | 0.01 | 0.1 | 0.1 | μA |
| V_{UVLO} | Undervoltage lockout threshold for turn off | V_{UVLO} decreasing | | 235 | 250 | 265 | mV |
| V_{UVLO} | Undervoltage lockout threshold for turn on | V_{UVLO} increasing | | 330 | 350 | 370 | mV |
| | UVLO input current | $V_{UVLO} = 0.5$ V | | | 0.3 | 0.3 | μA |
| | Overvoltage protection threshold | | | 5.5 | 7 | 7 | V |
| | Overtemperature protection | | | 140 | | | °C |
| | Overtemperature hysteresis | | | 20 | | | °C |

PIN ASSIGNMENTS

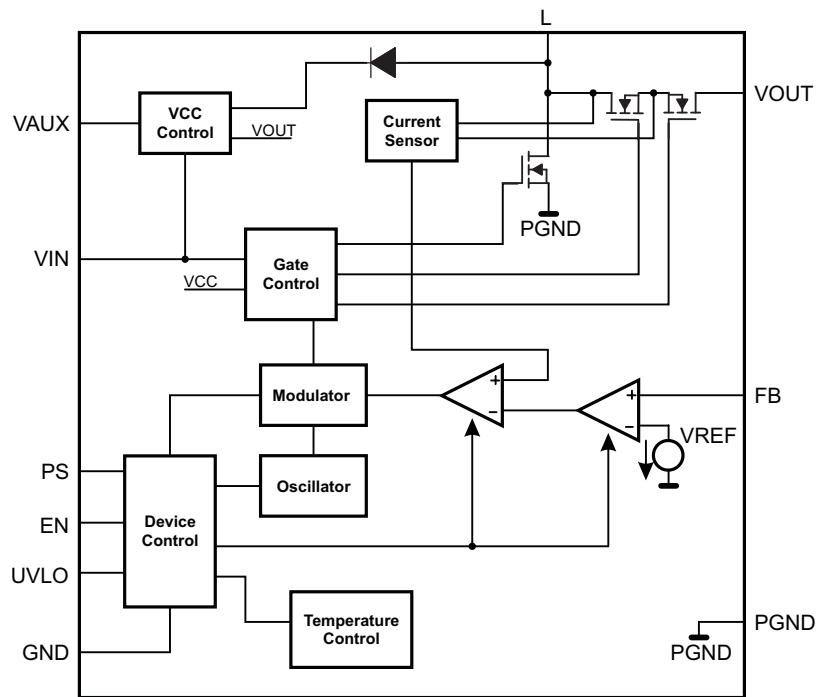
DRC PACKAGE
(TOP VIEW)



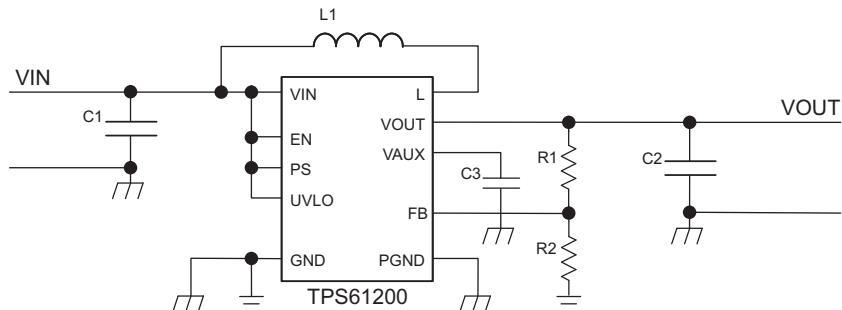
Terminal Functions

| TERMINAL NAME | | I/O | DESCRIPTION |
|------------------------|-----|-----|--|
| NAME | NO. | | |
| EN | 6 | I | Enable input (1: enabled, 0: disabled). |
| FB | 10 | I | Voltage feedback of adjustable versions, must be connected to V_{OUT} at fixed output voltage versions |
| GND | 9 | | Control / logic ground |
| PS | 8 | I | Enable/disable Power Save mode (1 : disabled, 0: enabled) |
| L | 3 | I | Connection for Inductor |
| UVLO | 7 | I | Undervoltage lockout comparator input, must be connected to VAUX if not used |
| PGND | 4 | | Power ground |
| VIN | 5 | I | Boost converter input voltage |
| VOUT | 2 | O | Boost converter output |
| VAUX | 1 | O/I | Supply voltage for control stage |
| PowerPAD TM | | | Must be soldered to achieve appropriate power dissipation. Should be connected to PGND. |

FUNCTIONAL BLOCK DIAGRAM (TPS61200)



PARAMETER MEASUREMENT INFORMATION



List of Components:

| COMPONENT REFERENCE | PART NUMBER | MANUFACTURER | VALUE |
|---------------------|---------------|--------------|-----------------------------|
| C1 | | any | 10 μ F, X7R Ceramic |
| C2 | | any | 2 x 10 μ F, X7R Ceramic |
| L1 | LPS3015-222ML | Coilcraft | 2.2 μ H |

TYPICAL CHARACTERISTICS

Table of Graphs

| | | FIGURE |
|------------------------|---|--------|
| Maximum output current | vs Input voltage | 1 |
| Efficiency | vs Output current (TPS61200), Power Save Enabled | 2 |
| | vs Output current (TPS61200), Power Save Disabled | 3 |
| | vs Output current (TPS61201), Power Save Enabled | 4 |
| | vs Output current (TPS61201), Power Save Disabled | 5 |
| | vs Output current (TPS61202), Power Save Enabled | 6 |
| | vs Output current (TPS61202), Power Save Disabled | 7 |
| | vs Input voltage (TPS61201), Power Save Enabled | 8 |
| | vs Input voltage (TPS61201), Power Save Disabled | 9 |
| | vs Input voltage (TPS61202), Power Save Enabled | 10 |
| | vs Input voltage (TPS61202), Power Save Disabled | 11 |
| Output voltage | vs Output current (TPS61201) | 12 |
| | vs Output current (TPS61202) | 13 |
| Waveforms | Output Voltage TPS61201, Power Save Mode Disabled | 14 |
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| | TPS61202 Load Transient Response | 19 |
| | TPS61201 Line Transient Response | 20 |
| | TPS61202 Line Transient Response | 21 |
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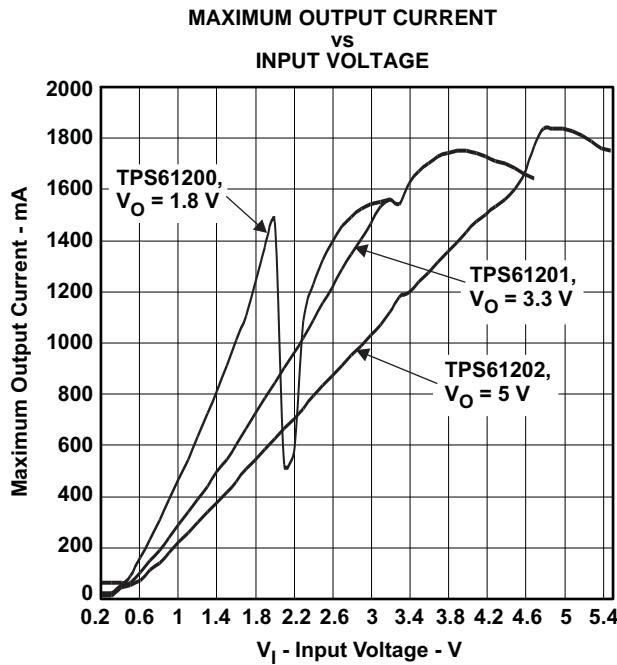


Figure 1.

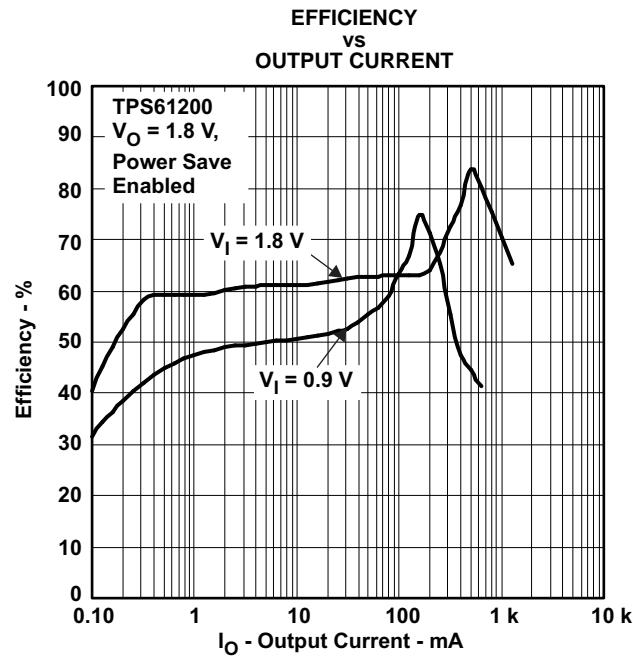


Figure 2.

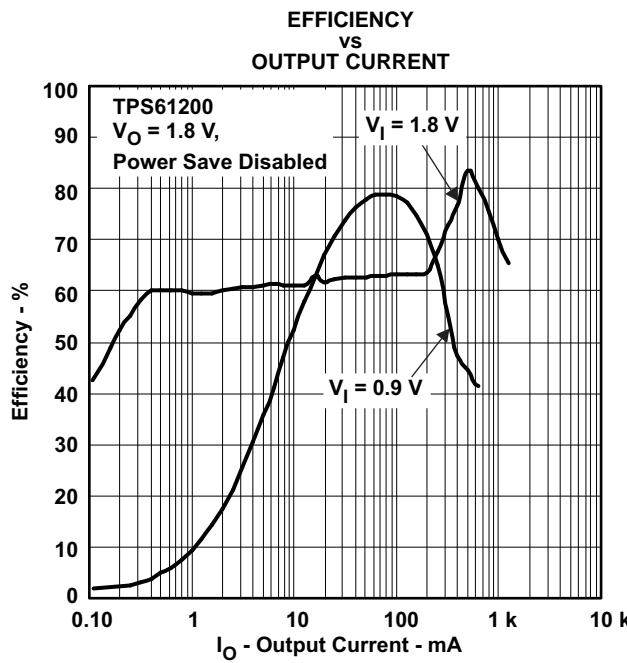


Figure 3.

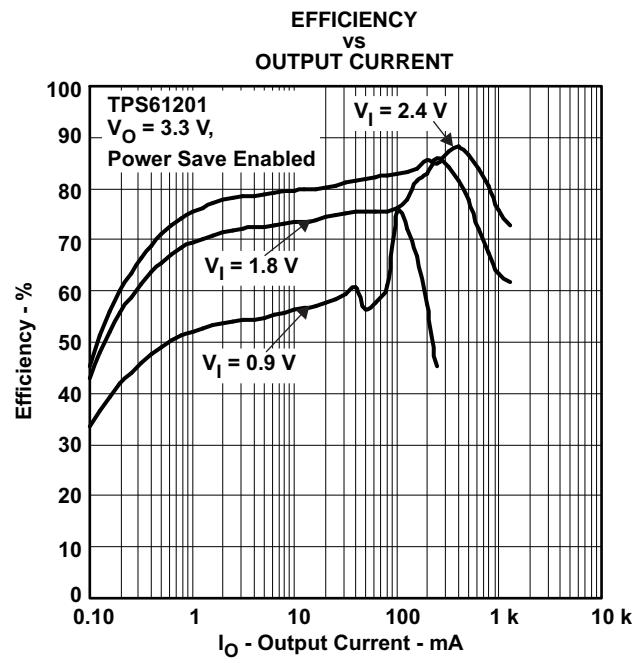


Figure 4.

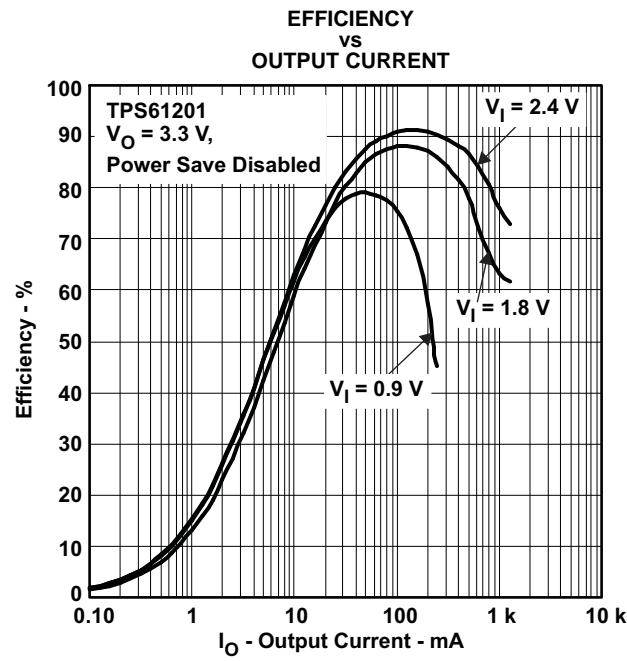


Figure 5.

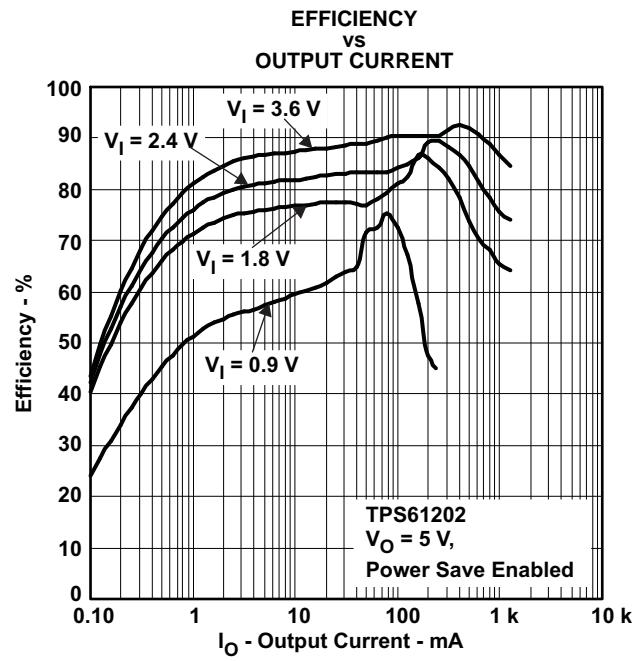


Figure 6.

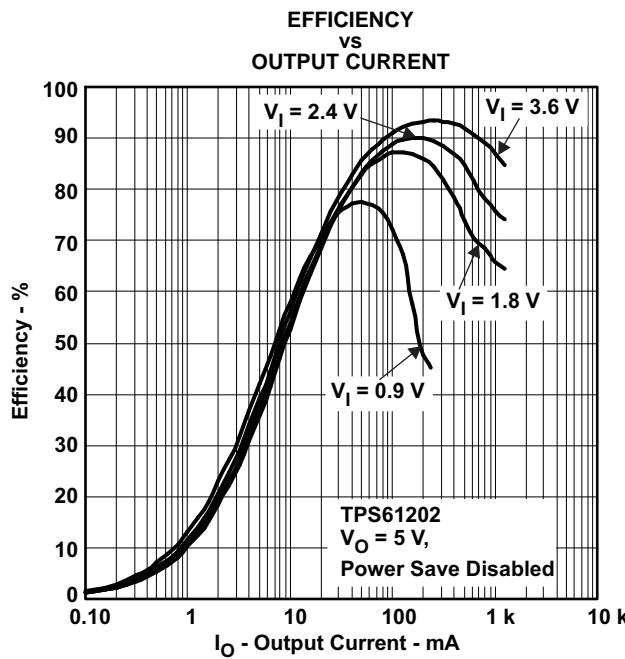


Figure 7.

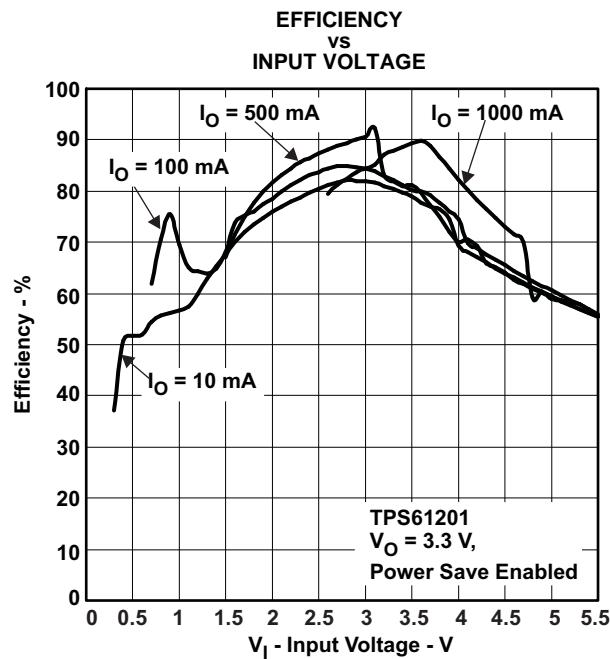


Figure 8.

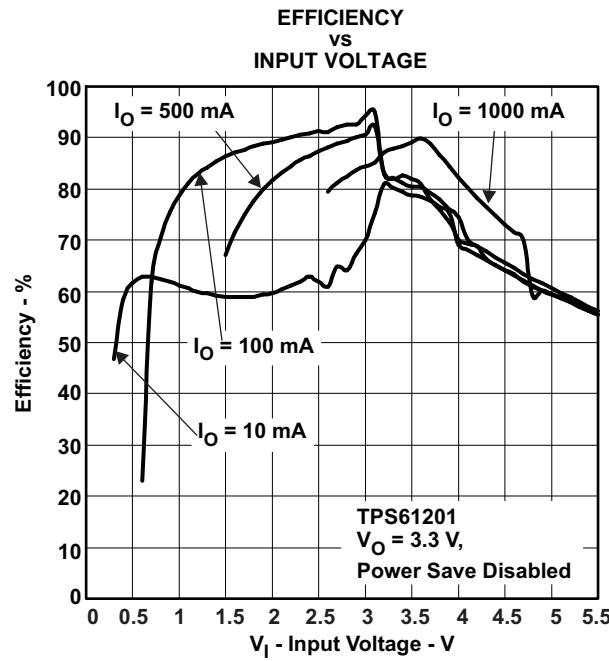


Figure 9.

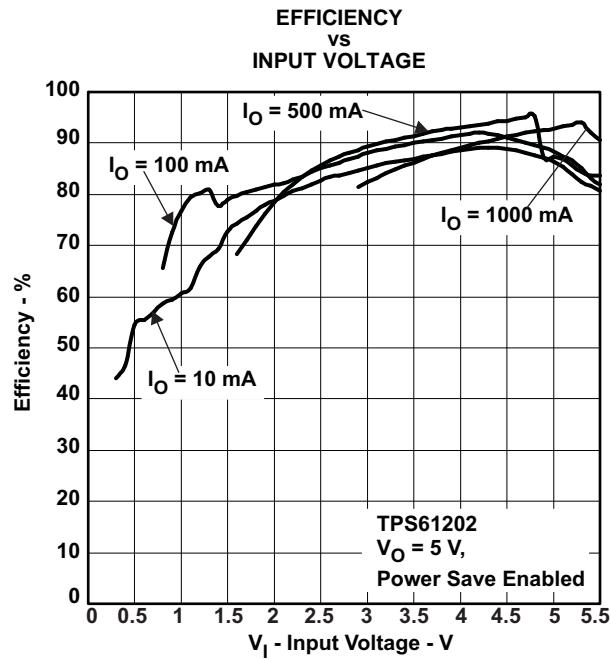


Figure 10.

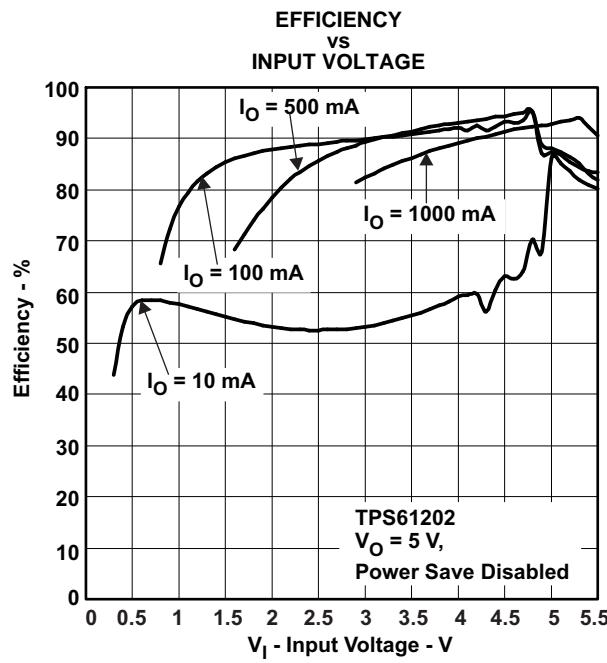


Figure 11.

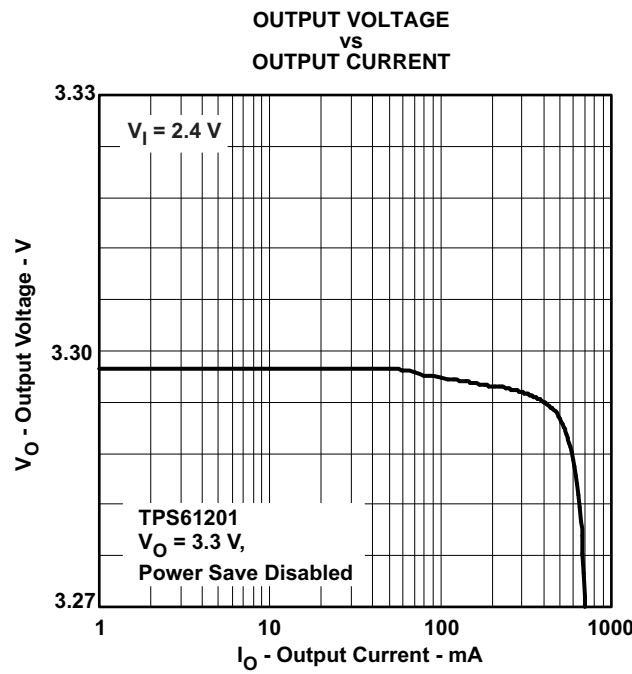


Figure 12.

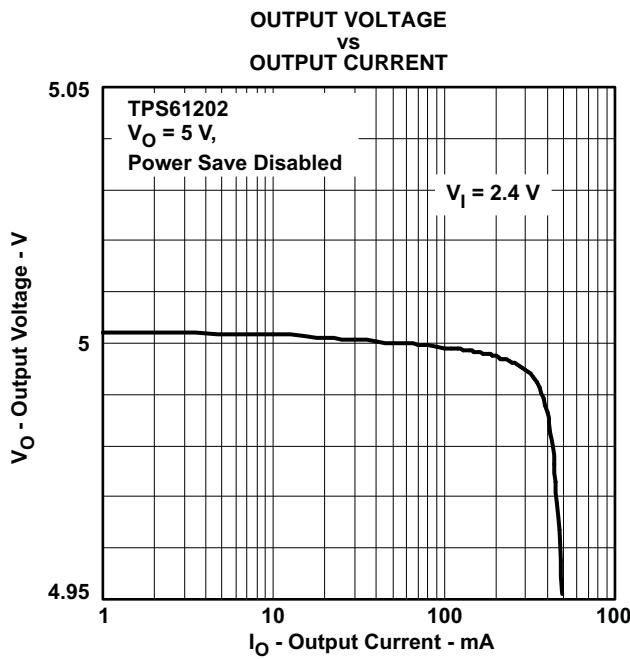


Figure 13.

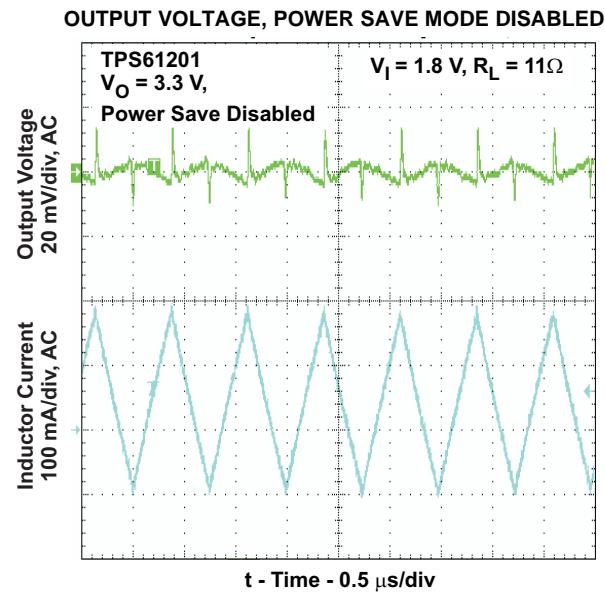


Figure 14.

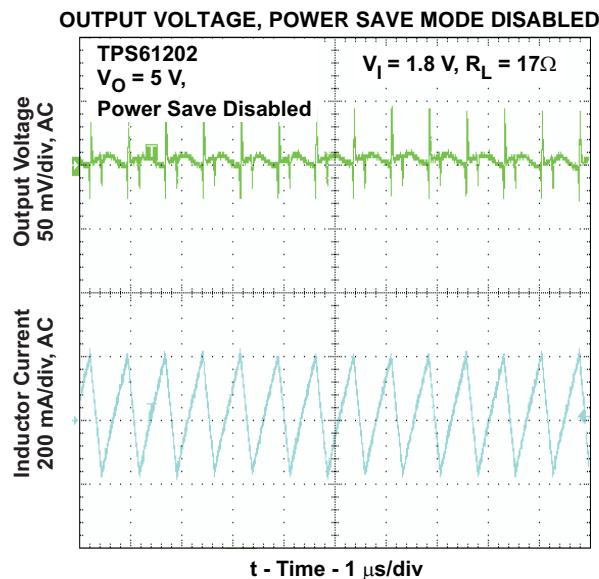


Figure 15.

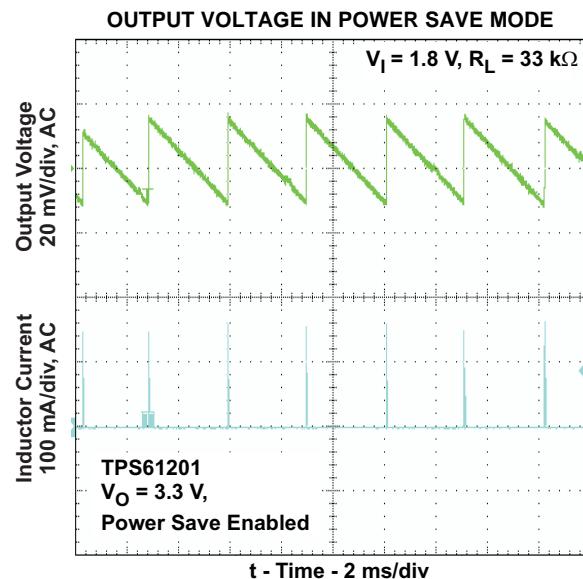


Figure 16.

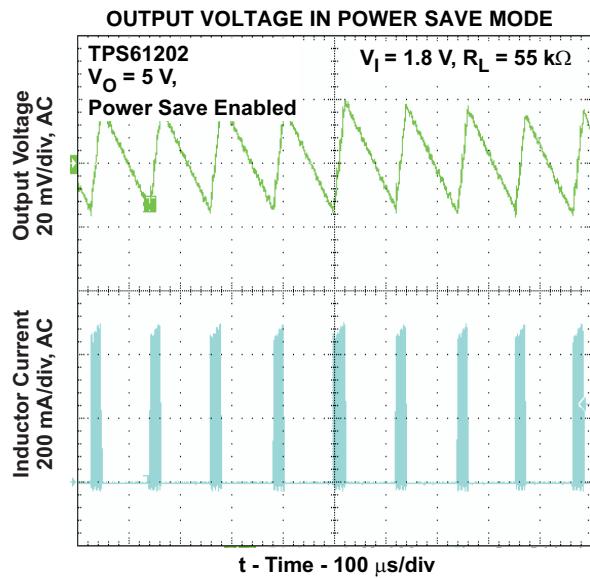


Figure 17.

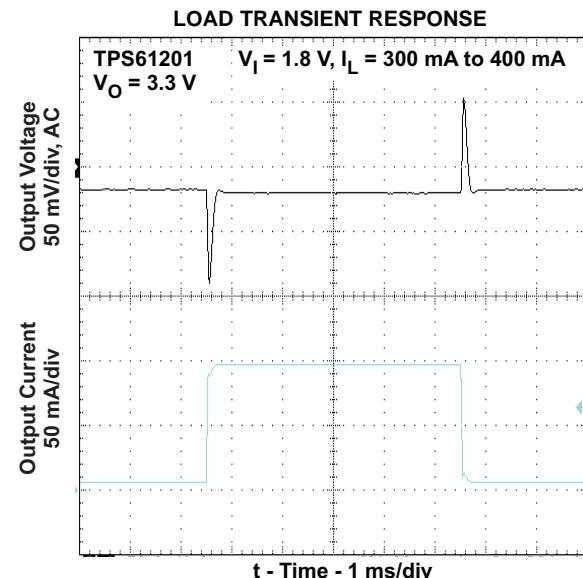


Figure 18.

LOAD TRANSIENT RESPONSE

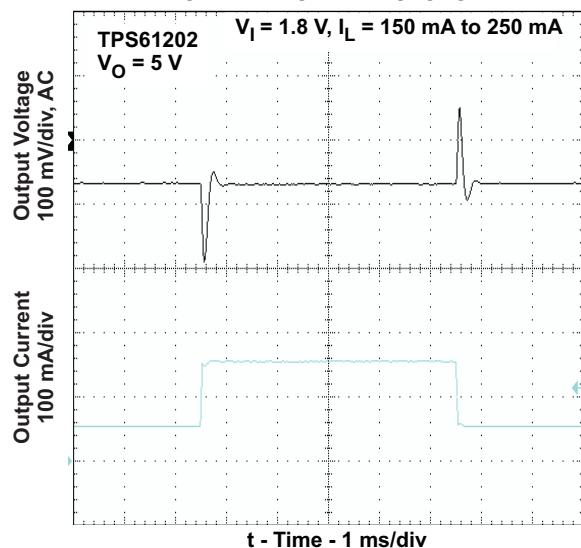


Figure 19.

LINE TRANSIENT RESPONSE

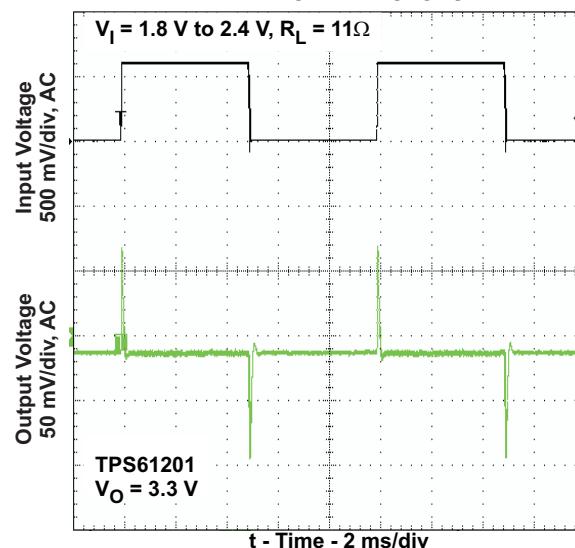


Figure 20.

LINE TRANSIENT RESPONSE

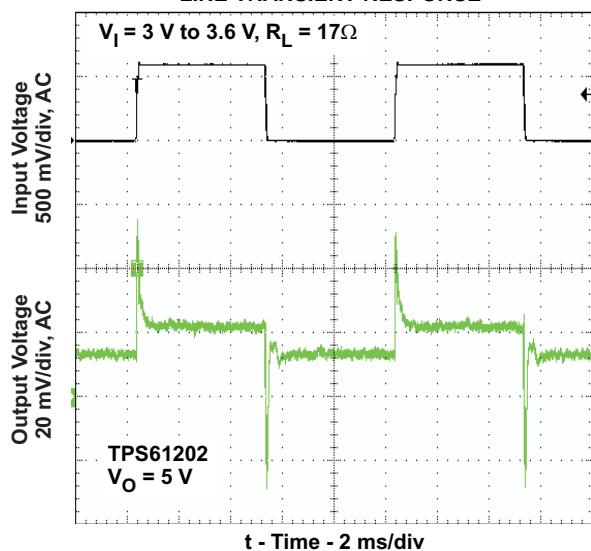


Figure 21.

START-UP AFTER ENABLE

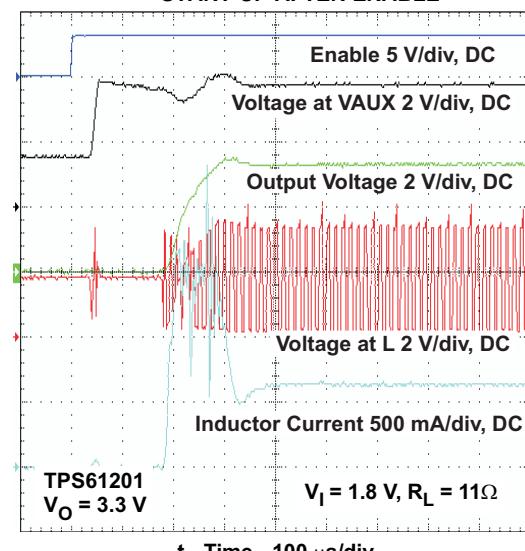


Figure 22.

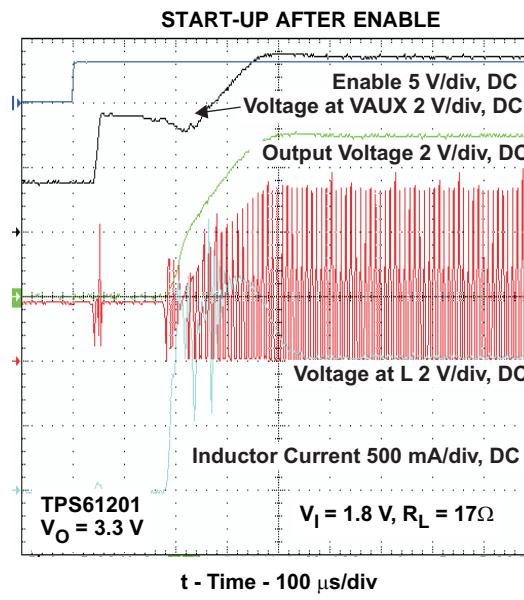


Figure 23.

DETAILED DESCRIPTION

CONTROLLER CIRCUIT

The controlling circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and can immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. For adjustable output voltages, a resistive voltage divider must be connected to that pin. For fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current as well as the peak input current. Thus, the maximum input power is controlled as well as the maximum peak current to achieve a safe and stable operation under all possible conditions. To protect the device from overheating, an internal temperature sensor is implemented.

Synchronous Operation

The device uses three internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point ideally close to the GND pin. Due to the 3-switch topology, the load is always disconnected from the input during shutdown of the converter.

Down Regulation

A boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. For example, it is able to regulate 3 V at the output with two fresh alkaline cells at the input having a total cell voltage of 3.2 V. Another example is powering white LEDs with a forward voltage of 3.6 V from a fully charged Li-Ion cell with an output voltage of 4.2 V. To control these applications properly, a Down Conversion mode is implemented.

If the input voltage reaches or exceeds the output voltage, the converter automatically changes to a Down Conversion mode. In this mode, the control circuit changes the behavior of the two rectifying switches. While continuing switching it sets the voltage drop across the rectifying switches as high as needed to regulate the output voltage. This means the power losses in the converter increase. This must be taken into account for thermal consideration.

Power Save Mode

The Power Save (PS) pin can be used to select different operation modes. To enable Power Save mode the PS pin must be set low. Power Save mode is used to improve efficiency at light load. If Power Save mode is enabled, the converter stops operating if the average inductor current decreases below about 300 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter stops operating once the conditions for stopping operation are met again.

The Power Save mode can be disabled by programming high at the PS pin. In Down Conversion mode, Power Save mode is always enabled and the device cannot be forced into fixed frequency operation at light loads. The PS input supports standard logic thresholds.

Device Enable

The device is put into operation when EN is set high. It is put into a Shutdown mode when EN is set to GND. In Shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Softstart and Short-Circuit Protection

After being enabled, the device starts operating. At first it keeps the main output VOUT disconnected, and charges the capacitor at VAUX. If the capacitor at VAUX is charged to about 2.5 V, the device switches to normal operation. This means VOUT is turned on and the capacitor at VOUT is charged while the load connected to the device is supplied. To ramp up the output voltage in a controlled way, the average current limit is set to 400 mA and rise proportional to the increase of the output voltage. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short-circuit at the output, and keeps the current limit low to protect itself and the application. When there is a short at the output during operation, the current limit is decreased accordingly.

Undervoltage Lockout

An undervoltage lockout function prevents the main output at VOUT from being supplied if the voltage at UVLO drops below 0.25 V. When using a resistive divider at the voltage to be monitored, for example the supply voltage, any threshold for the monitored voltage can be programmed. If in undervoltage lockout mode, the device still maintains its supply voltage at VAUX, but it is not turned off until EN is programmed low. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6120x DC/DC converters are intended for systems powered by a single up to triple cell Alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.7 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion or Li-Polymer with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source like solar cells or fuel cells with a typical output voltage between 0.3 V and 5.5 V can power systems where the TPS6120x is used.

Programming the Output Voltage

Within the TPS6120X family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. At the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μ A, and the voltage across the resistor between FB and GND, R_2 , is typically 500 mV. Based on those two values, the recommended value for R_2 should be lower than 500 k Ω , in order to set the divider current at 1 μ A or higher. It is recommended to keep the value for this resistor in the range of 200 k Ω . The value of the resistor connected between VOUT and FB, R_1 , depending on the needed output voltage (V_{OUT}), can be calculated using [Equation 1](#):

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-M Ω resistor should be chosen for R_1 when for R_2 a 180-k Ω has been selected.

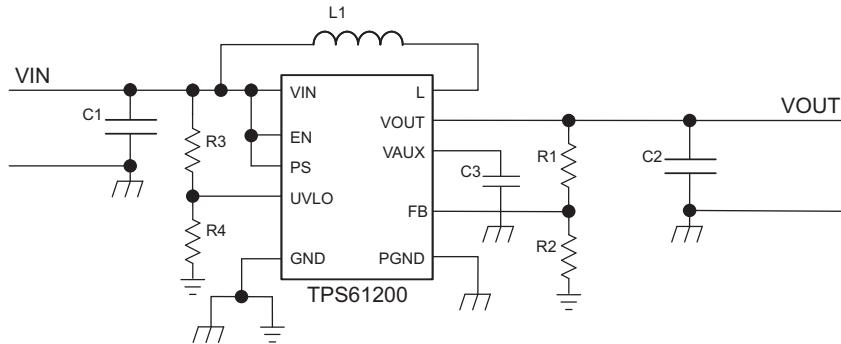


Figure 24. Typical Application Circuit for Adjustable Output Voltage Option

Programming the UVLO Threshold Voltage

The UVLO input can be used to shut down the main output if the supply voltage is getting too low. The internal reference threshold is typically 250 mV. If the supply voltage should cause the shutdown when it is dropping below 250 mV, it can be connected directly to the UVLO pin. If the shutdown has already happen at higher voltages, a resistor divider can be used. R3 and R4 in [Figure 24](#) show an example of how to monitor the input voltage of the circuit. The current through the resistive divider should be about 100 times greater than the current into the UVLO pin. The typical current into the UVLO pin is 0.01 μ A, and the voltage across R4 is equal to the UVLO voltage threshold that is generated on-chip, which has a value of 250 mV. The recommended value for R4 is; therefore, in the range of 250 k Ω . From this, the value of resistor R3, depending on the desired shutdown voltage V_{INMIN} , can be calculated using [Equation 2](#).

$$R3 = R4 \times \left(\frac{V_{INMIN}}{V_{UVLO}} - 1 \right) \quad (2)$$

Inductor Selection

To make sure that the TPS6120X devices can operate, an inductor must be connected between pin VIN and pin L. To estimate the minimum inductance value [Equation 3](#) can be used.

$$L_{MIN} = V_{IN} \times 0.5 \frac{\mu\text{s}}{\text{A}} \quad (3)$$

In [Equation 3](#), the minimum inductance, L_{MIN} , for boost mode operation is calculated. V_{IN} is the maximum input voltage. The recommended inductor value range is between 1.5 μH and 4.7 μH . The minimum inductor value should not be below 1.5 μH , even if [Equation 3](#) yields in something lower. Using 2.2 μH is recommended anyway for getting best performance over the whole input and output voltage range.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. [Equation 4](#) shows how to calculate the peak current I .

$$I_{LMAX} = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times V_{OUT} \times f \times L} \quad (4)$$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. The following inductor series from different suppliers have been used with TPS6120x converters:

Table 1. List of Inductors

| VENDOR | INDUCTOR SERIES |
|------------------|-----------------|
| Coilcraft | LPS3015 |
| | LPS4012 |
| Murata | LQH3NP |
| Tajo Yuden | NR3015 |
| Wurth Elektronik | WE-TPC Typ S |

Capacitor Selection

Input Capacitor

At least a 4.7 μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

To get an estimate of the recommended minimum output capacitance, [Equation 5](#) can be used.

$$C_{OUT} = 5 \times L \times \frac{\mu\text{F}}{\mu\text{H}} \quad (5)$$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Capacitor at VAUX

Between the VAUX pin and GND a capacitor must be connected. This capacitor is used to maintain and filter the control supply voltage. It is charged during startup and before the main output VOUT is turned on. To ensure stable operation, using at least $0.1\mu\text{F}$ is recommended. At output voltages below 2.5 V, the capacitance should be in the range of $1\mu\text{F}$. Since this capacitor is also used as a snubber capacitor for the main switch, using a ceramic capacitor with low ESR is important.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6120x devices is 125°C . The thermal resistance of the 10-pin QFN 3×3 package (DRC) is $R_{\theta JA} = 48.7\text{ }^\circ\text{C/W}$, if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C . Therefore, the maximum power dissipation is about 820 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125^\circ\text{C} - 85^\circ\text{C}}{48.7\text{ }^\circ\text{C/W}} = 820\text{ mW} \quad (6)$$

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS61200DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61200DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61200DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61200DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61201DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61201DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61201DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61201DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DSCR | ACTIVE | SON | DSC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DSCRG4 | ACTIVE | SON | DSC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DSCT | ACTIVE | SON | DSC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS61202DSCTG4 | ACTIVE | SON | DSC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

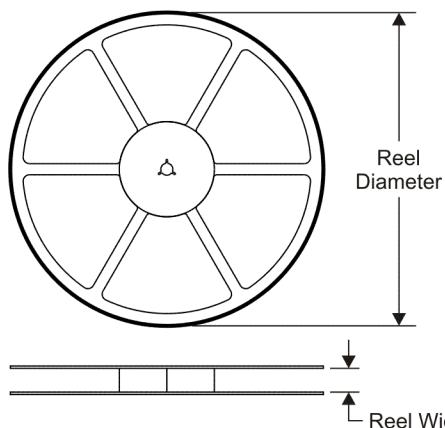
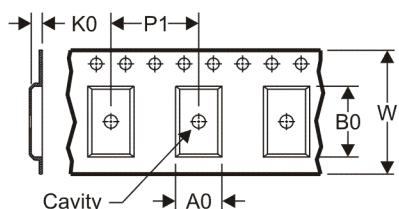
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

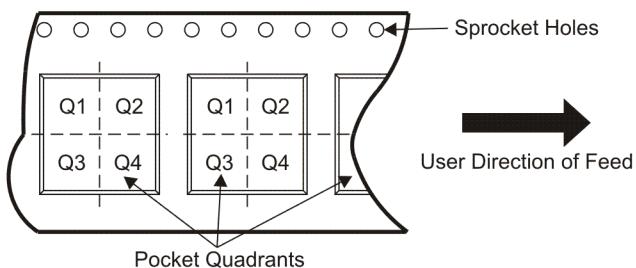
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61200DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61200DRCT | SON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61201DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61201DRCT | SON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61202DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61202DRCT | SON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61202DSCR | SON | DSC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61202DSCT | SON | DSC | 10 | 250 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

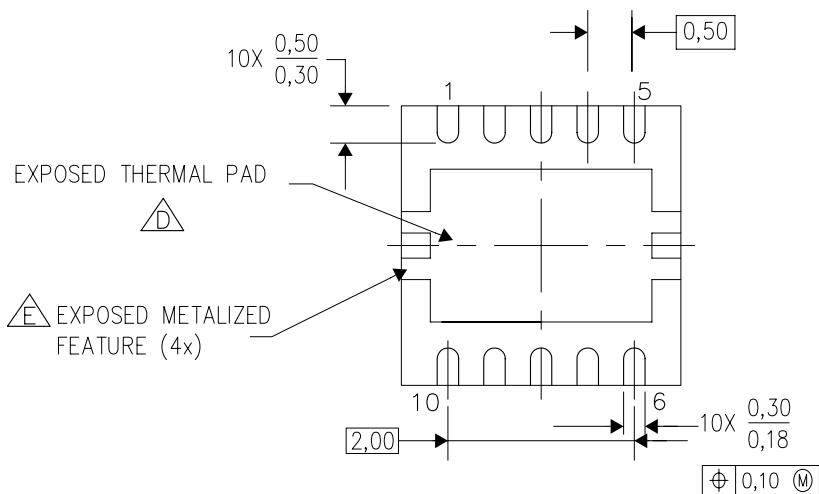
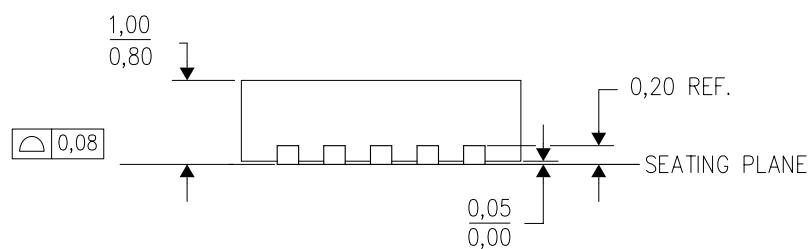
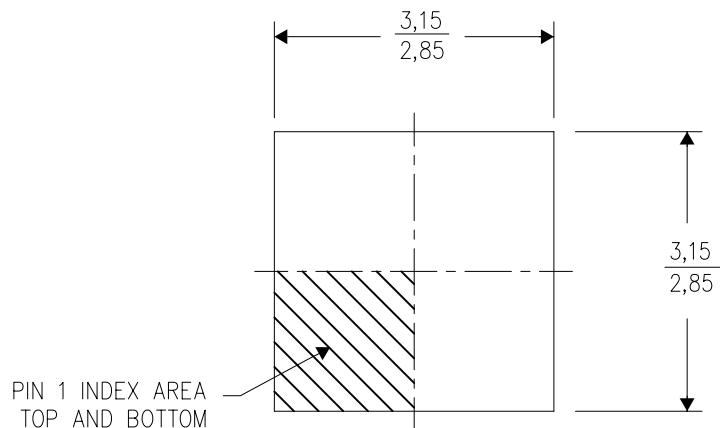

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61200DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61200DRCT | SON | DRC | 10 | 250 | 190.5 | 212.7 | 31.8 |
| TPS61201DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61201DRCT | SON | DRC | 10 | 250 | 190.5 | 212.7 | 31.8 |
| TPS61202DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61202DRCT | SON | DRC | 10 | 250 | 190.5 | 212.7 | 31.8 |
| TPS61202DSCR | SON | DSC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61202DSCT | SON | DSC | 10 | 250 | 346.0 | 346.0 | 29.0 |

MECHANICAL DATA

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102/G 06/08

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Small Outline No-Lead (SON) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

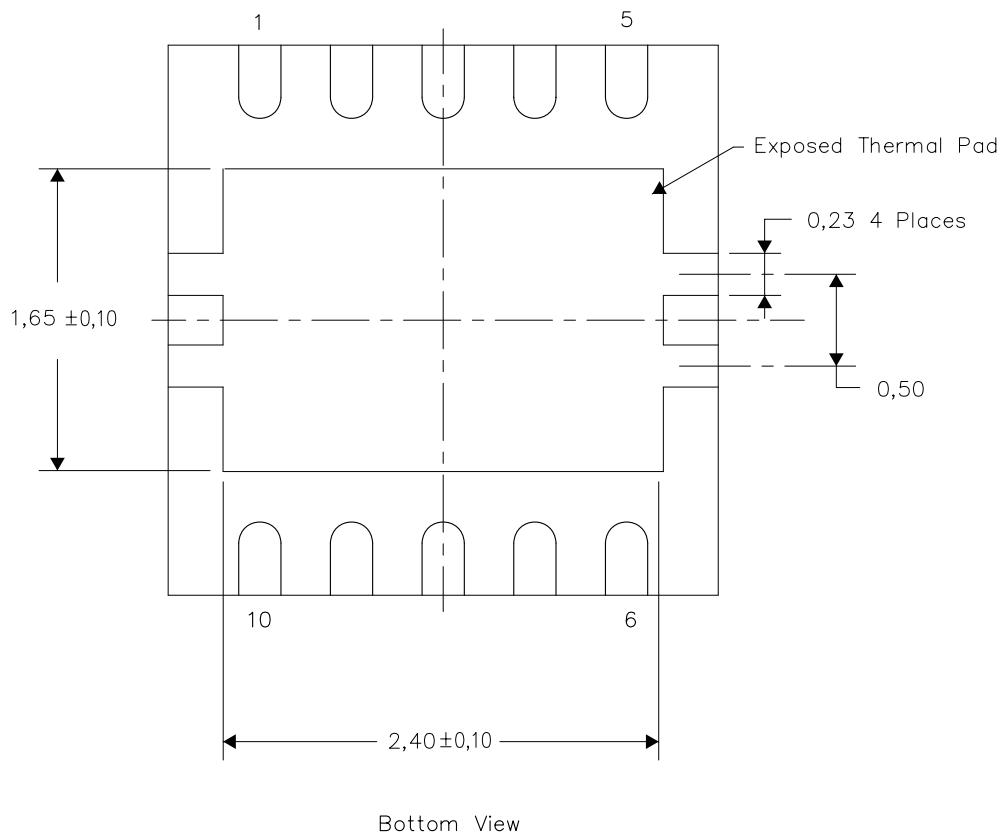
 Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

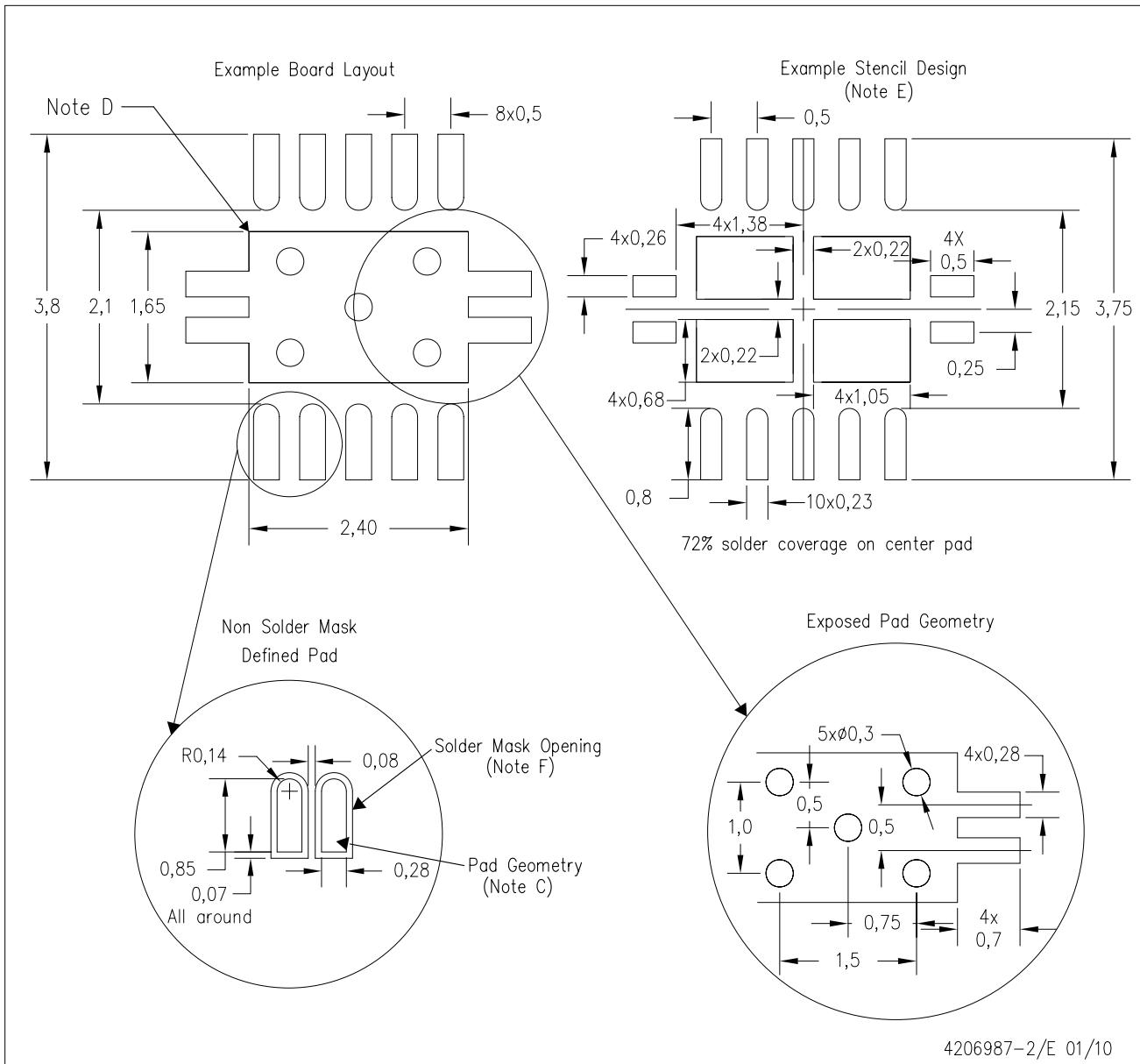


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S-PVSON-N10)



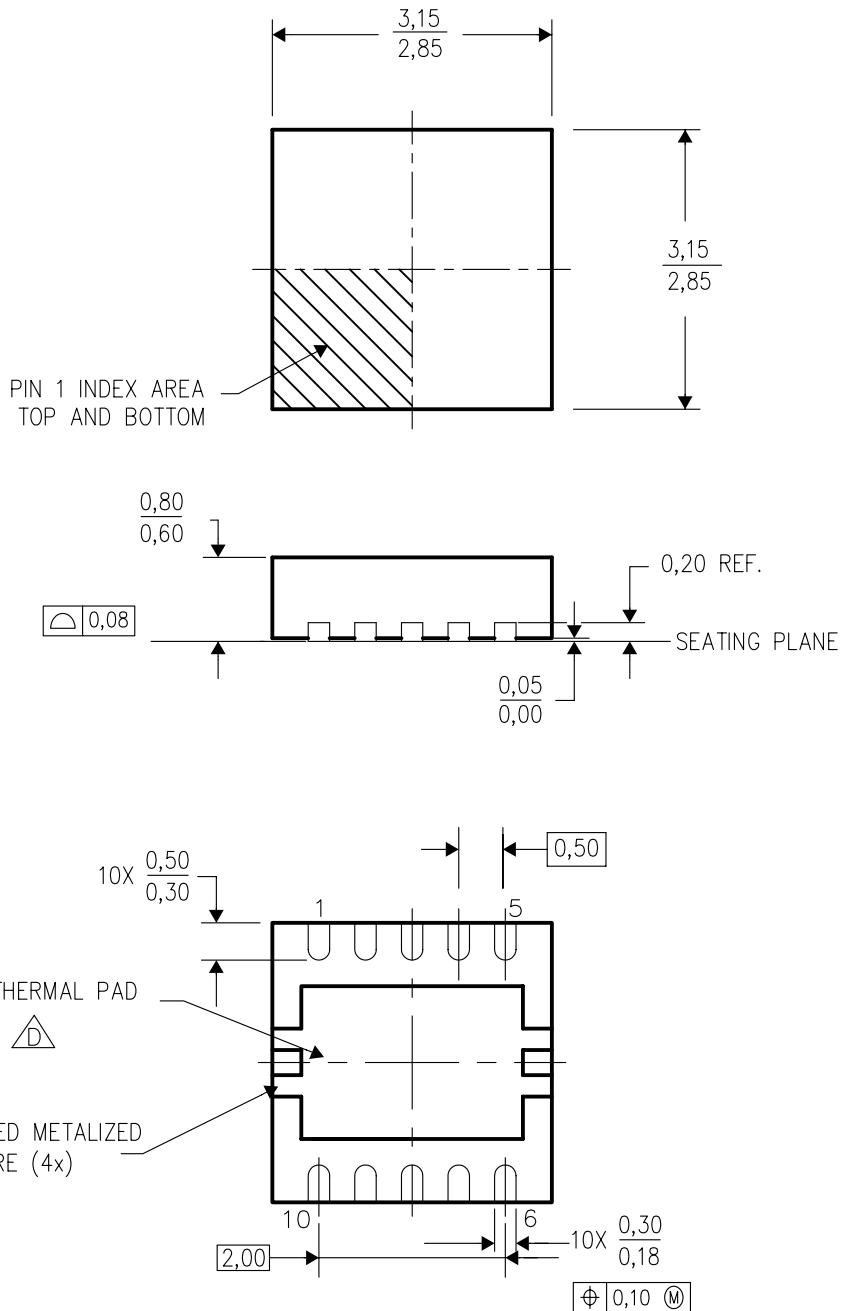
4206987-2/E 01/10

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DSC (S-PDSO-N10)

PLASTIC SMALL OUTLINE



4207383/B 06/06

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Small Outline No-Lead (SON) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

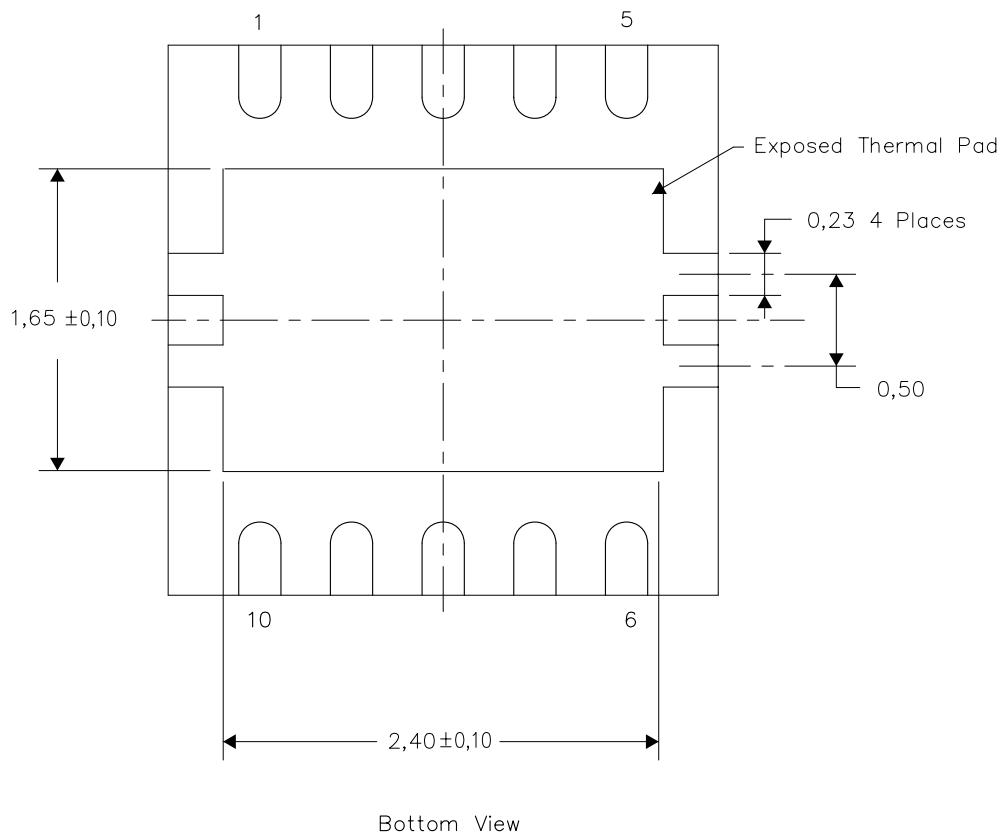
 Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

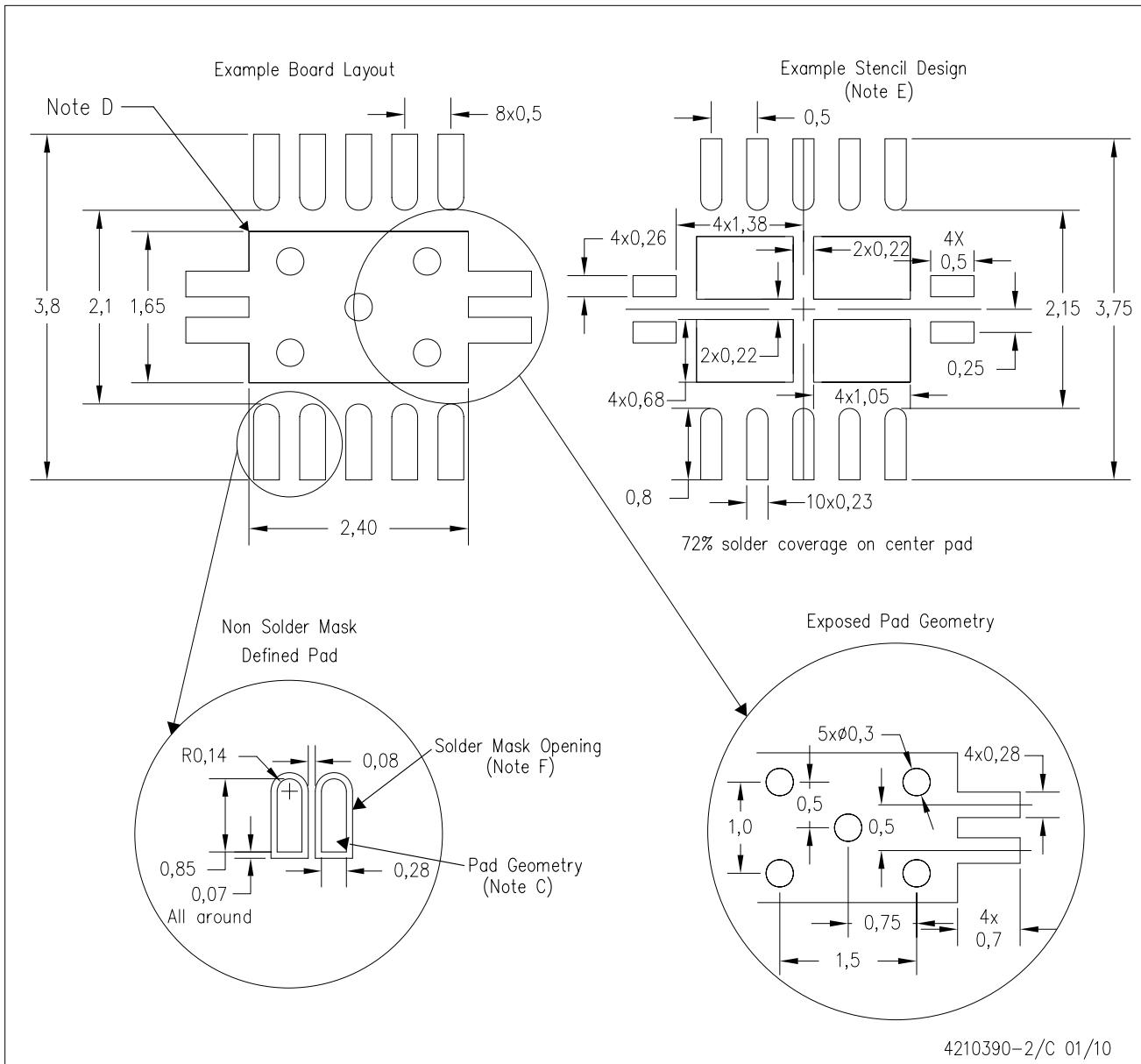


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DSC (S-PVSON-N10)



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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