HSDL-3602

IrDA® Data 1.4 Compliant 4 Mb/s 3V Infrared Transceiver

Data Sheet

Description

The HSDL-3602 is a low profile infrared transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data link. The module is compliant to IrDA Data Physical Layer Specifications 1.4 and IEC825-Class 1 Eye Safety Standard.

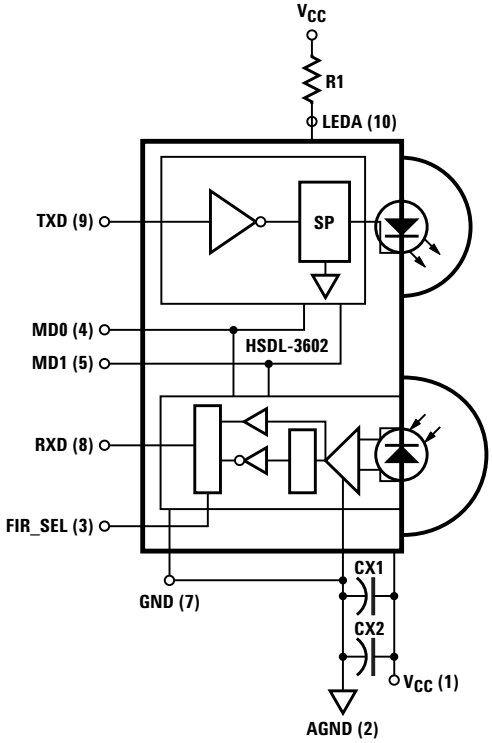
The HSDL-3602 contains a high-speed and high-efficiency 870 nm LED, a silicon PIN diode, and an integrated circuit. The IC contains an LED driver and a receiver providing a single output (RXD) for all data rates supported.

Applications

- Digital imaging
  - — Digital still cameras
  - — Photo-imaging printers
- Data communication
  - — Notebook computers
  - — Desktop PCs
  - — Win CE handheld products
  - — Personal Digital Assistants (PDAs)
  - — Printers
  - — Fax machines, photocopiers
  - — Screen projectors
  - — Auto PCs
  - — Dongles
  - — Set-top box
- Telecommunication products
  - — Cellular phones
  - — Pagers
- Small industrial and medical instrumentation
  - — General data collection devices
  - — Patient and pharmaceutical data collection devices
- IR LANs

Features

- Fully compliant to IrDA 1.1 specifications:
  - — 9.6 kb/s to 4 Mb/s operation
  - — Excellent nose-to-nose operation
- Typical link distance > 1.5 m
- IEC825-Class 1 eye safe
- Wide operating voltage range — 2.7 V to 3.6 V
- Small module size — 4.0 x 12.2 x 4.9 mm (H x W x D)
- Complete shutdown — TXD, RXD, PIN diode
- Low shutdown current — 10 nA typical
- Adjustable optical power management — Adjustable LED drive-current to maintain link integrity
- Single Rx data output — FIR select pin switch to FIR
- Integrated EMI shield — Excellent noise immunity
- Edge detection input — Prevents the LED from long turn-on time
- Interface to various super I/O and controller devices
- Designed to accommodate light loss with cosmetic window
- Only 2 external components are required
- Lead free package



HSDL-3602 Functional block diagram

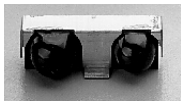
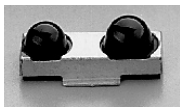
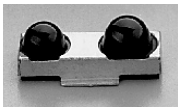
The HSDL-3602 can be completely shut down to achieve very low power consumption. In the shut down mode, the PIN diode is inactive, thus producing very little photo-current even under very bright ambient light. The HSDL-3602 also incorporates the capability for adjustable optical power. With two programming pins; MODE 0 and MODE 1, the optical power output can be adjusted lower when the nominal desired link distance is one-third or two-third of the full IrDA link.

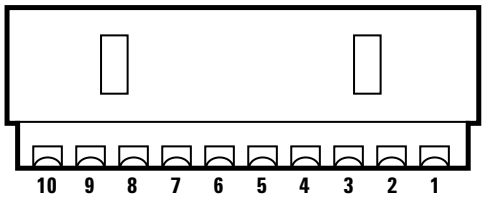
The HSDL-3602 comes with a front view packaging option (HSDL-3602-007/-037) and a top view packaging option (HSDL-3602-008/-038). It has an integrated shield that helps to ensure low EMI emission and high immunity to EMI field, thus enhancing reliable performance.

Application Support Information

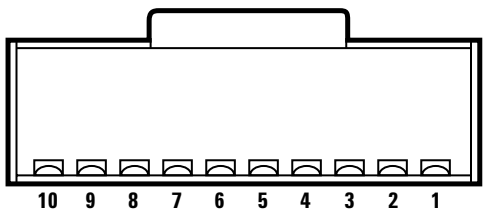
The Application Engineering group in Avago Technologies is available to assist you with the Technical understanding associated with HSDL-3602 infrared transceiver module. You can contact them through your local Avago Technologies' sales representatives for additional details.

Ordering Information

Package Option	Package	Part Number	Standard Package Increment
	Front View	HSDL-3602-007	400
	Front View	HSDL-3602-037	1800
	Top View	HSDL-3602-008	400
	Top View	HSDL-3602-038	1800



Back view (HSDL-3602-007/-037)



Bottom view (HSDL-3602-008/-038)

I/O Pins Configuration Table

Pin	Description	Symbol
1	Supply Voltage	V_{CC}
2	Analog Ground	AGND
3	FIR Select	FIR_SEL
4	Mode 0	MD0
5	Mode 1	MD1
6	No Connection	NC
7	Ground	GND
8	Receiver Data Output	RXD
9	Transmitter Data Output	TXD
10	LED Anode	LEDA

Transceiver Control Truth Table

Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

X = Don't Care

Transceiver I/O Truth Table

		Inputs		Outputs	
Transceiver Mode	**FIR_SEL**	**TXD**	**EI**	**LED**	**RXD**
Active	X	1	X	On	Not Valid
Active	0	0	High[1]	Off	Low[3]
Active	1	0	High[2]	Off	Low[3]
Active	X	0	Low	Off	High
Shutdown	X	X[4]	Low	Not Valid	Not Valid

X = Don't Care EI = In-Band Infrared Intensity at detector

Notes:

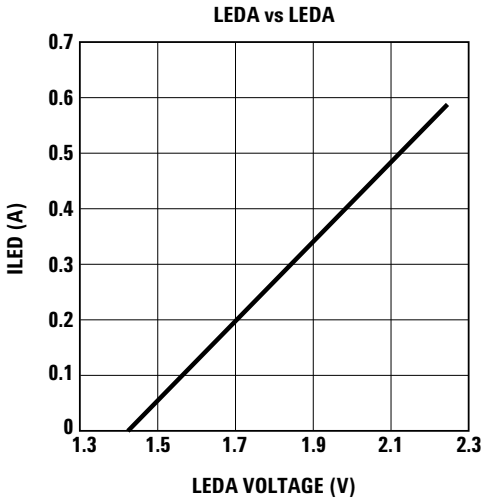
1. In-Band EI ≤ 115.2 kb/s and FIR_SEL = 0.
2. In-Band EI ≥ 0.576 Mb/s and FIR_SEL = 1.
3. Logic Low is a pulsed response. The condition is maintained for duration dependent on the pattern and strength of the incident intensity.
4. To maintain low shutdown current, TXD needs to be driven high or low and not left floating.

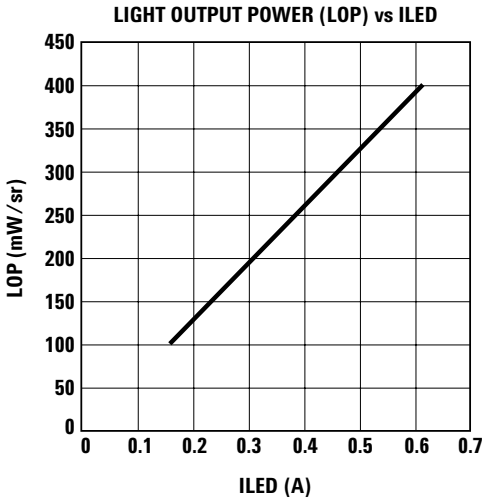
Recommended Application Circuit Components

Component	Recommended Value
R1	2.2 Ω ± 5%, 0.5 Watt, for 2.7 ≤ V_{CC} ≤ 3.3 V operation
	2.7 Ω ± 5%, 0.5 Watt, for 3.0 ≤ V_{CC} ≤ 3.6 V operation
CX1[5]	0.47 µF ± 20%, X7R Ceramic
CX2[6]	6.8 µF ± 20%, Tantalum

Notes:

5. CX1 must be placed within 0.7 cm of the HSDL-3602 to obtain optimum noise immunity.
6. In "HSDL-3602 Functional Block Diagram" on page 1 it is assumed that Vled and V_{CC} share the same supply voltage and filter capacitors. In case the 2 pins are powered by different supplies CX2 is applicable for Vled and CX1 for V_{CC}. In environments with noisy power supplies, including CX2 on the V_{CC} line can enhance supply rejection performance.





Marking Information

The HSDL-3602-007/-037 is marked '3602YYWW' on the shield where 'YY' indicates the unit's manufacturing year, and 'WW' refers to the work week in which the unit is tested.

Absolute Maximum Ratings[7]

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Storage Temperature	T_S	–40	+100	°C	
Operating Temperature	T_A	–20	+70	°C	
DC LED Current	I_{LED} (DC)		165	mA	
Peak LED Current	I_{LED} (PK)		650	mA	≤ 90 µs pulse width, ≤ 25% duty cycle
			750	mA	≤ 2 µs pulse width, ≤ 10% duty cycle
LED Anode Voltage	V_{LEDA}	–0.5	7	V	
Supply Voltage	V_{CC}	0	7	V	
Transmitter Data Input Current	I_{TXD} (DC)	–12	12	mA	
Receiver Data Output Voltage	V_O	–0.5	V_{CC} + 0.5	V	$\|I_O(RXD)\|$ = 20 µA

Note:
7. For implementations where case to ambient thermal resistance ≤ 50°C/W.

Caution: *The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Operating Temperature	T_A	–20	+70	˚C	
Supply Voltage	V_{CC}	2.7	3.6	V	
Logic High Input Voltage for TXD, MD0, MD1, and FIR_SEL	V_{IH}	2 V_{CC}/3	V_{CC}	V	
Logic Low Transmitter Input Voltage	V_{IL}	0	V_{CC}/3	V	
LED (Logic High) Current Pulse Amplitude	I_{LEDA}	400	650	mA	
Receiver Signal Rate		0.0024	4	Mb/s	

Electrical & Optical Specifications

Specifications hold over the Recommended Operating Conditions unless otherwise noted. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25˚C and 3.3 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Transceiver							
Supply Current	Shutdown	I_{CC1}		10	200	nA	$V_{SD} \geq V_{CC} - 0.5$
	Idle	I_{CC2}		2.5	5	mA	V_I(TXD) ≤ V_{IL}, EI = 0
Digital Input Current	Logic Low/High	I_L/I_H	–1		1	µA	$0 \leq V_I \leq V_{CC}$
Transmitter							
Transmitter Radiant Intensity	Logic High Intensity	EI_H	100	250	400	mW/sr	V_{IH} = 3.0 V I_{LEDA} = 400 mA $\theta_{1/2} \leq 15^{\circ}$
	Peak Wavelength	λ_p		875		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		35		nm	
	Viewing Angle	$2\theta_{1/2}$	30		60	°	
	Optical Pulse Width	tpw (EI)	1.5	1.6	1.8	µs	tpw(TXD) = 1.6 µs at 115.2 kb/s
			148	217	260	ns	tpw(TXD) = 217 ns at 1.15 Mb/s
			115	125	135	ns	tpw(TXD) = 125 ns at 4.0 Mb/s
	Rise and Fall Times	t_r (EI), t_f (EI)			40	ns	tpw(TXD) = 125 ns at 4.0 Mb/s $t_{r/f}$(TXD) = 10 ns
	Maximum Optical Pulse Width	tpw (max)		20	50	µs	TXD pin stuck high
LED Anode On State Voltage		V_{ON}(LEDA)			2.4	V	I_{LEDA} = 400 mA, V_I(TXD) ≥ V_{IH}
LED Anode Off State Leakage Current		I_{LK}(LEDA)		1	100	nA	$V_{LEDA} = V_{CC}$ = 3.6 V, V_I(TXD) ≤ V_{IL}

Electrical & Optical Specifications

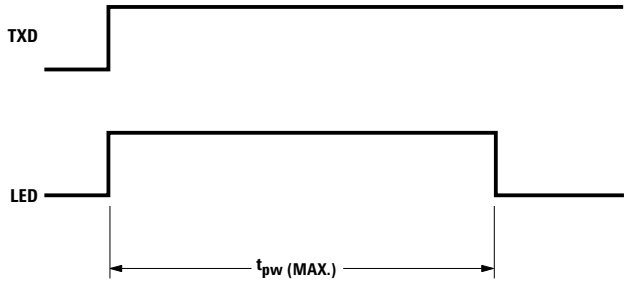
Specifications hold over the Recommended Operating Conditions unless otherwise noted. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25°C and 3.3 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver							
Receiver Data Output Voltage	Logic Low	V_{OL}	0	—	0.4	V	I_{OL} = 1.0 mA, EI ≥ 3.6 μW/cm^2, $\theta_{1/2} \leq 15°$
	Logic High	V_{OH}	V_{CC} – 0.2	—	V_{CC}	V	I_{OH} = –20 μA, EI ≤ 0.3 μW/cm^2, $\theta_{1/2} \leq 15°$
	Viewing Angle	$2\theta_{1/2}$	30			°	
Logic High Receiver Input Irradiance		EI_H	0.0036		500	mW/cm^2	For in-band signals ≤ 115.2 kb/s[8]
			0.0090		500	mW/cm^2	0.576 Mb/s ≤ in-band signals ≤ 4 Mb/s[8]
Logic Low Receiver Input Irradiance		EI_L			0.3	μW/cm^2	For in-band signals[8]
Receiver Peak Sensitivity Wavelength		λ_P		880		nm	
Receiver SIR Pulse Width		tpw (SIR)	1		4.0	μs	$\theta_{1/2} \leq 15°$[10], C_L = 10 pF
Receiver MIR Pulse Width		tpw (MIR)	100		500	ns	$\theta_{1/2} \leq 15°$[11], C_L = 10 pF
Receiver FIR Pulse Width		tpw (FIR)	85		165	ns	$\theta_{1/2} \leq 15°$[12], C_L = 10 pF, V_{CC} = 3 to 3.6 V
					190	ns	$\theta_{1/2} \leq 15°$[12], C_L = 10 pF, V_{CC} = 2.7 V
Receiver ASK Pulse Width		tpw (ASK)		1		μs	500 kHz/50% duty cycle carrier ASK[13]
Receiver Latency Time for FIR		t_L (FIR)		40	50	μs	
Receiver Latency Time for SIR		t_L (SIR)		20	50	μs	
Receiver Rise/Fall Times		$t_{r/f}$ (RXD)		25		ns	
Receiver Wake Up Time		t_W			100	μs	[14]

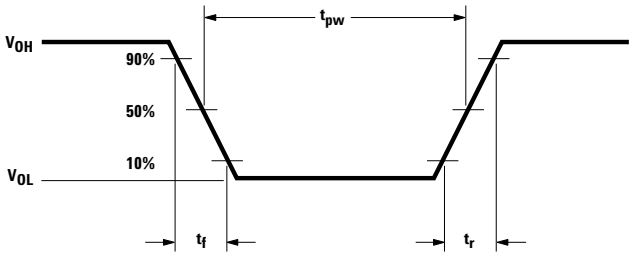
Notes:

8. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
9. Logic Low is a pulsed response. The condition is maintained for duration dependent on pattern and strength of the incident intensity.
10. For in-band signals ≤ 115.2 kb/s where 3.6 μW/cm^2 ≤ EI ≤ 500 mW/cm^2.
11. For in-band signals at 1.15 Mb/s where 9.0 μW/cm^2 ≤ EI ≤ 500 mW/cm^2.
12. For in-band signals of 125 ns pulse width, 4 Mb/s, 4 PPM at recommended 400 mA drive current.
13. Pulse width specified is the pulse width of the second 500 kHz carrier pulse received in a data bit. The first 500 kHz carrier pulse may exceed 2 μs in width, which will not affect correct demodulation of the data stream. An ASK or DASK system using the HSDL-3602 has been shown to correctly receive all data bits for 9 μW/cm^2 ≤ EI ≤ 500 mW/cm^2 incoming signal strength. ASK or DASK should use the FIR channel enabled.
14. The wake up time is the time between the transition from a shutdown state to an active state, and the time when the receiver is active and ready to receive infrared signals.

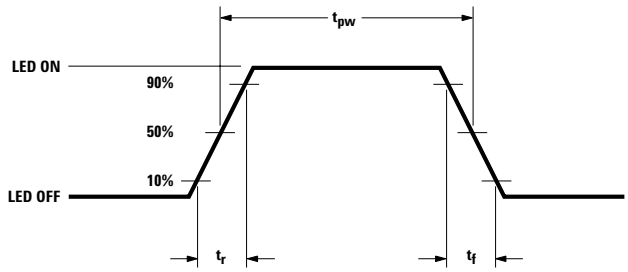
TXD "Stuck ON" Protection



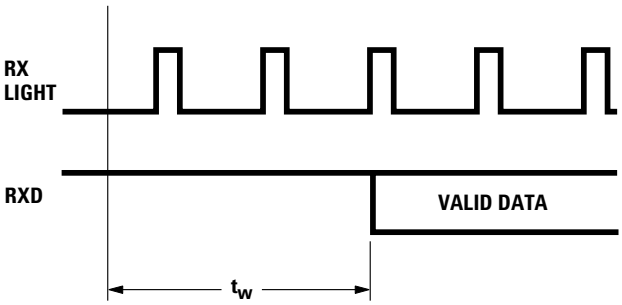
RXD Output Waveform



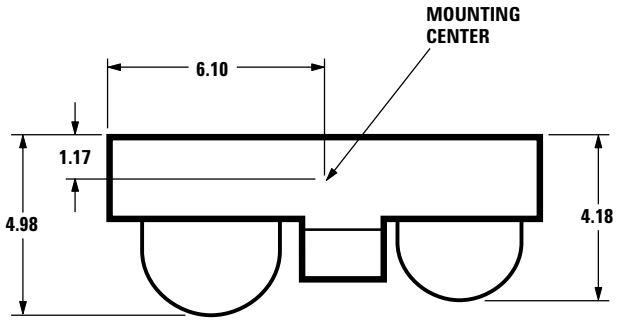
LED Optical Waveform



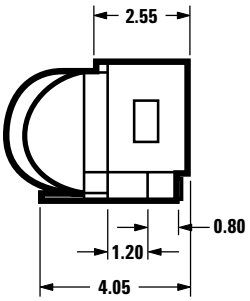
Receiver Wake Up Time Definition (when MD0 ≠ 1 and MD1 ≠ 0)



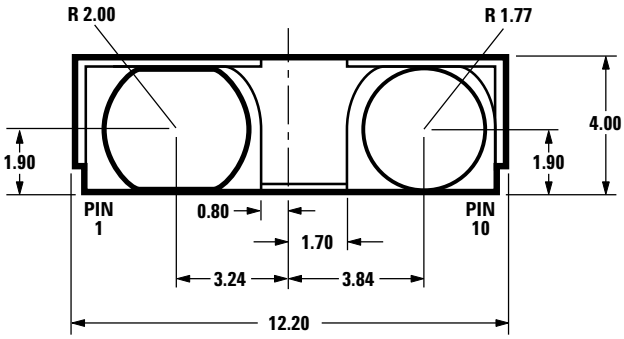
HSDL-3602-007 and HSDL-3602-037 Package Outline with Dimension and Recommended PC Board Pad Layout



TOP VIEW



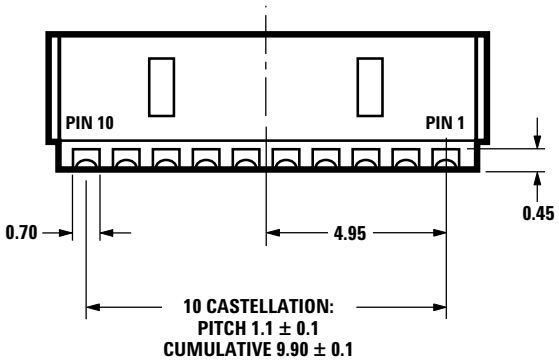
SIDE VIEW



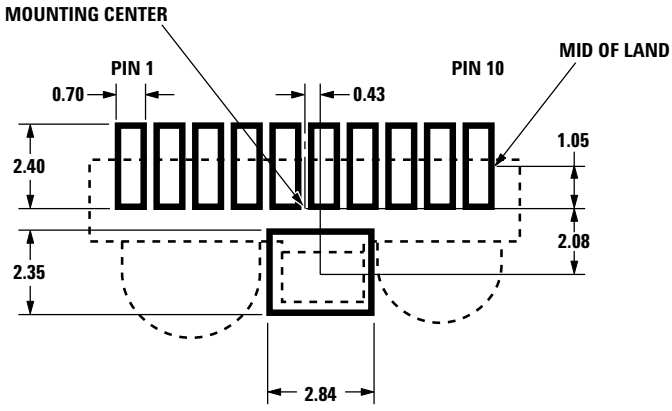
FRONT VIEW

ALL DIMENSIONS IN MILLIMETERS (mm).

DIMENSION TOLERANCE IS 0.20 mm
UNLESS OTHERWISE SPECIFIED.

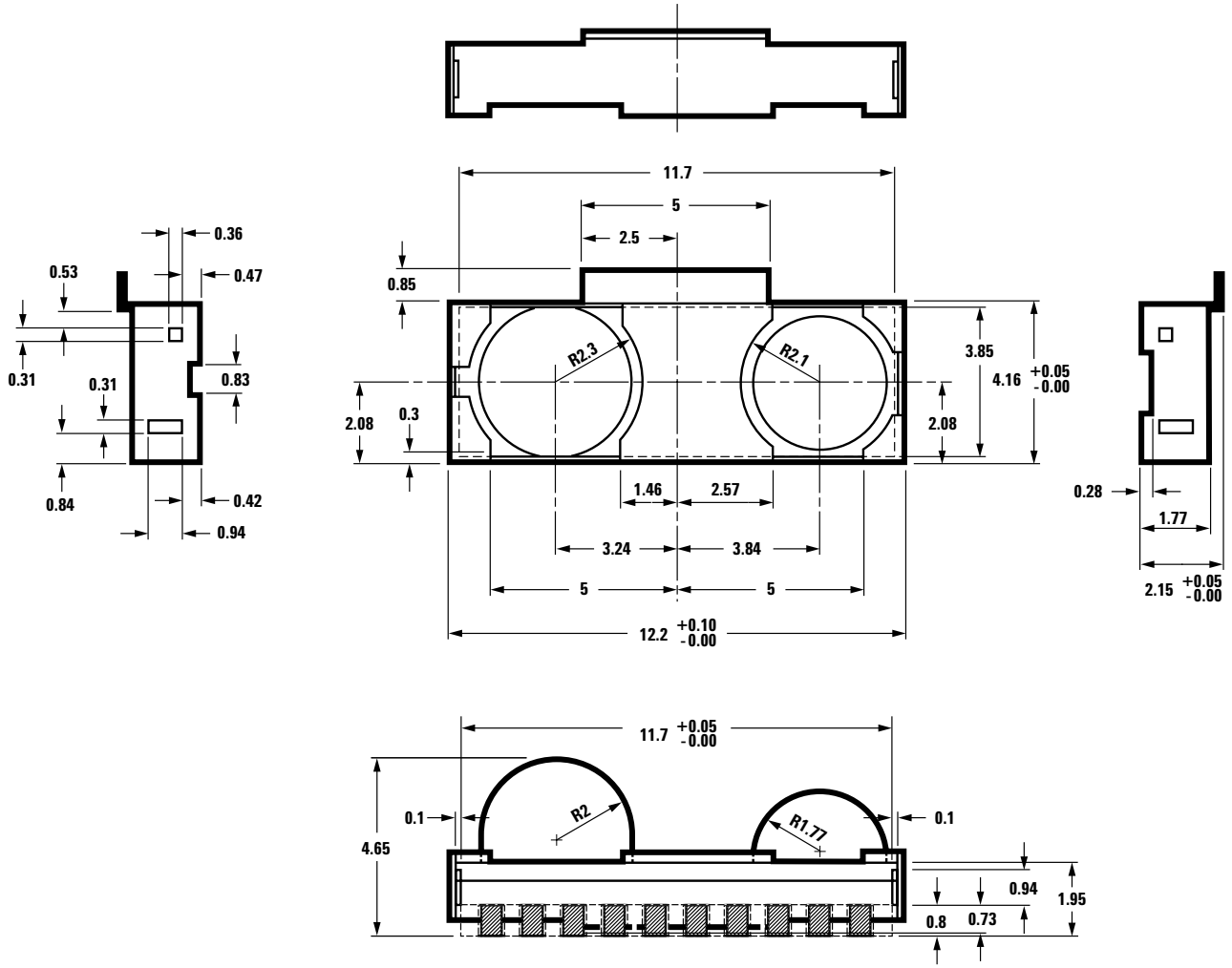


BACK VIEW



LAND PATTERN

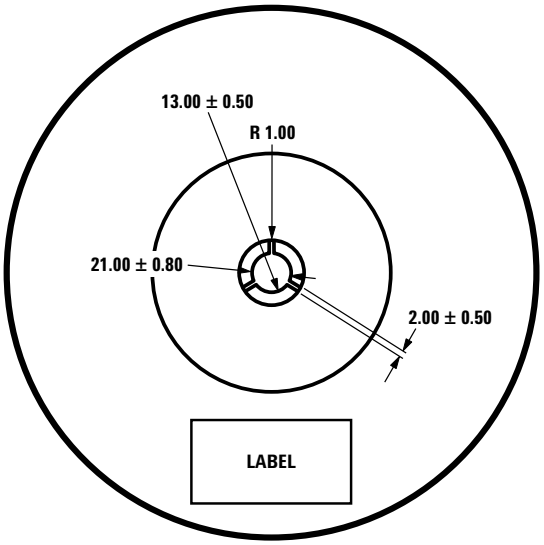
HSDL-3602-008 and HSDL-3602-038 Package Outline with Dimension and Recommended PC Board Pad Layout



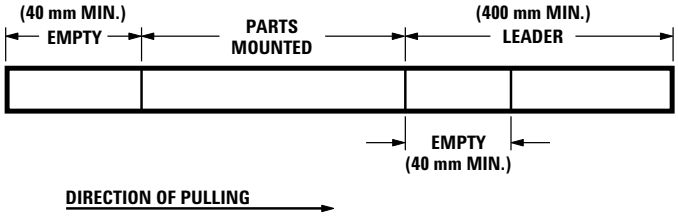
Tape and Reel Dimensions (HSDL-3602-007, -037)

ALL DIMENSIONS IN MILLIMETERS (mm)

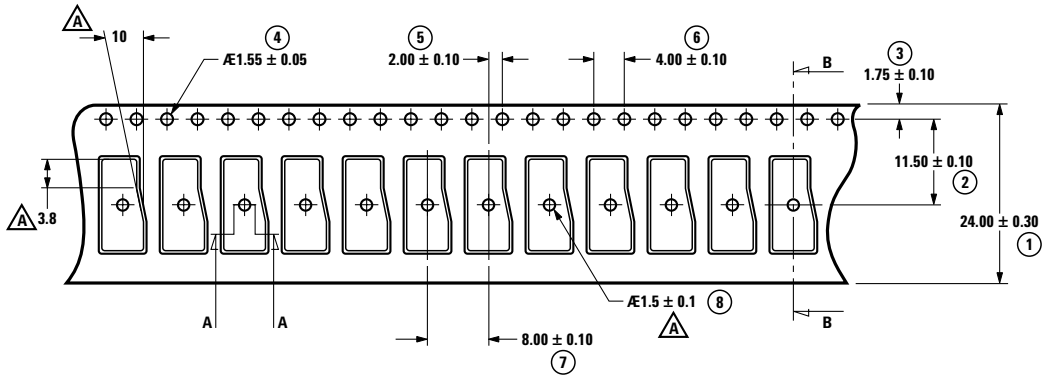
QUANTITY = 400 PIECES PER REEL (HSDL-3602-007)
1800 PIECES PER TAPE (HSDL-3602-037)

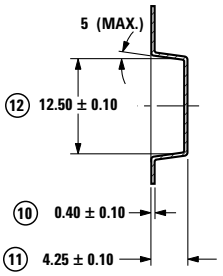


SHAPE AND DIMENSIONS OF REELS

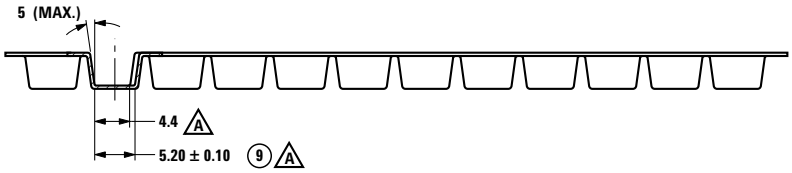


CONFIGURATION OF TAPE





SECTION B-B

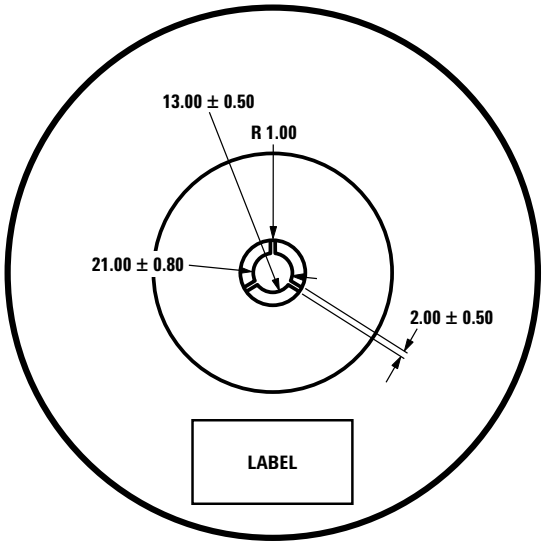


SECTION A-A

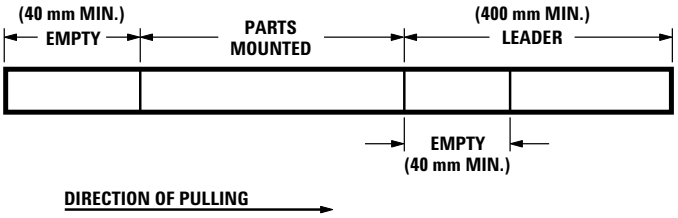
Tape and Reel Dimensions (HSDL-3602-008, -038)

ALL DIMENSIONS IN MILLIMETERS (mm)

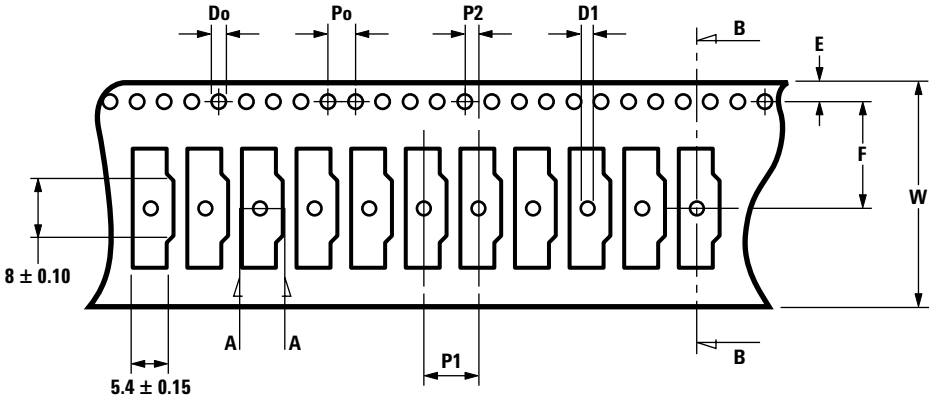
QUANTITY = 400 PIECES PER REEL (HSDL-3602-008)
1800 PIECES PER TAPE (HSDL-3602-038)

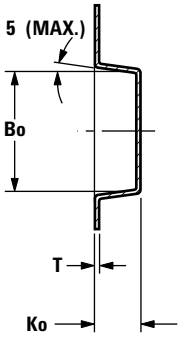


SHAPE AND DIMENSIONS OF REELS

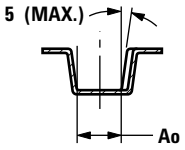


CONFIGURATION OF TAPE





SECTION B-B



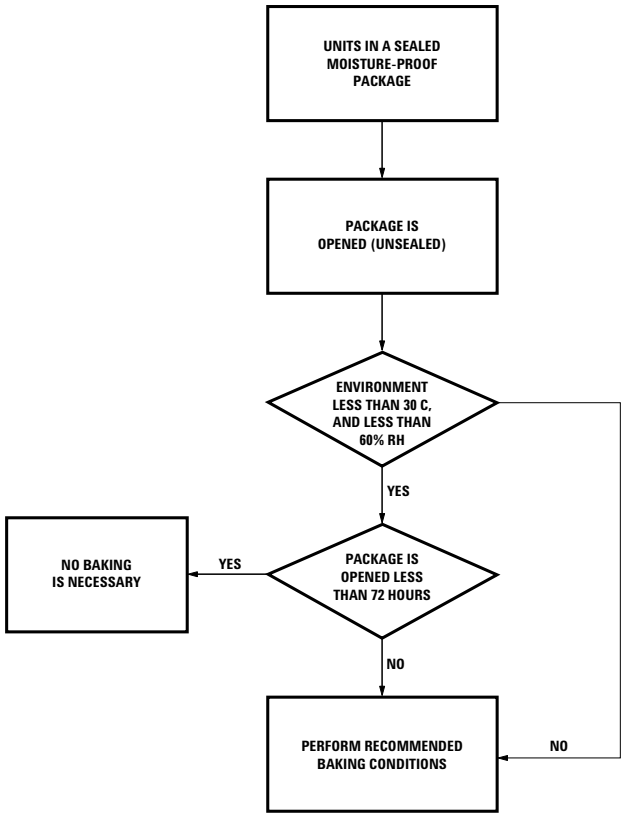
SECTION A-A

SYMBOL	Ao	Bo	Ko	Po	P1	P2	T
SPEC	4.4 ± 0.10	12.50 ± 0.10	4.85 ± 0.10	4.0 ±0.10	8.0 ± 0.10	2.0 ± 0.10	0.35 ± 0.10
SYMBOL	E	F	Do	D1	W	10Po	
SPEC	1.75 ± 0.10	11.5 ± 0.10	1.55 ± 0.10	1.5 ± 0.10	24.0 ± 0.3	40.0 ± 0.20	

NOTES:
1. I.D. sprocket hole pitch cumulative tolerance is ± 0.2 mm.
2. Corner camber shall be not more than 1 mm per 100 mm through a length of 250 mm.
3. Ao and Bo measured on a place 0.3 mm above the bottom of the pocket.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Moisture Proof Packaging

All HSDL-3602 options are shipped in moisture proof package. Once opened, moisture absorption begins.



Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time
In reels	60°C	≥ 48 hours
In bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hour

Baking should be done only once.

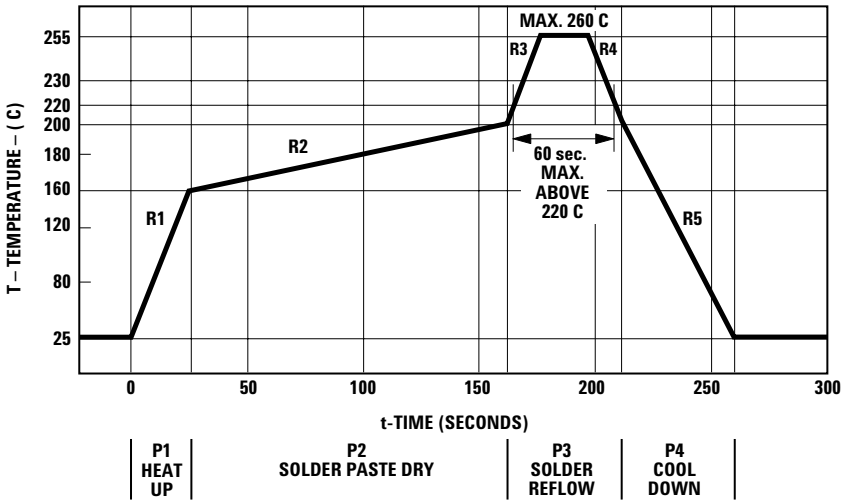
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 3 days if stored at the recommended storage conditions. If times longer than 72 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25˚C to 160˚C	4˚C/s
Solder Paste Dry	P2, R2	160˚C to 200˚C	0.5˚C/s
Solder Reflow	P3, R3	200˚C to 255˚C	4˚C/s
		(260˚C at 10 seconds max.)	
	P3, R4	255˚C to 200˚C	–6˚C/s
Cool Down	P4, R5	200˚C to 25˚C	–6˚C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the following table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and HSDL-3602 castellation pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3602 castellations.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3602 castellations to change dimensions evenly, putting minimal stresses on the HSDL-3602 transceiver.

Appendix A: HSDL-3602-007/-037 SMT Assembly Application Note

1.0. Solder Pad, Mask, and Metal Solder Stencil Aperture

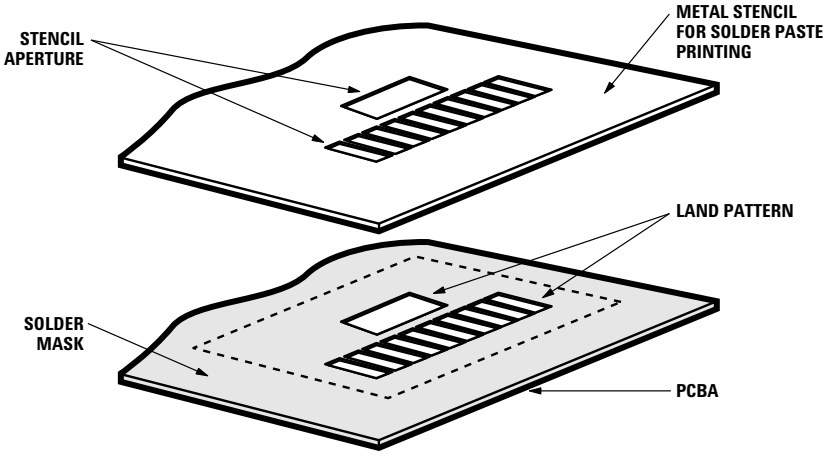


Figure 1. Stencil and PCBA.

1.1. Recommended Land Pattern for HSDL-3602-007/-037

Dim.	mm	inches
a	2.40	0.095
b	0.70	0.028
c (pitch)	1.10	0.043
d	2.35	0.093
e	2.80	0.110
f	3.13	0.123
g	4.31	0.170

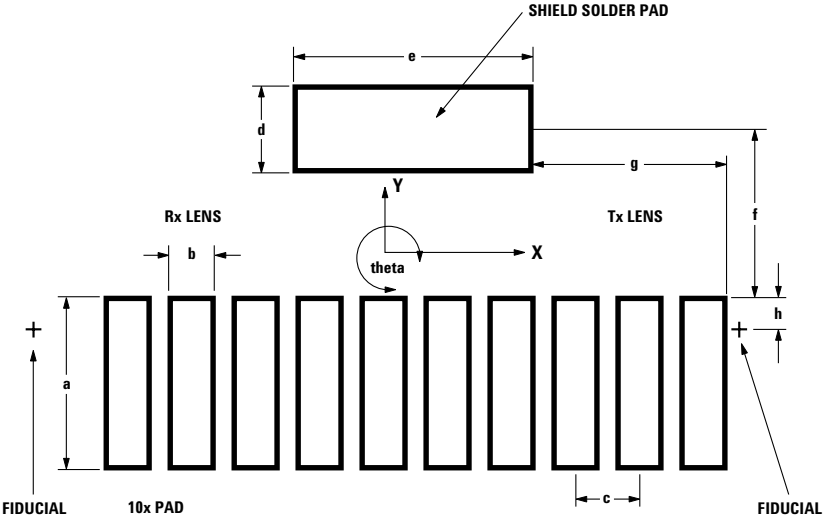


Figure 2. Top view of land pattern.

1.2. Adjacent Land Keep-out and Solder Mask Areas

Dim.	mm	inches
h	min. 0.2	min. 0.008
j	13.4	0.528
k	4.7	0.185
l	3.2	0.126

- Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- "h" is the minimum solder resist strip width required to avoid solder bridging adjacent pads.
- It is recommended that 2 fiducial cross be placed at mid-length of the pads for unit alignment.

Note : Wet/Liquid Photo-Imagineable solder resist/mask is recommended.

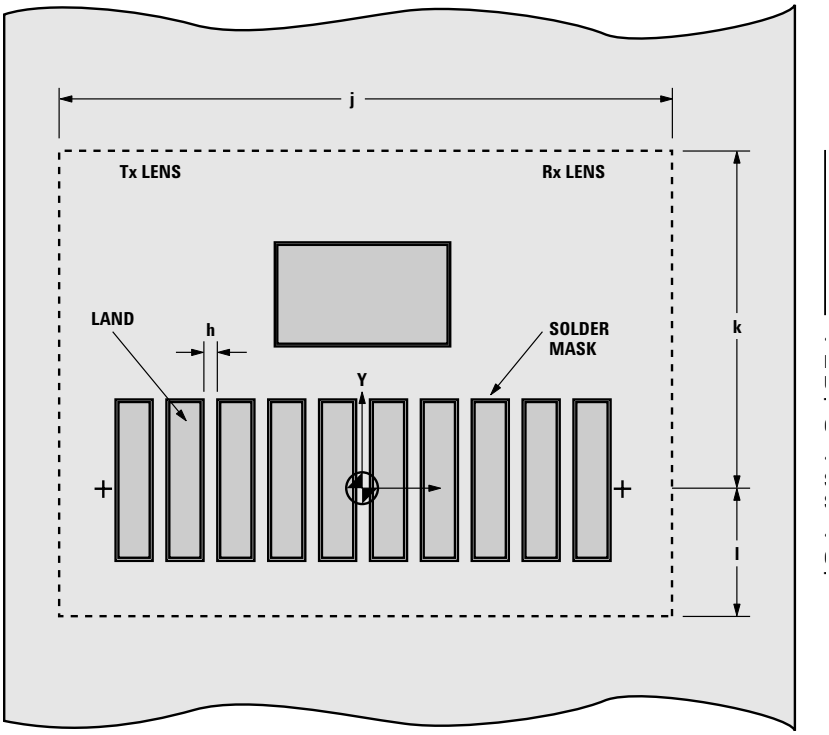


Figure 3. HSDL-3602-007/-037 PCBA-Adjacent land keep-out and solder mask.

2.0. Recommended solder paste/cream volume for castellation joints

Based on calculation and experiment, the printed solder paste volume required per castellation pad is 0.30 cubic mm (based on either no-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

2.1. Recommended Metal Solder Stencil Aperture

It is recommended that only 0.152 mm (0.006 inches) or 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

See Figure 4			
	t, nominal stencil thickness		**l, length of aperture**
	mm	**inches**	**mm**	**inches**
	0.152	0.006	2.8 ± 0.05	0.110 ± 0.002
	0.127	0.005	3.4 ± 0.05	0.134 ± 0.002
w, the width of aperture is fixed at 0.70 mm (0.028 inches)				
Aperture opening for shield pad is 2.8 mm x 2.35 mm as per land dimension.				

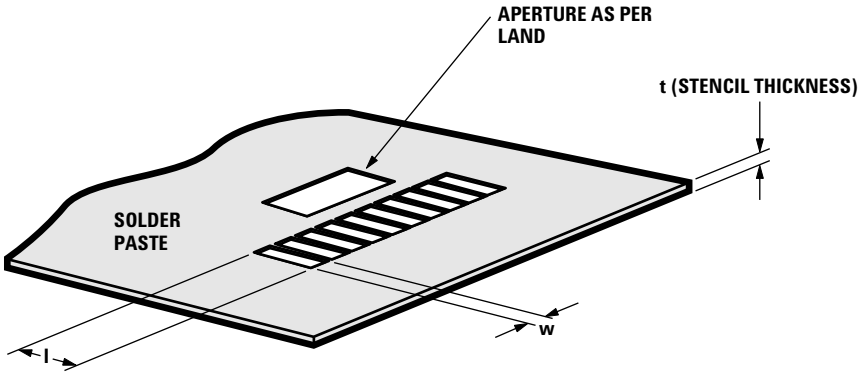


Figure 4. Solder paste stencil aperture.

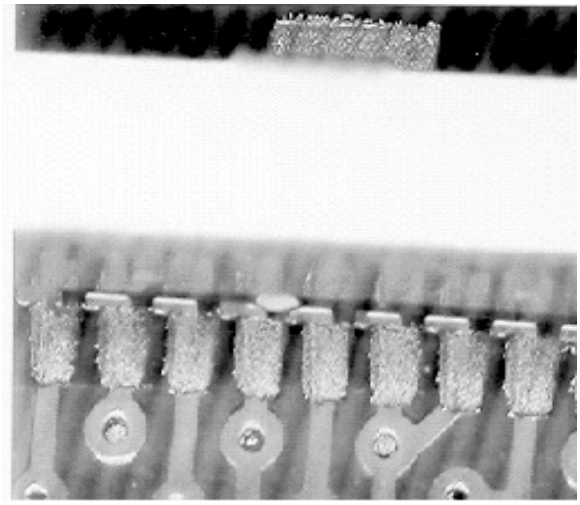
3.0. Pick and Place Misalignment Tolerance and Product Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, the unit will self-align in the X-direction after solder reflow. Units should be properly reflowed in IR Hot Air convection oven using the recommended reflow profile. The direction of board travel does not matter.

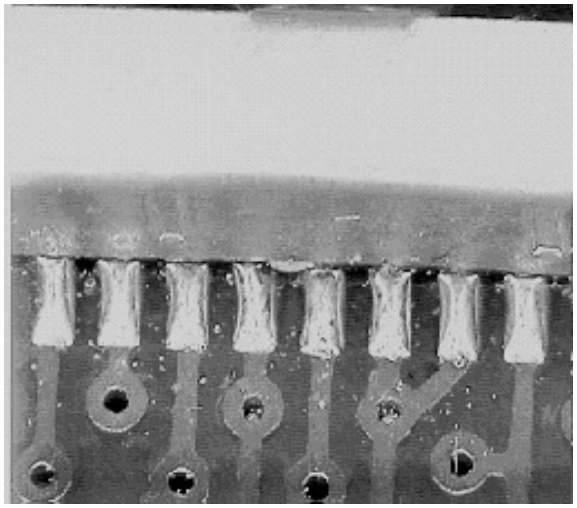
Allowable Misalignment Tolerance	
X-direction	≤ 0.2 mm (0.008 inches)
Theta-direction	± 2 degrees

3.1. Tolerance for X-axis Alignment of Castellation

Misalignment of castellation to the land pad should not exceed 0.2 mm or approximately half the width of the castellation during placement of the unit. The castellations will completely self-align to the pads during solder reflow as seen in the pictures below.



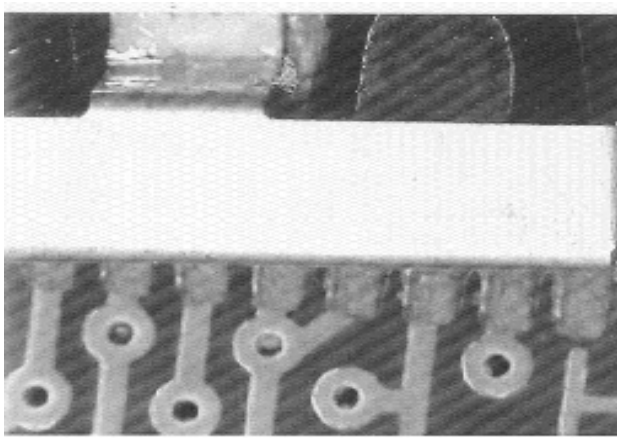
Picture 1. Castellation misaligned to land pads in X-axis before reflow.



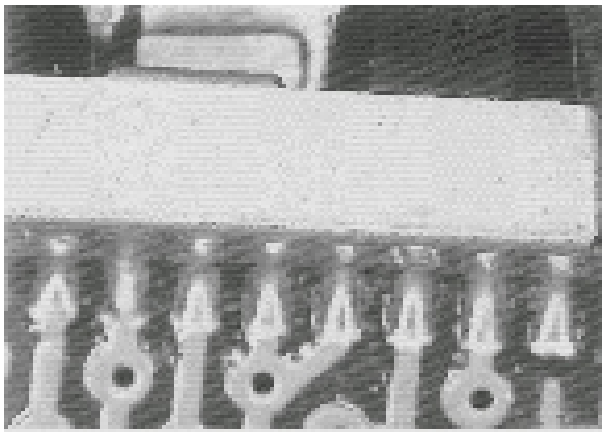
Picture 2. Castellation self-align to land pads after reflow.

3.2. Tolerance for Rotational (Theta) Misalignment

Units when mounted should not be rotated more than ± 2 degrees with reference to center X-Y as specified in Figure 2. Pictures 3 and 4 show units before and after reflow. Units with a Theta misalignment of more than 2 degrees do not completely self-align after reflow. Units with ± 2 degree rotational or Theta misalignment self-aligned completely after solder reflow.



Picture 3. Unit is rotated before reflow.



Picture 4. Unit self-aligns after reflow.

3.3. Y-axis Misalignment of Castellation

In the Y-direction, the unit does not self-align after solder reflow. It is recommended that the unit be placed in line with the fiducial mark (mid-length of land pad). This will enable sufficient land length (minimum of 1/2 land length) to form a good joint. See Figure 5.

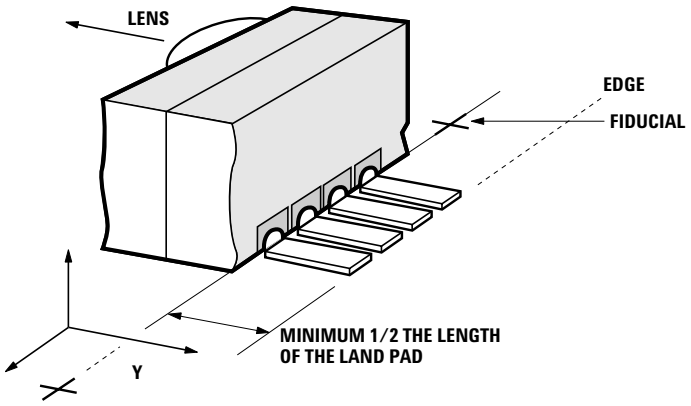
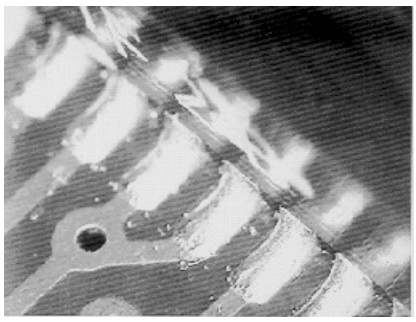


Figure 5. Section of a castellation in Y-axis.

3.4. Example of Good HSDL-3602-007/-037 Castellation Solder Joints

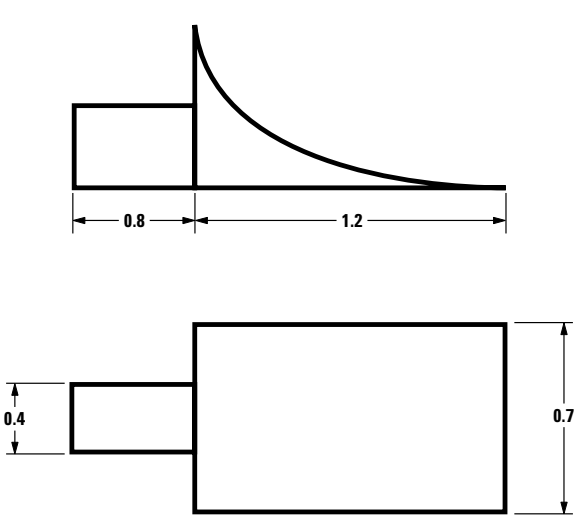
This joint is formed when the printed solder paste volume is adequate, i.e., 0.30 cubic mm and reflowed properly. It should be reflowed in IR Hot-air convection reflow oven. Direction of board travel does not matter.



Picture 5. Good solder joint.

4.0. Solder Volume Evaluation and Calculation

Geometery of an HSDL-3602-007/-037 solder fillet.



Appendix B: HSDL-3602-008/-038 SMT Assembly Application Note

1.0. Solder Pad, Mask, and Metal Solder Stencil Aperture

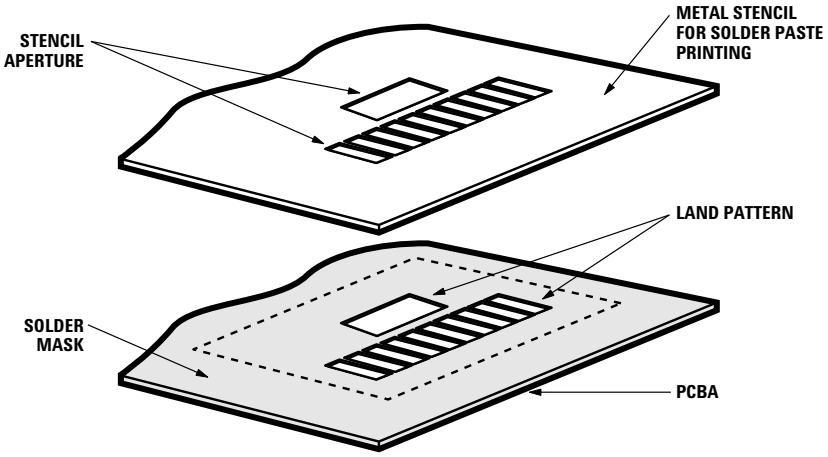
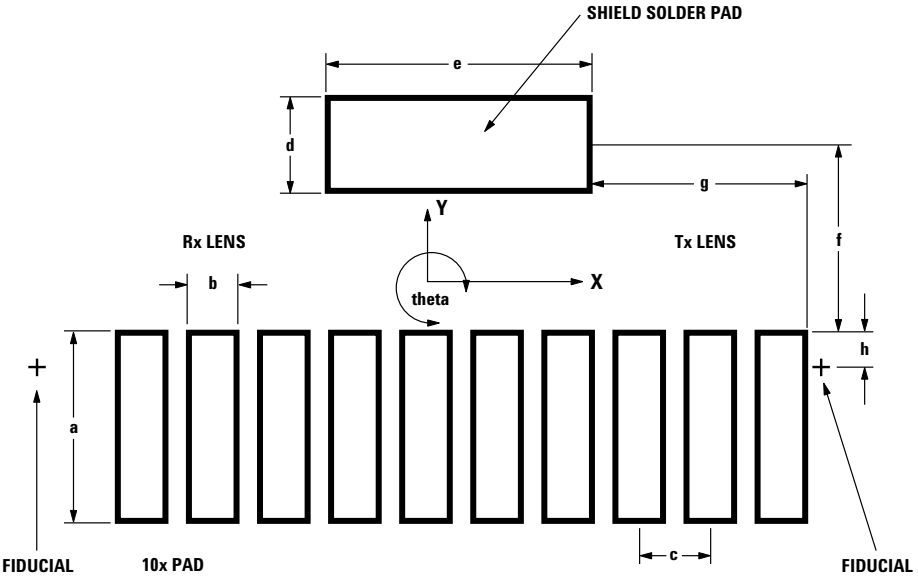


Figure 1. Stencil and PCBA.

1.1. Recommended Land Pattern for HSDL-3602-008/-038

Dim.	mm	inches
a	1.95	0.077
b	0.60	0.024
c (pitch)	1.10	0.043
d	1.60	0.063
e	5.70	0.224
f	3.80	0.123
g	2.40	0.170



2.0 Y-axis Misalignment of Castellation

In the Y-direction, the unit does not self-align after solder reflow. It is recommended that the unit be placed in line with the fiducial mark (mid-length of land pad). This will enable sufficient land length (minimum of 1/2 land length) to form a good joint. See Figure 2.

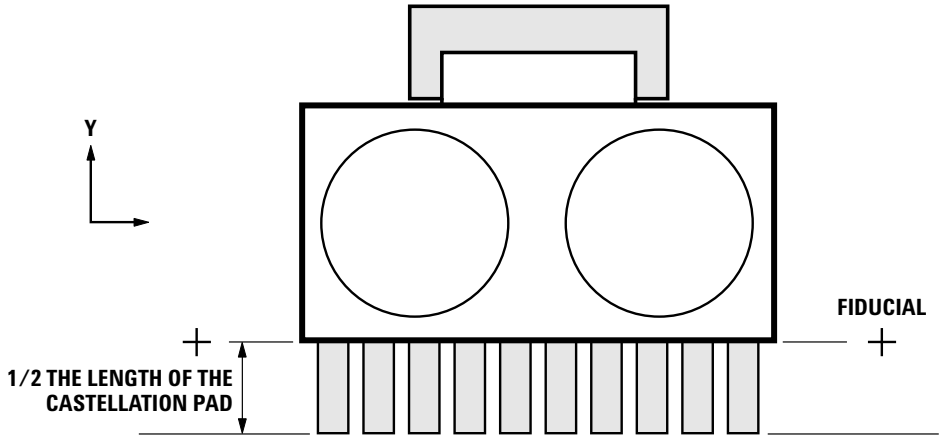


Figure 2. Section of a castellation in Y-axis.

Appendix C: General Application Guide for the HSDL-3602 Infrared IrDA® Compliant 4 Mb/s Transceiver

Description

The HSDL-3602 wide voltage operating range infrared transceiver is a low-cost and small form factor that is designed to address the mobile computing market such as notebooks, printers and LAN access as well as small embedded mobile products such as digital cameras, cellular phones, and PDAs. It is fully compliant to IrDA 1.1 specification up to 4 Mb/s, and supports HP-SIR, Sharp ASK, and TV Remote modes. The design of the HSDL-3602 also includes the following unique features:

- Low passive component count.
- Adjustable Optical Power Management (full, 2/3, 1/3 power).
- Shutdown mode for low power consumption requirement.
- Single-receive output for all data rates.

Adjustable Optical Power Management

The HSDL-3602 transmitter offers user-adjustable optical power levels. The use of two logic-level mode-select input pins, MODE 0 and MODE 1, offers shutdown mode as well as three transmit power levels as shown in the following Table. The power levels are setup to correspond nominally to maximum, two-third, and one-third of the transmission distance. This unique feature allows lower optical power to be transmitted at shorter link distances to reduce power consumption.

MODE	MODE 1	Transmitter
1	0	Shutdown
0	0	Full Power
0	1	2/3 Power
1	1	1/3 Power

There are 2 basic means to adjust the optical power of the HSDL-3602:

Dynamic: This implementation enables the transceiver pair to adjust their transmitter power according to the link distance. However, this requires the IrDA protocol stack (mainly the IrLAP layer) to be modified. Please contact Agilent Application group for further details.

Static: Pre-program the ROM BIOS of the system (e.g. notebook PC, digital camera, cell phones, or PDA) to allow the end user to select the desired optical power during the system setup stage.

Selection of Resistor R1
Resistor R1 should be selected to provide the appropriate peak pulse LED current over different ranges of Vcc. The recommended R1 for the voltage range of 2.7 V to 3.3 V is 2.2 Ω while for 3.0 V to 3.6 V is 2.7 Ω. The HSDL-3602 typically provides 250 mW/sr of intensity at the recommended minimum peak pulse LED current of 400 mA.

Interface to Recommended I/O chips
The HSDL-3602's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required.

Data rate from 9.6 kb/s up to 4 Mb/s is available at the RXD pin. The FIR_SEL pin selects the data rate that is receivable through RXD. Data rates up to 115.2 kb/s can be received if FIR_SEL is set to logic low. Data rates up to 4 Mb/s can be received if FIR_SEL is set to logic high. Software driver is necessary to program the FIR_SEL to low or high at a given data rate.

4 Mb/s IR link distance of greater than 1.5 meters have been demonstrated using typical HSDL-3602 units with National Semiconductor's PC87109 3 V Endec and Super I/Os, and the SMC Super I/O chips.

(A) National Semiconductor Super I/O and Infrared Controller

For National Semiconductor Super I/O and Infrared Controller chips, IR link can be realized with the following connections:

- Connect IRTX of the National Super I/O or IR Controller to TXD (pin 9) of the HSDL-3602.
- Connect IRRX1 of the National Super I/O or IR Controller to RXD (pin 8) of the HSDL-3602.
- Connect IRSL0 of the National Super I/O or IR Controller to FIR_SEL (pin 3) of the HSDL-3602.

Please refer to the table below for the IR pin assignments for the National Super I/O and IR Controllers that support IrDA 1.1 up to 4 Mb/s:

(B) HSDL-3602 Interoperability with National Semiconductor PC97338VJG SIO Evaluation R eport

Introduction

The objective of this report is to demonstrate the interoperability of the HSDL-3602 IR transceiver IR module as wireless communication ports at the speed of 2.4 kb/s - 4 Mb/s with NS's PC97338VJG Super I/O under typical operating conditions.

Test Procedures

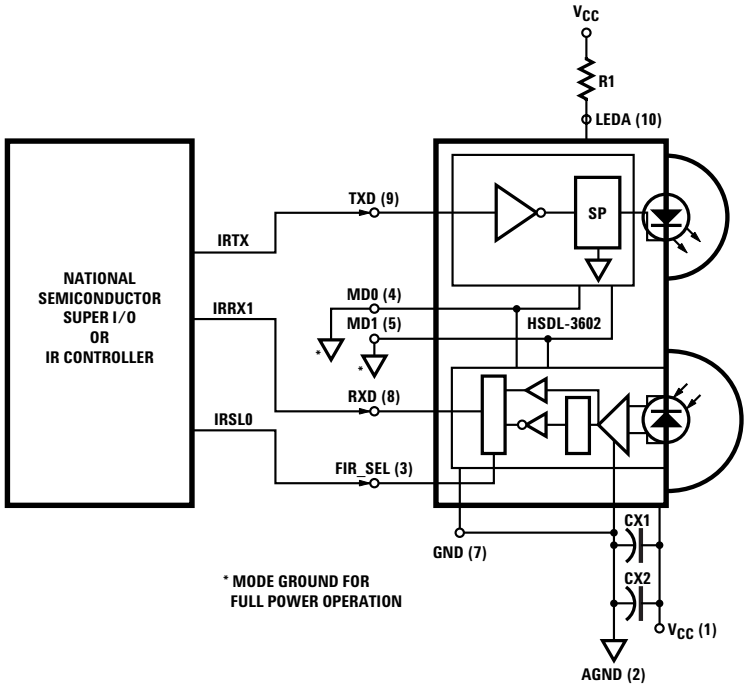
(1) Two PC97338VJG evaluation boards were connected to the ISA Bus of two PCs (Pentium 200 MHz) running Microsoft's DOS operating system. One system with an HSDL-3602 IR transceiver connected to the PC97338VJG evaluation board will act as the master device. Another system with an HSDL-3602 IR transceiver connected to the PC97338VJG will act as the slave device (i.e. Device Under Test).

(2) The test software used in this interoperability test is provided by National Semiconductor. A file size of 1.7M byte from the master device, with the PC97338VJG performing the framing, encoding is transmitted to the slave device. The slave device, with the PC97338VJG performing the decoding, and CRC checksum, will receive the file. The file is then checked for error by comparing the received file with the original file using the DOS "fc" command.

(3) The link distance is measured by adjusting the distance between the master and slave for errorless data communications.

	IRTX	IRRX1	IRSL0
PC97/87338VJG	63	65	66
PC87308VUL	81	80	79
PC87108AVHG	39	38	37
PC87109VBE	15	16	14

Please refer to the National Semiconductor data sheets and application notes for updated information.



HSDL-3600
FUNCTIONAL BLOCK DIAGRAM

HSDL-3602 Interoperability with NS PC97338 Report

(i) Test Conditions
V_{CC} = 3.0 – 3.6 V
RLED = 2.7 Ω
Optical transmitter pulse width = 125 ns
Mode set to full power

(ii) Test Result
The interoperability test results show that HSDL-3602 IR transceiver can operate ≥ 1.5 meter link distance from 3 V to 3.6 V with NS's PC97338 at any IrDA 1.1 data rate without error.

HSDL-3602 Interoperability with SMC 669/769 Report

(i) Test Conditions
Vcc = 3.0 – 3.6 V
RLED = 2.2 Ω
Optical transmitter pulse width = 125 ns
Mode set to full power

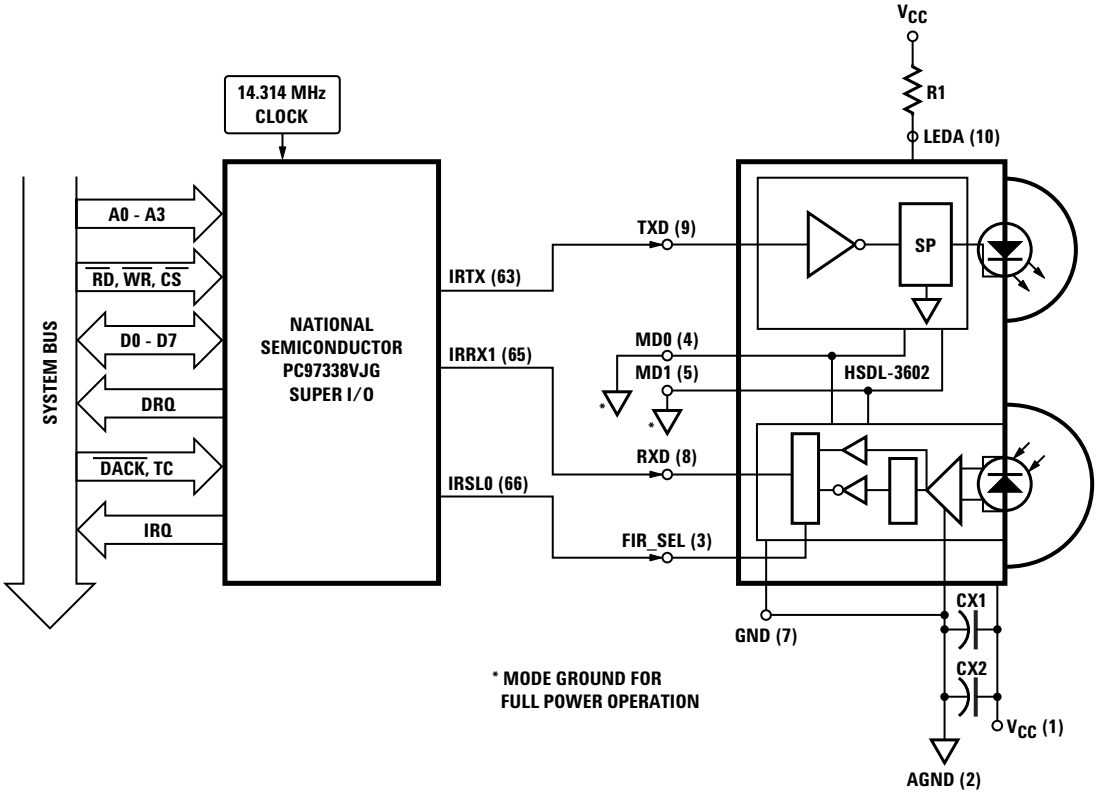
(ii) Test Result
The interoperability test results show that HSDL-3602 IR transceiver can operate ≥ 1.5 meter link distance from 3 V to 3.6 V with SMC 669/769 at any IrDA 1.1 data rate without error.

(C) Standard Micro System Corporation (SMC) Super and Ultra I/O Controllers

For SMC Super and Ultra I/O Controller chips, IR link can be realized with the following connections:

- Connect IRTX of the SMC Super or Ultra I/O Controller to TXD (pin 9) of the HSDL-3602.
- Connect IRRX of the SMC Super or Ultra I/O Controller to RXD (pin 8) of the HSDL-3602.
- Connect IRMODE of the Super or Ultra I/O Controller to FIR_SEL (pin 3) of the HSDL-3602.

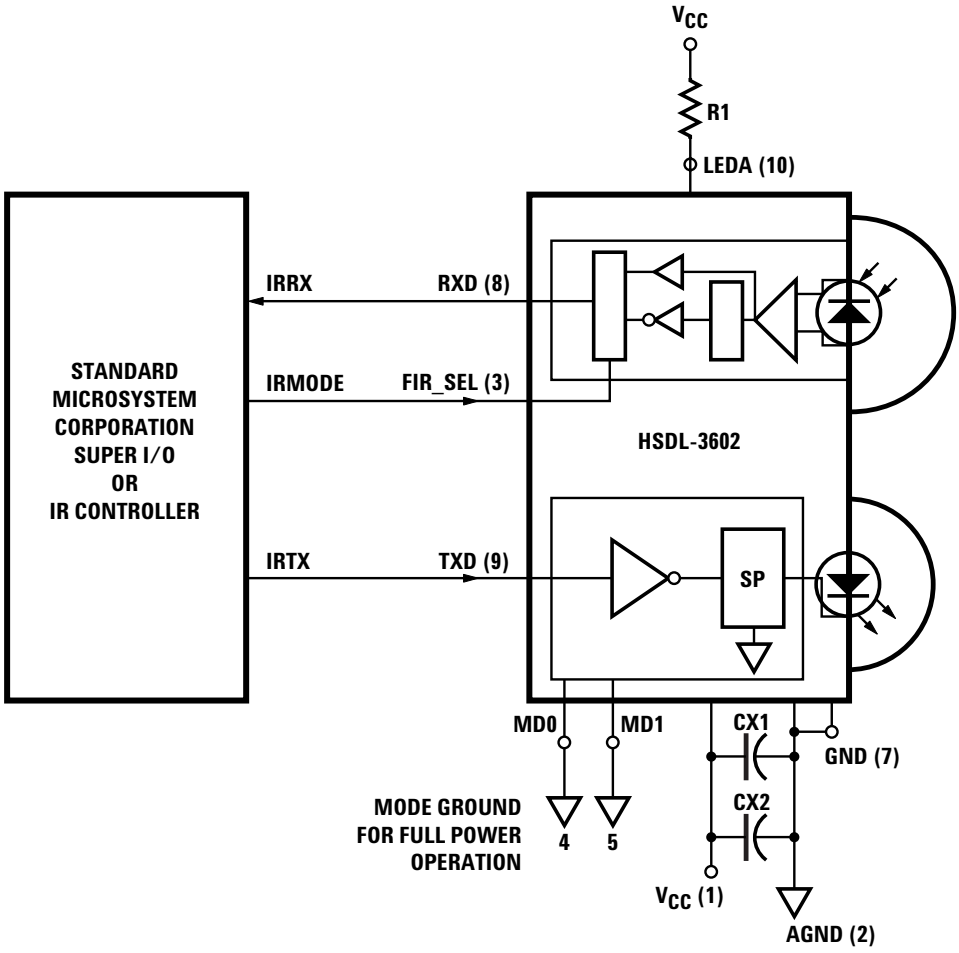
Please refer to the table below for the IR pin assignments for the SMC Super or Ultra I/O Controllers that support IrDA 1.1 up to 4Mb/s:



HSDL-3602 FUNCTIONAL BLOCK DIAGRAM

	IRTX	IRRX	IRMODE
FDC37C669FR	89	88	23
FDC37N769	87	86	21
FDC37C957/8FR	204	203	145 or 190

HSDL-3602 Interoperability with SMC's Super I/O or IR Controller



Appendix D: Optical Port Dimensions for HSDL-3602:

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30^0 and the maximum size corresponds to a cone angle of 60°.

In the figure below, X is the width of the window, Y is the height of the window and Z is the distance from the HSDL-3602 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 7.08mm. The equations for computing the window dimensions are as follows:

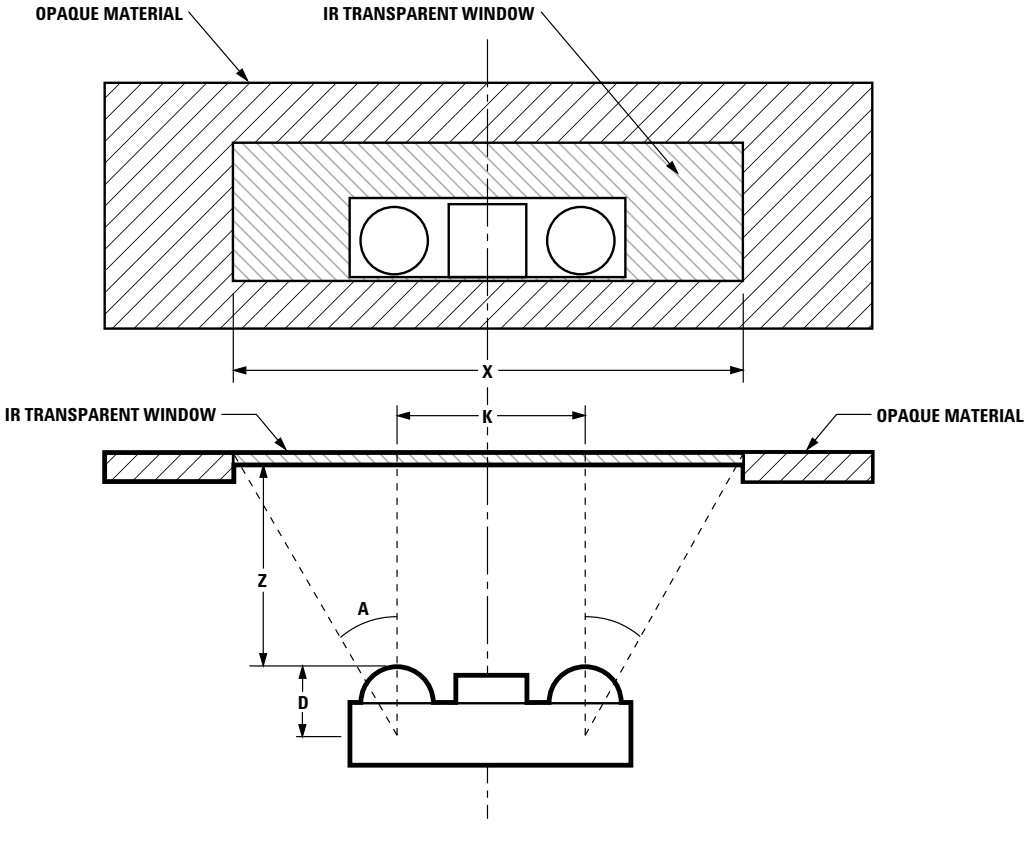
X = K + 2*(Z+D)*tanA

Y = 2*(Z+D)*tanA

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

Z'=Z+t/n

where 't' is the thickness of the window and 'n' is the refractive index of the window material.

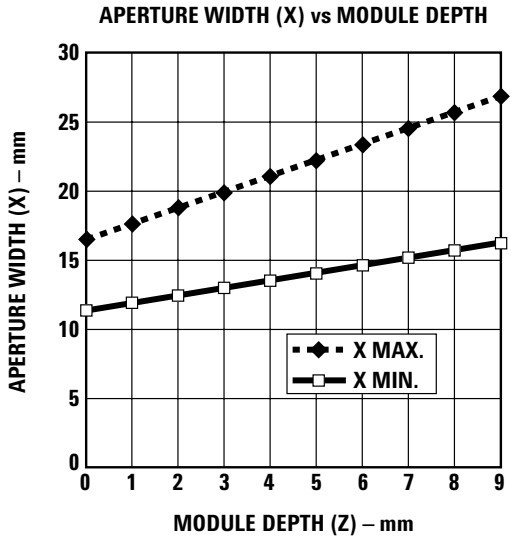


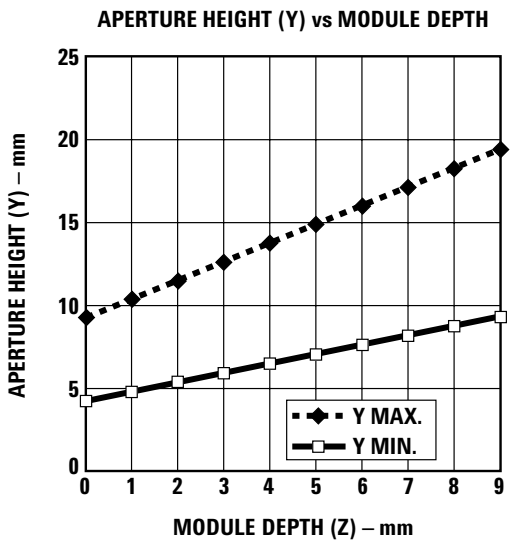
HSDL-3602 Optical Port Dimensions

Section of a castellation in Y-axis.

The depth of the LED image inside the HSDL-3602, D, is 8mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15^0 and the maximum is 30^0. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs:

	Aperture Width (x, mm)		Aperture height (y, mm)	
Module Depth, (z) mm	**max.**	**min.**	**max.**	**min.**
0	16.318	11.367	9.238	4.287
1	17.472	11.903	10.392	4.823
2	18.627	12.439	11.547	5.359
3	19.782	12.975	12.702	5.895
4	20.936	13.511	13.856	6.431
5	22.091	14.047	15.011	6.967
6	23.246	14.583	16.166	7.503
7	24.401	15.118	17.321	8.038
8	25.555	15.654	18.475	8.574
9	26.710	16.190	19.630	9.110





Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10 percent or less for best optical performance. Light loss should be measured at 875 nm.

Shape of the Window

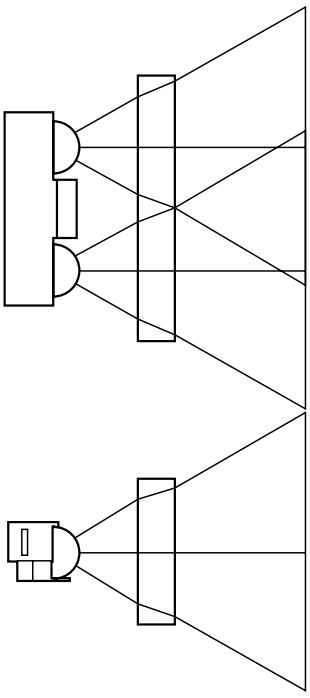
From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.

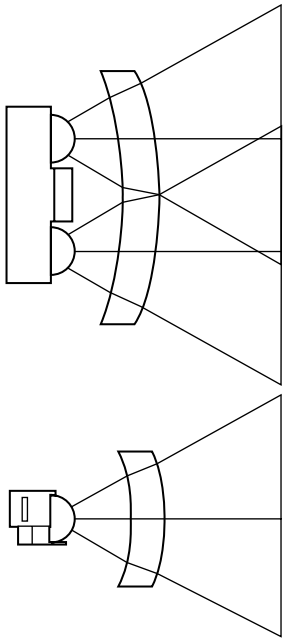
Flat Window

(First choice)



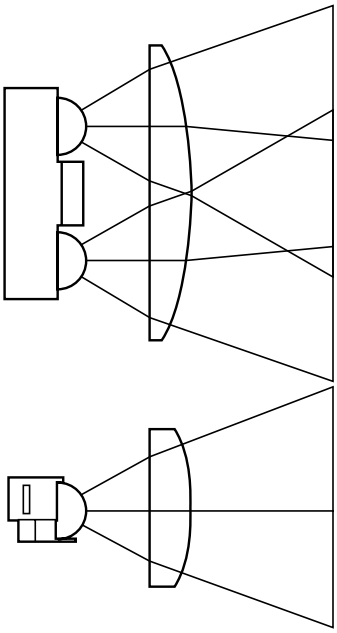
Curved Front and Back

(Second choice)



Curved Front, Flat Back

(Do not use)



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