



### Actual Size $= 5 \times 7$ mm



#### **Product Features**

- High Q fundamental-mode crystal
- No internal PLL or frequency multiplication
- Very low phase noise
- LVCMOS compatible output
- Commercial and industrial operation
- ±50 ppM stability (or as specified)
- $\pm 50$  to  $\pm 100$  ppM absolute (net) pull range
- RoHS Compliant

## **Product Description**

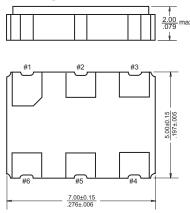
The ST1307 is a voltage controlled crystal oscillator that achieves superb jitter and pullability over a broad range of operating conditions and frequencies. The device is constructed with a hermetically sealed, fundamental-mode quartz crystal resonator exhibiting a high-Q for exceptional phase noise performance. The device, available on tape and reel, is contained in a 5x7mm ceramic package.

## **Applications**

The ST1307 Series VCXO is an ideal component in phase locked loop circuits that perform clock smoothing, clock/data recovery, or frequency translation and card synchronization functions, supporting jitter-sensitive applications such as:

- SMPTE-compliant Video networking
- SONET/SDH timing control and line cards
- T1/E1 Platforms
- Satellite and microwave communications

## **Package Outline**



#### **Pin Functions**

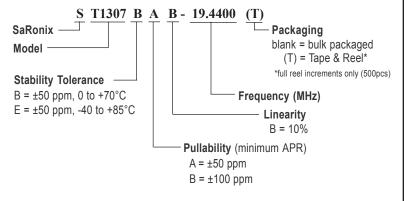
Pad	Function			
1	Control voltage			
2	Output Enable/Disable			
3	Ground			
4	Output			
5	No Connect			
6	Supply voltage			

Full Mechanical Drawings page 6. Dimensions are in mm/inches.

### **Common Frequencies**

Contact SaRonix for additional f	requencies	
1.5440	14.7456	20.4800
2.0480	15.0000	24.5760
6.1760	16.3840	25.0000
8.1920	18.4320	27.0000
12.2880	19.4400	
12.3520	20.0000	

## **Ordering Information**







## **Electrical Performance**

Parameter	Min.	Тур.	Max.	Units	Notes
Output frequency (F <sub>N</sub> )	1.0		32.0	MHz	As specified
Supply voltage	+2.97	+3.3	+3.63	V	
Supply current			15	mA	
Frequency stability			±50	ppM	See #1 and #2 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, VOL			10% V <sub>DD</sub>	V	
Output logic 1, V <sub>OH</sub>	90% V <sub>DD</sub>			V	
Output load			30	pF	
Duty cycle	45		55	%	measured 50% V <sub>DD</sub>
Rise and fall time			8	ns	measured 20/80% V <sub>DD</sub>
Jitter, total			20	ps pk-pk	

#### **Notes:**

- 1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, shock and vibration, with control voltage held at center.
- 2.  $\pm 12$  ppM max due to aging (10 years at 40°C average ambient operating temperature).

## **Frequency Modulation Function**

Parameter	Min.	Тур.	Max.	Units	Notes
Absolute pull range (APR)	±50 to ±100			ppM	See #1 below
Control voltage range	+0.3		+3.0	V <sub>DC</sub>	As rated
Center control voltage		+1.65		V	For RMT center frequency
Monotonic linearity			10	%	Positive transfer slope
Input impedance	50			kΩ	Control voltage pin
Modulation bandwidth	50			kHz	-3dB

#### Notes

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1. As specified. APR is relative to the nominal output frequency F<sub>N</sub>; APR is inclusive (net) of frequency deviation due to stability.

## **Output Enable / Disable Function**

Parameter	Min.	Тур.	Max.	Units	Notes
Input voltage, output enable	3.0			V	or open
Input voltage, output high impedance			0.3	V	Output is high impendance

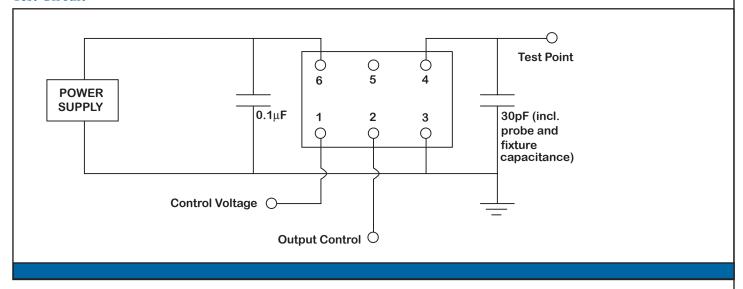




## **Absolute Maximum Ratings**

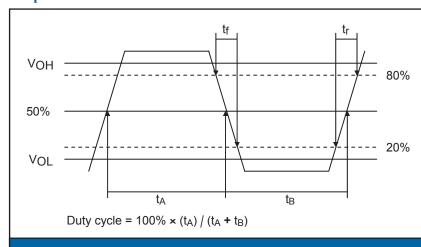
Parameter	Min.	Тур.	Max.	Units	Notes
Storage temperature	-55		+125	°C	
Control voltage range	-0.5		V <sub>DD</sub> +0.5	V	

## **Test Circuit**

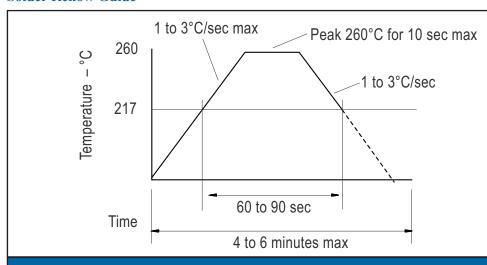




## **Output Waveform**



#### **Solder Reflow Guide**



## **Reliability Test Ratings**

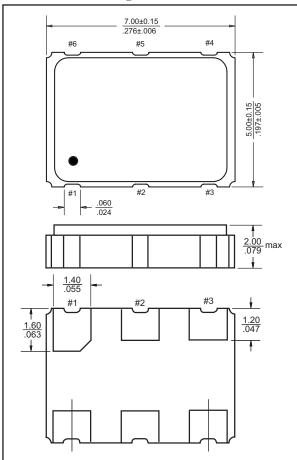
This product is rated under the following test conditions:

Туре	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

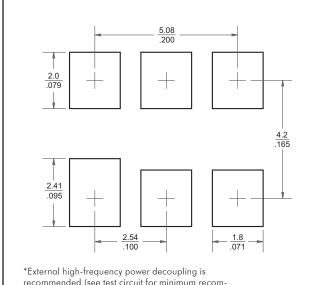




## **Mechanical Drawings**



### **Recommended Land Pattern\***



recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

**Marking LINE 1: Marking LINE 2:** 

**Marking LINE 3:** 

**ST1307xxx** 12.3456

(SaRonix, Model, Option Codes)

(Frequency in MHz) YYWWx

(Pin 1, Year, Week, Origin)

\*\* Exact location of items may vary