DATA SHEET

PCA9555

16-bit I^2C and SMBus I/O port with interrupt

Product data

2001 May 07

File under Integrated Circuits ICL03

Philips
Semiconductors

PHILIPS

16-bit I²C and SMBus I/O port with interrupt PCA9555

FEATURES

- Operating power supply voltage range of 2.3 V–5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active low interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 to 400 kHz clock frequency
- EDS protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The PCA9555 is a silicon CMOS circuit which provides parallel input/output expansion for SMBus and I²C applications. The PCA9555 consists of an input port register, output port register, a polarity inversion register, and a configuration register, and an I²C/SMBus interface.

The system master can invert the PCA9555 input data by writing to the active HIGH polarity inversion register. The system master can enable the I/Os as either inputs or outputs by writing to the configuration register.

The power-on reset sets the registers to their default values and initializes the device state machine.

The three programmable hardware address pins (A0, A1, A2) allows up to 8 devices to be used simultaneously on a single I²C bus or system management bus.

PIN CONFIGURATION

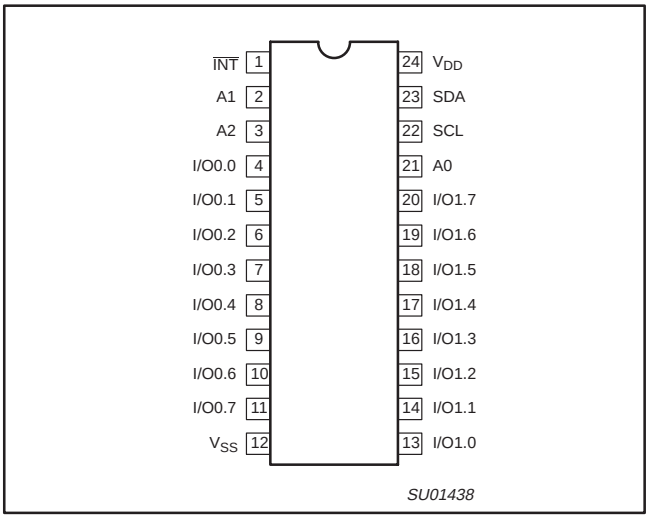


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{INT}$	Interrupt output (open drain)
2	A1	Address input 1
3	A2	Address input 2
4	I/O0.0	I/O0.0
5	I/O0.1	I/O0.1
6	I/O0.2	I/O0.2
7	I/O0.3	I/O0.3
8	I/O0.4	I/O0.4
9	I/O0.5	I/O0.5
10	I/O0.6	I/O0.6
11	I/O0.7	I/O0.7
12	V_{SS}	Supply ground
13	I/O1.0	I/O1.0
14	I/O1.1	I/O1.1
15	I/O1.2	I/O1.2
16	I/O1.3	I/O1.3
17	I/O1.4	I/O1.4
18	I/O1.5	I/O1.5
19	I/O1.6	I/O1.6
20	I/O1.7	I/O1.7
21	A0	Address input 0
22	SCL	Serial clock line
23	SDA	Serial data line
24	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic SO24 Type I	–40 to +85 °C	PCA9555D	SOT137-1
24-Pin Plastic SSOP24 Type II	–40 to +85 °C	PCA9555DB	SOT340-1
24-Pin Plastic TSSOP24 Type I	–40 to +85 °C	PCA9555PW	SOT355-1

BLOCK DIAGRAM

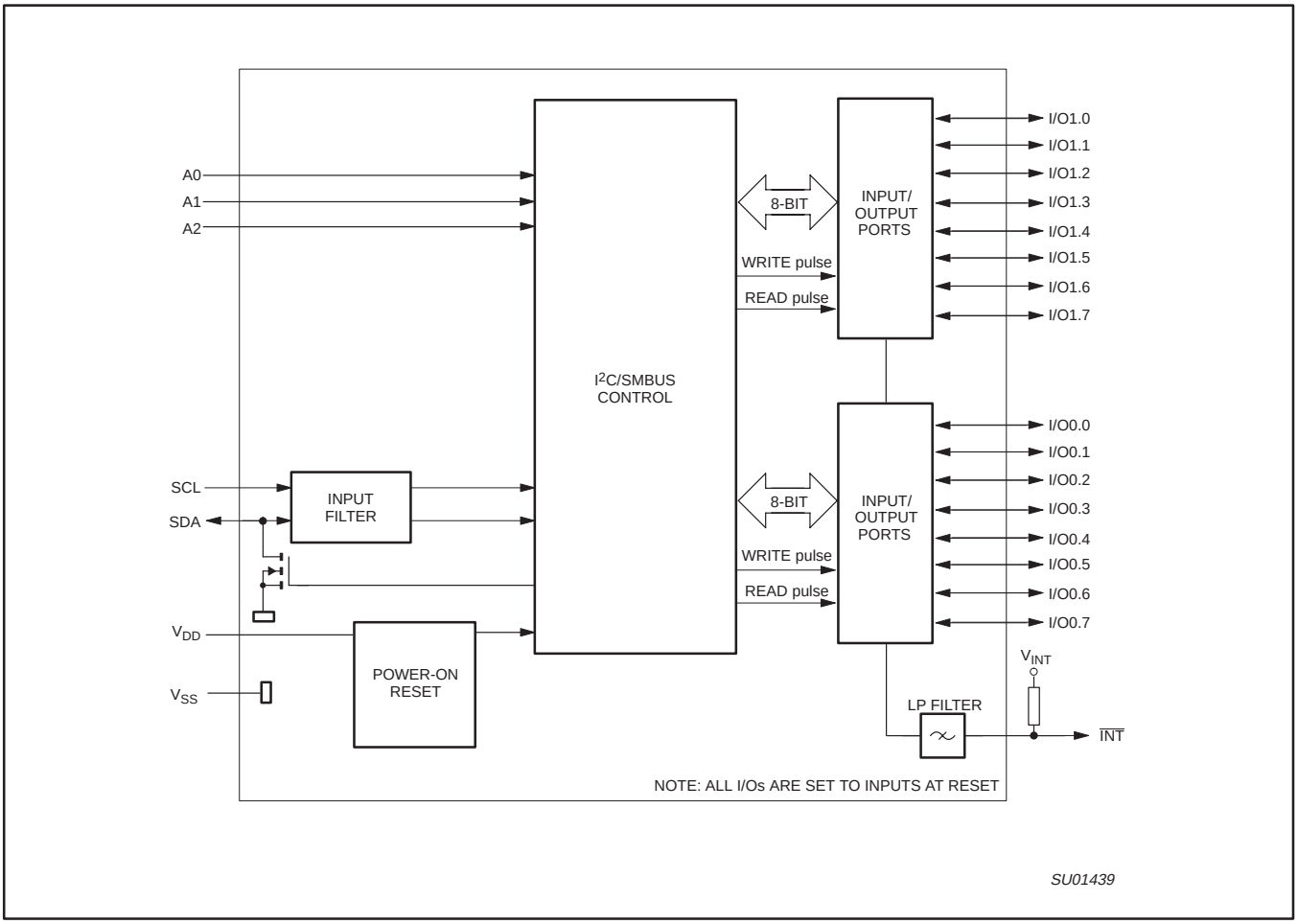
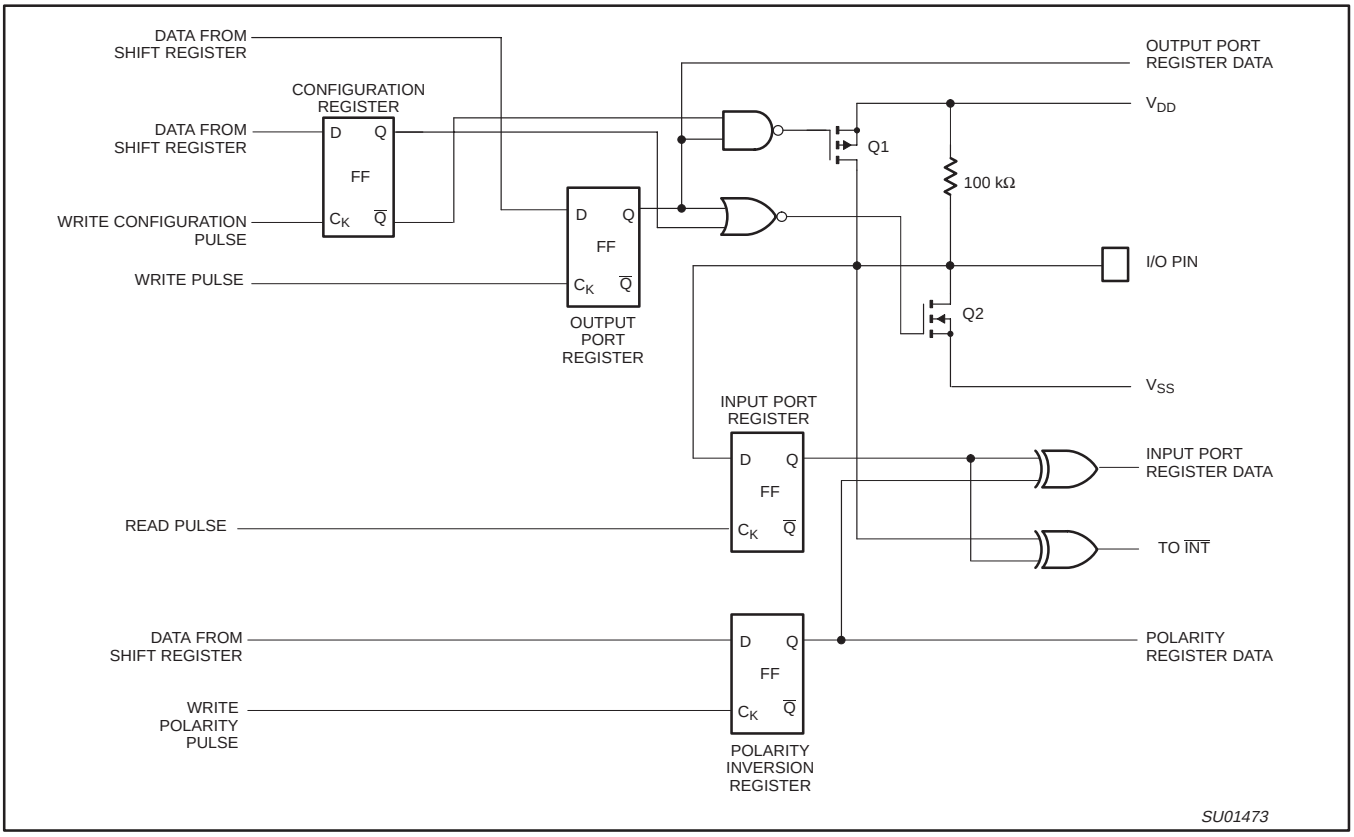


Figure 2. Block diagram

SIMPLIFIED SCHEMATIC OF I/Os



NOTE: At Power-on Reset, all registers return to default values.

Figure 3. Simplified schematic of I/Os

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance path that exists between the pin and either V_{DD} or V_{SS}.

REGISTERS

Command Byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Registers 0 and 1 – Input Port Registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

Registers 2 and 3 – Output Port Registers

bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
default	1	1	1	1	1	1	1	1
bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
default	1	1	1	1	1	1	1	1

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Registers 4 and 5 – Polarity Inversion Registers

bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
default	0	0	0	0	0	0	0	0
bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the Input Port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Registers 6 and 7 – Configuration Registers

bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
default	1	1	1	1	1	1	1	1
bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to V_{DD} at each pin. At reset the device's ports are inputs with a pull-up to V_{DD}.

POWER-ON RESET

When power is applied to V_{DD}, an internal power-on reset holds the PCA9555 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9555 registers and SMBus state machine will initialize to their default states.

DEVICE ADDRESS

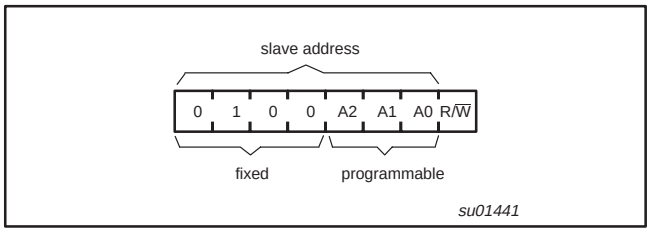


Figure 4. PCA9555 address

BUS TRANSACTIONS

Writing to the port registers

Data is transmitted to the PCA9555 by sending the device address and setting the least significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figures and). For example, if the first byte is sent to Output Port (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Reading the port registers

In order to read data from the PCA9555, the bus master must first send the PCA9555 address with the least significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again but this time, the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9555 (see Figures 7 and 8). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

Interrupt Output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read (see Figure 8). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

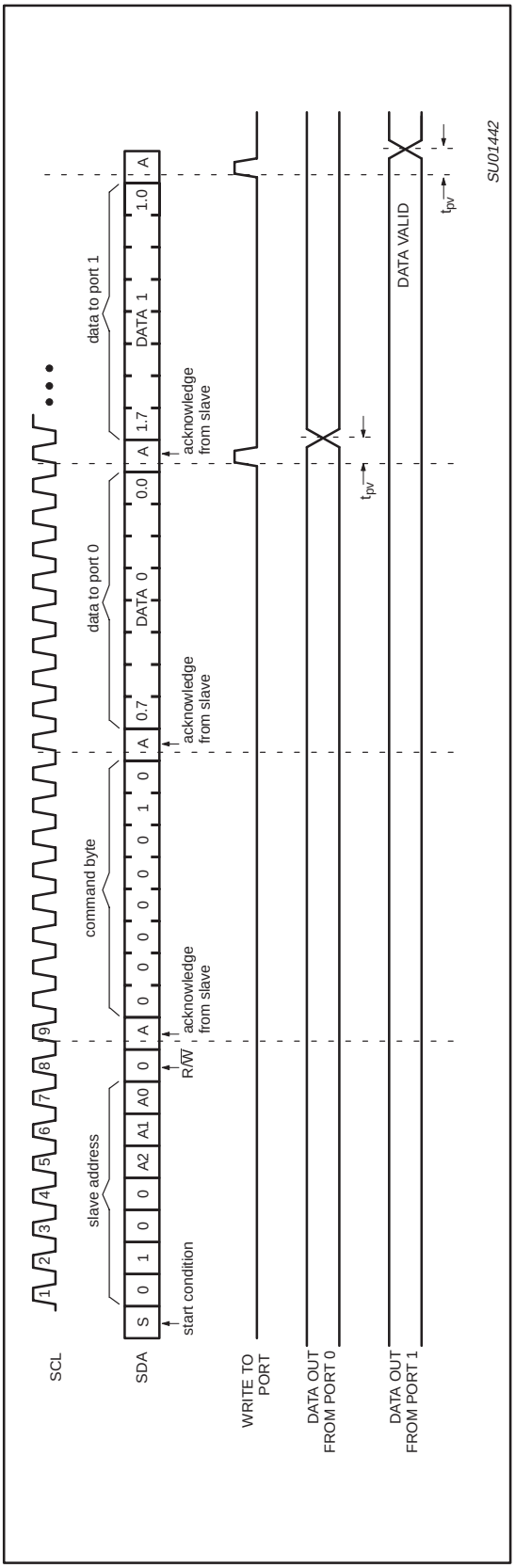


Figure 5. WRITE to output port registers

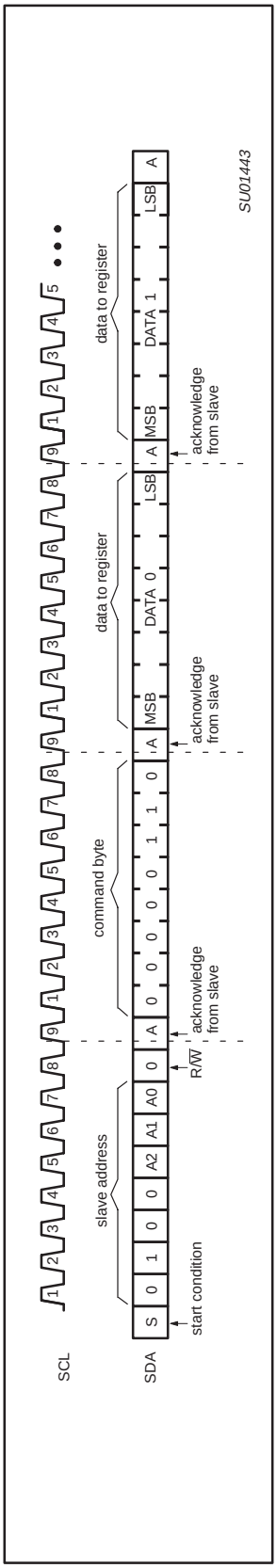
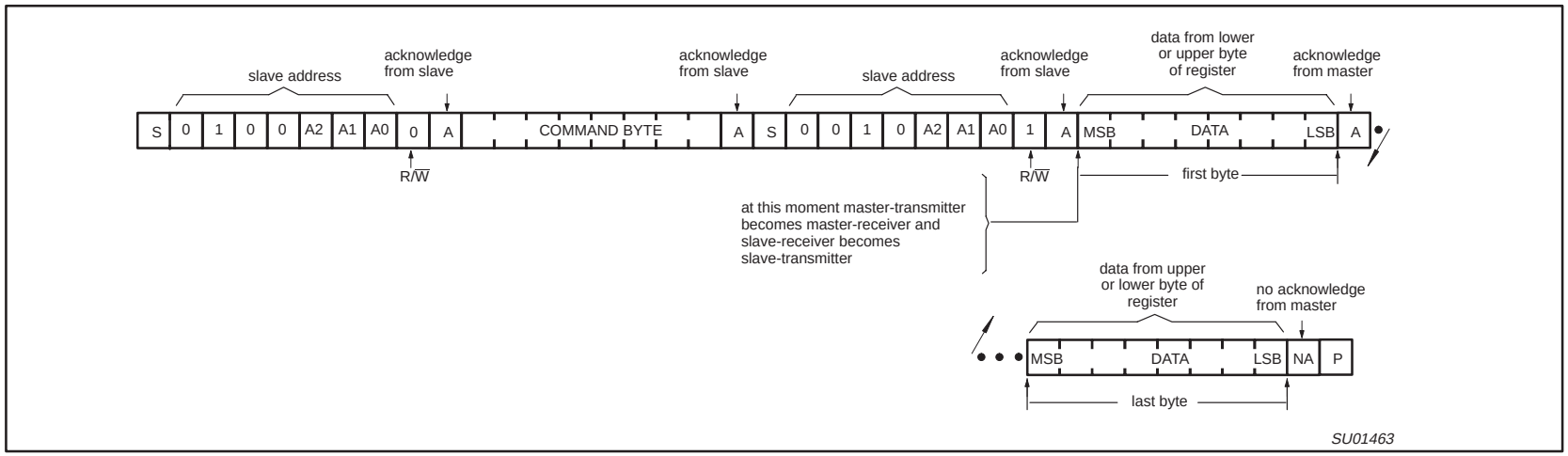
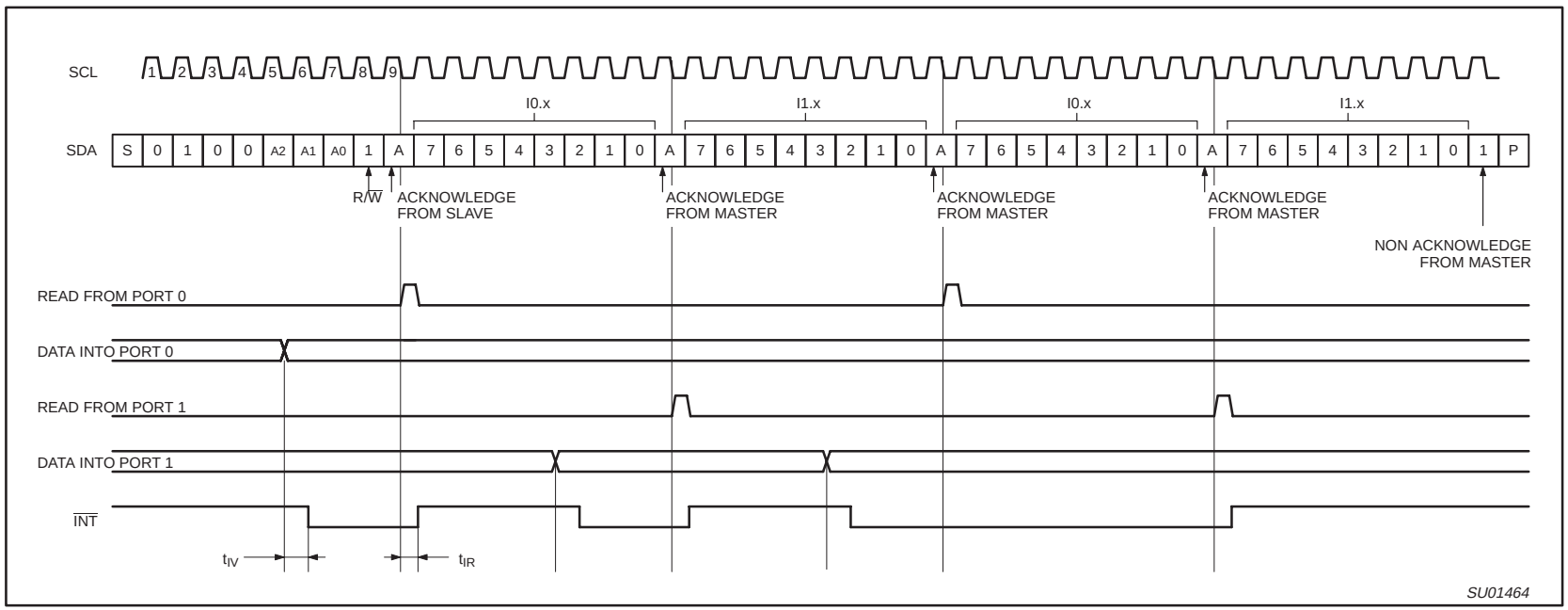


Figure 6. WRITE to configuration registers



NOTE: Transfer can be stopped at any time by a STOP condition.

Figure 7. READ from register



NOTES: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode).
It is assumed that the command byte has previously been set to 00 (read input port port register).

Figure 8. READ input port register

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
$V_{I/O}$	DC input current on an I/O		V_{SS} – 0.5	6	V
$I_{I/O}$	DC output current on an I/O		—	± 50	mA
I_I	DC input current		—	± 20	mA
I_{DD}	Supply current		—	160	mA
I_{SS}	Supply current		—	200	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.3 V; no load; $V_I = V_{DD}$; f_{SCL} = 100 kHz	—	0	1	µA
I_{DDL}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	—	700	µA
I_{DDH}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	—	1.5	mA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS}	1.25	—	1.65	V
input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.5 V; V_{DD} = 2.3–5.5 V; Note 1	8	8–20	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3–5.5 V; Note 1	10	10–24	—	mA
V_{OH}	HIGH level output voltage	I_{OH} = –8 mA; V_{DD} = 2.3 V; Note 2	1.8	—	—	V
		I_{OH} = –10 mA; V_{DD} = 2.3 V; Note 2	1.7	—	—	V
		I_{OH} = –8 mA; V_{DD} = 3.0 V; Note 2	2.6	—	—	V
		I_{OH} = –10 mA; V_{DD} = 3.0 V; Note 2	2.5	—	—	V
		I_{OH} = –8 mA; V_{DD} = 4.75 V; Note 2	4.1	—	—	V
		I_{OH} = –10 mA; V_{DD} = 4.75 V; Note 2	4.0	—	—	V
I_{IH}	Input leakage current	V_{DD} = 3.6 V; $V_I = V_{DD}$	—	—	1	µA
I_{IL}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	—	—	–100	µA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA

NOTES:

1. The total current sunk by all I/Os must be limited to 200 mA.
2. The total current sourced by all I/Os must be limited to 160 mA.

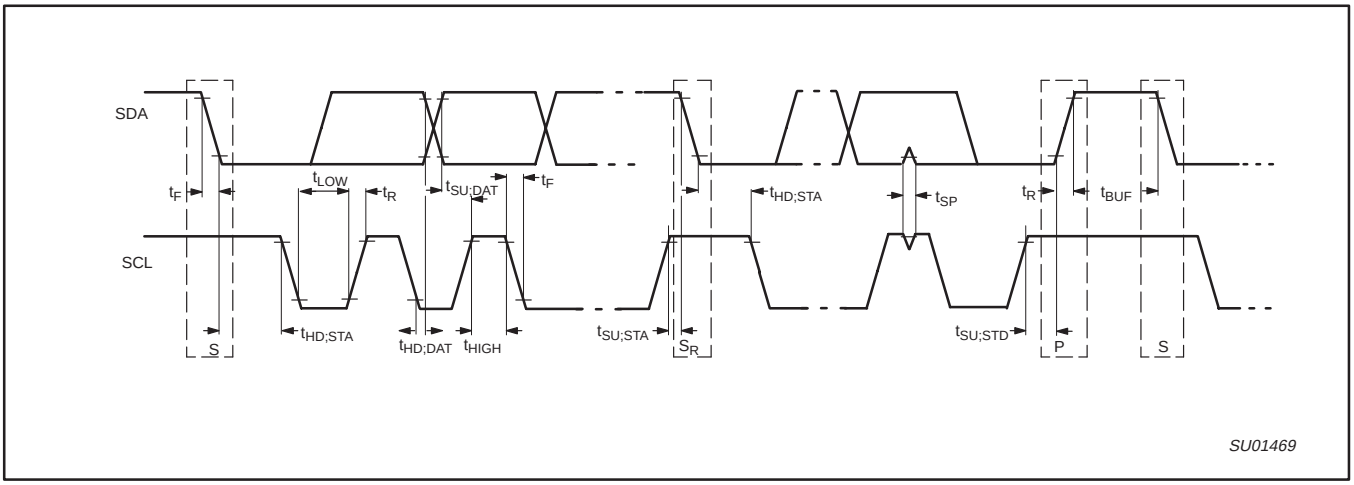


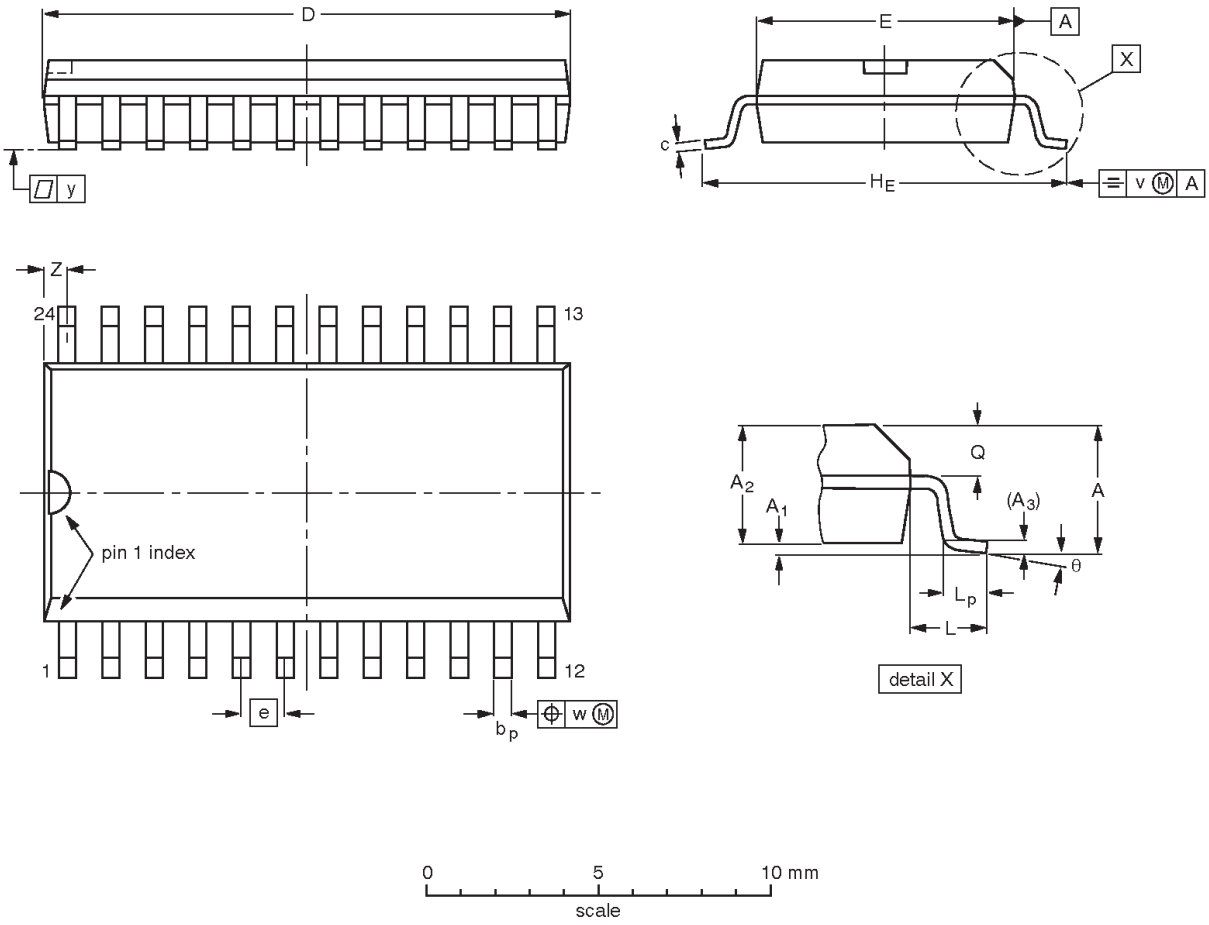
Figure 9. Definition of timing

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{VD;ACK}$	Valid time of ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	$20 + 0.1C_b$ [1]	300	ns
t_R	Clock/Data rise time	—	1000	$20 + 0.1C_b$ [1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	150	—	150	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Interrupt Timing						
t_{IV}	Interrupt valid	—	4	—	4	µs
t_{IR}	Interrupt reset	—	4	—	4	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

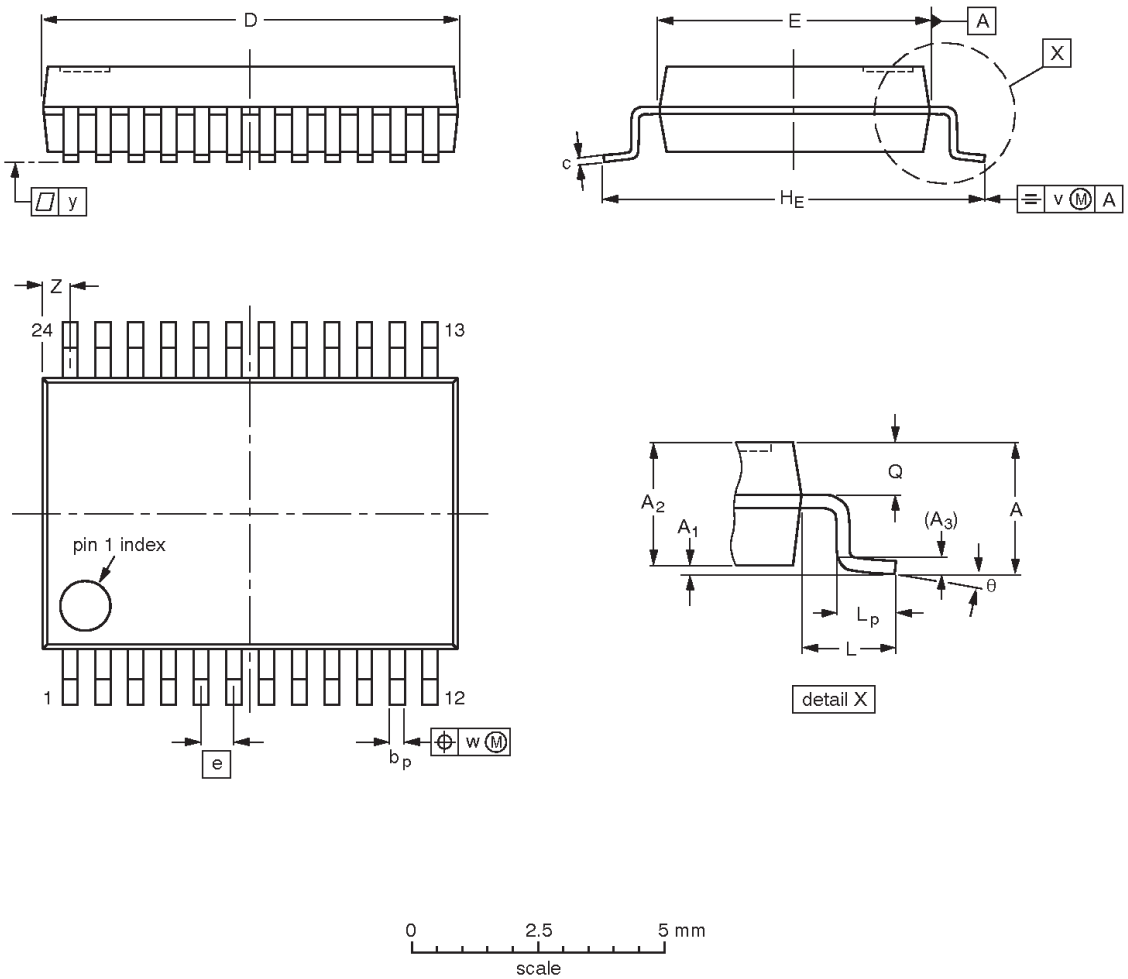
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

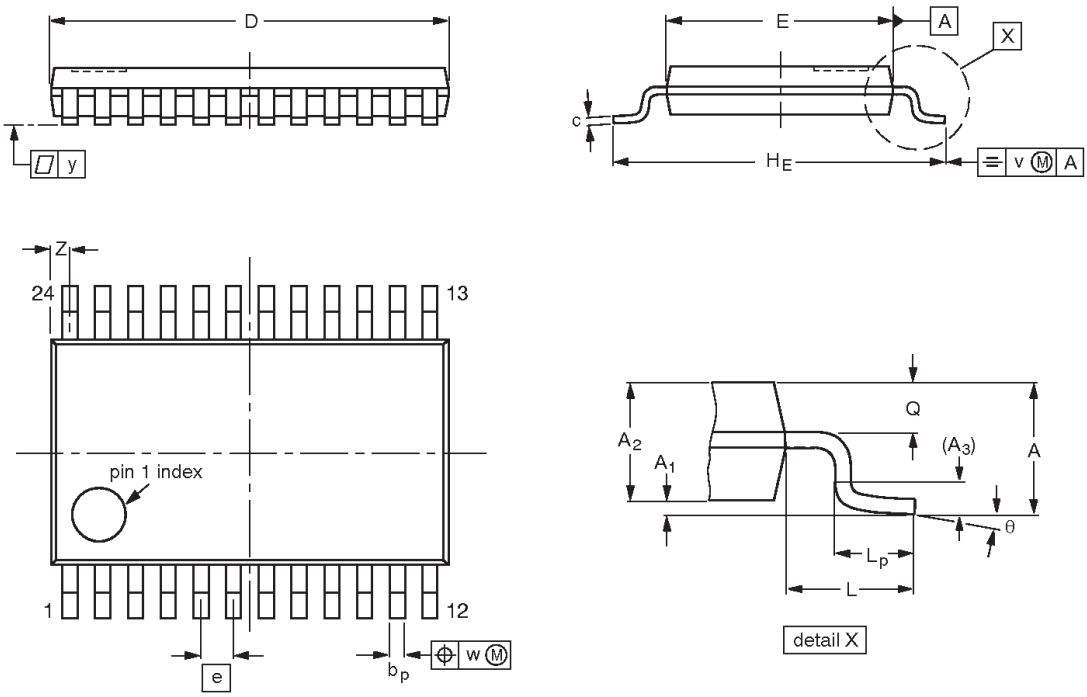
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

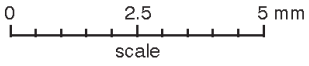
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

16-bit I²C and SMBus I/O port with interrupt PCA9555

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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