LOW SKEW, 1-TO-6, CRYSTAL-TO-LVDS FANOUT BUFFER

ICS8546-01

General Description

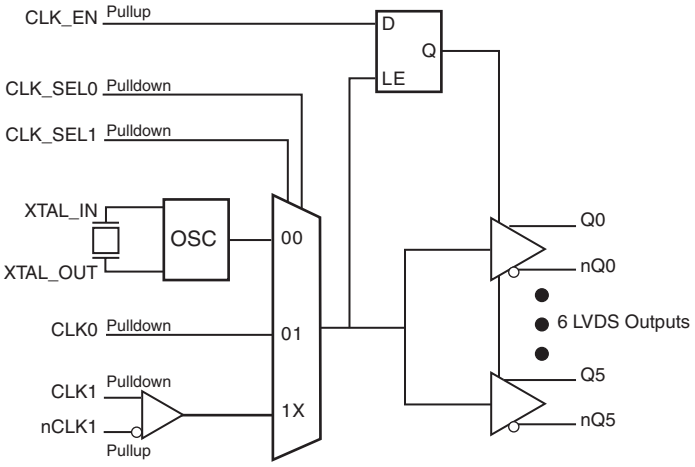
The ICS8546-01 is a low skew, high performance 1-to-6 Crystal Oscillator-to-LVDS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8546-01 has selectable crystal, single ended or differential clock inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to LVDS levels. The CLK1, nCLK1 pair can accept most standard differential input levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/ deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8546-01 ideal for those applications demanding well defined performance and repeatability.

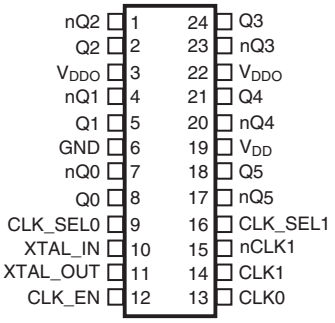
Features

- Six 3.3V or 2.5V LVDS outputs
- Selectable crystal oscillator, differential CLK1/nCLK1 pair or LVCMOS/LVTTL clock input
- CLK1/nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 266MHz
- Crystal frequency range: 14MHz - 40MHz
- Output skew: 60ps (typical)
- Part-to-part skew: 450ps (typical
- Propagation delay: 2.25ns (typical)
- Full 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS844S0258-07

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
6	GND	Power		Power supply ground.
7, 8	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels.
10, 11	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3.
13	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
14	CLK1	Input	Pulldown	Non-inverting differential clock input.
15	nCLK1	Input	Pullup	Inverting differential clock input.
17, 18	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
19	V_{DD}	Power		Positive supply pin.
20, 21	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Control Input Function Table

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q0:Q5**	**nQ0:nQ5**
0	0	0	XTAL	Disabled	Disabled
0	0	1	CLK0	Disabled	Disabled
0	1	X	CLK1/nCLK1	Disabled	Disabled
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1/nCLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in *Figure 1.*

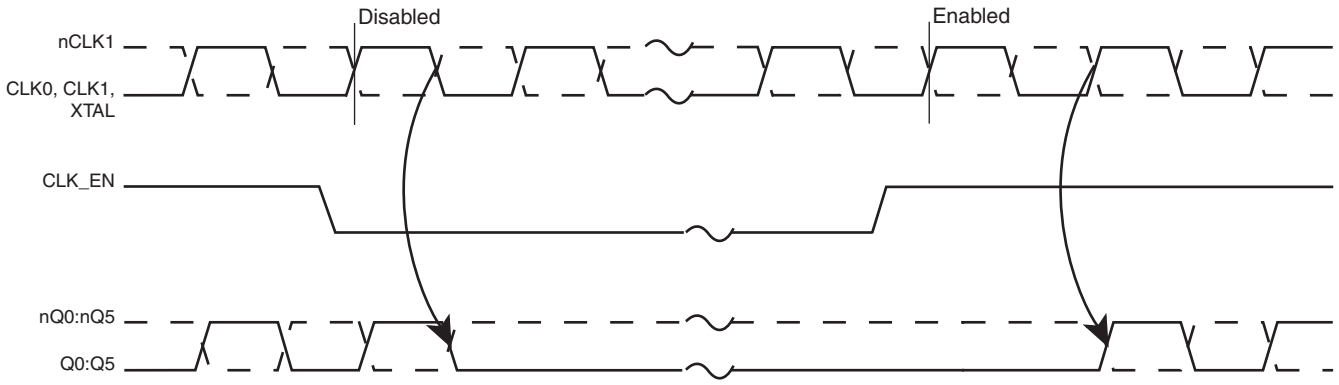


Figure 1. CLK_EN Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	87.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			105		mA
I_{DDO}	Power Supply Current			TBD		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			105		mA
I_{DDO}	Power Supply Current			TBD		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465V$	-0.3		0.8	V
			$V_{DD} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL[0:1]	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		CLK_EN	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL[0:1]	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		CLK_EN	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		CLK1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$				µA
I_{IL}	Input Low Current	nCLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		CLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4E. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			440		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4F. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.3		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		14		40	MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					266	MHz
t_{PD}	Propagation Delay; NOTE 1A, 1B	CLK1/nCLK1			1.85		ns
		CLK0			2		ns
*t*jit	Buffer Additive Phase Jitter, RMS		155.52MHz, Integration Range: 12kHz – 20MHz		0.23		ps
*t*sk(o)	Output Skew; NOTE 2, 3				60		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				350		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		450		ps
odc	Output Duty Cycle				50		%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 5A	*f* = 150MHz		-69		dB
		NOTE 5B	*f* = 250MHz		-70		dB

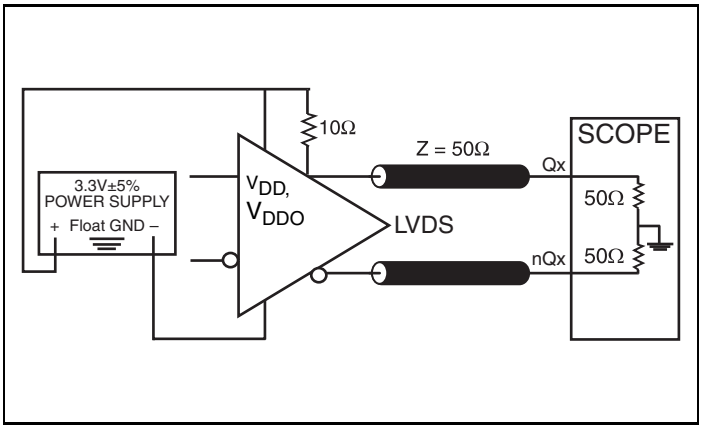
All parameters measured at f_{MAX} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from $V_{DD}/2$ input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5A: CLK0(150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.
NOTE 5B: CLK0(250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

Table 6B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

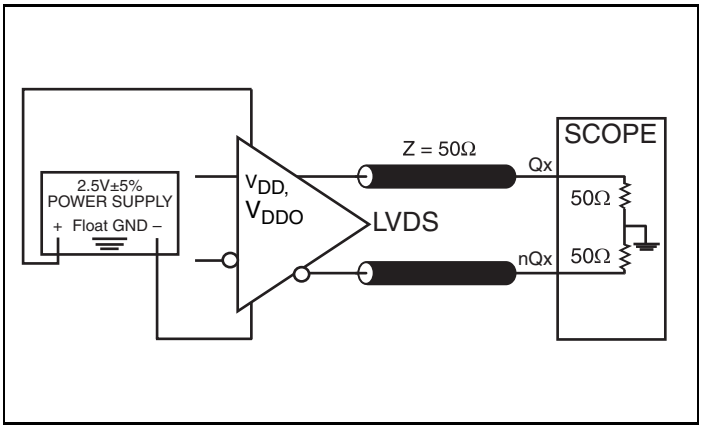
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					266	MHz
t_{PD}	Propagation Delay; NOTE 1A, 1B	CLK1/nCLK1			1.85		ns
		CLK0			2.1		ns
*t*jit	Buffer Additive Phase Jitter, RMS		155.52MHz, Integration Range: 12kHz – 20MHz		0.22		ps
*t*sk(o)	Output Skew; NOTE 2, 3				60		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				350		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		450		ps
odc	Output Duty Cycle				50		%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 5A	*f* = 150MHz		-43		dB
		NOTE 5B	*f* = 250MHz		-38		dB

All parameters measured at f_{MAX} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from $V_{DD}/2$ input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5A: CLK0(150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.
NOTE 5B: CLK0(250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

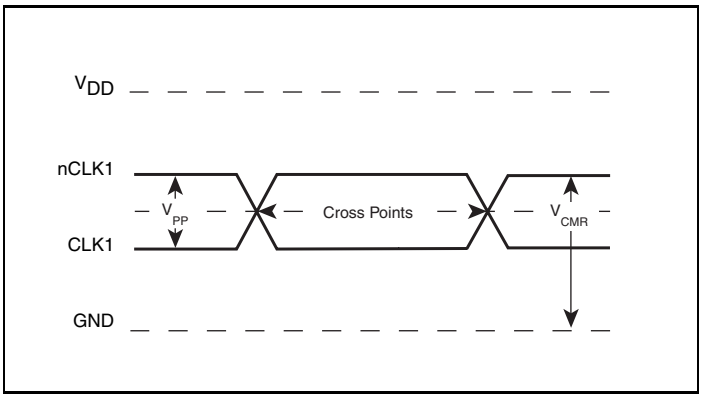
Parameter Measurement Information



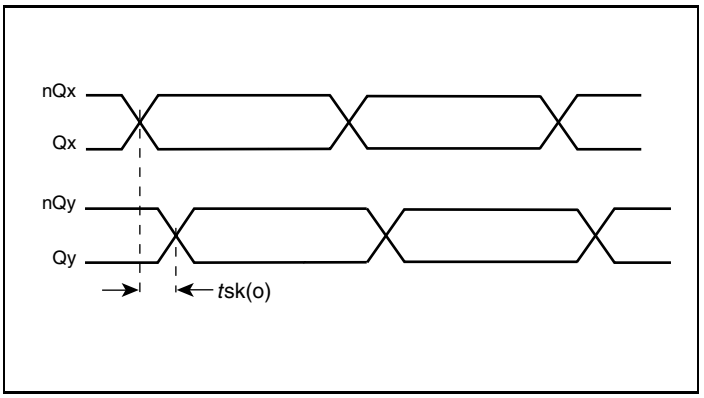
3.3V LVDS Output Load AC Test Circuit



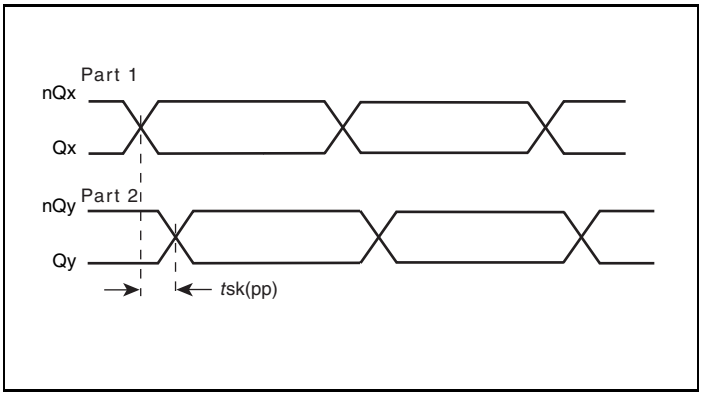
2.5V LVDS Output Load AC Test Circuit



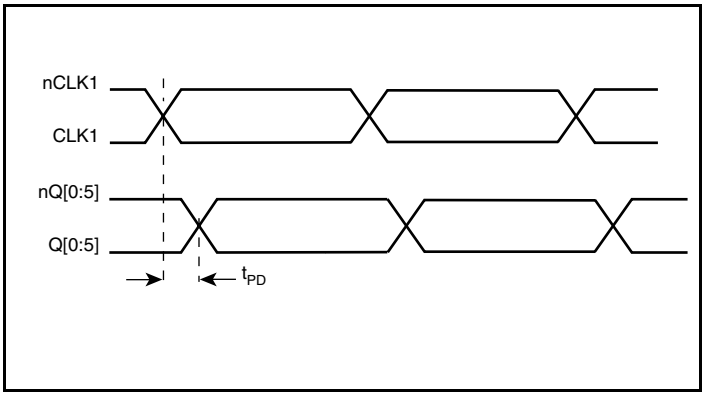
Differential Input Level



Output Skew

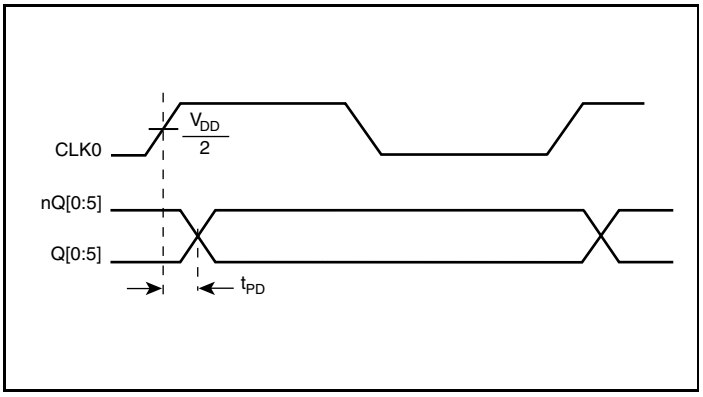


Part-to-Part Skew

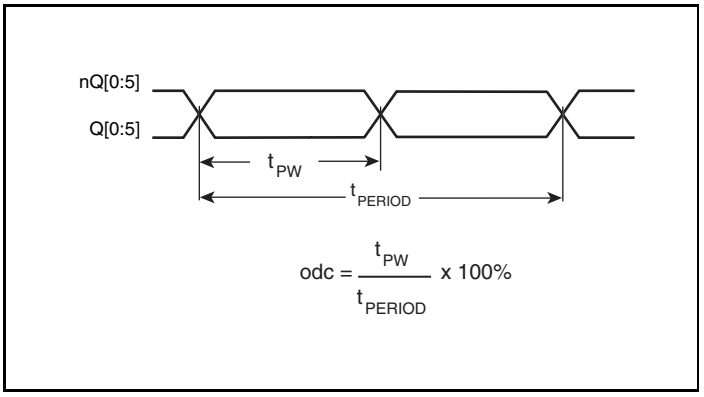


Propagation Delay (Differential Input)

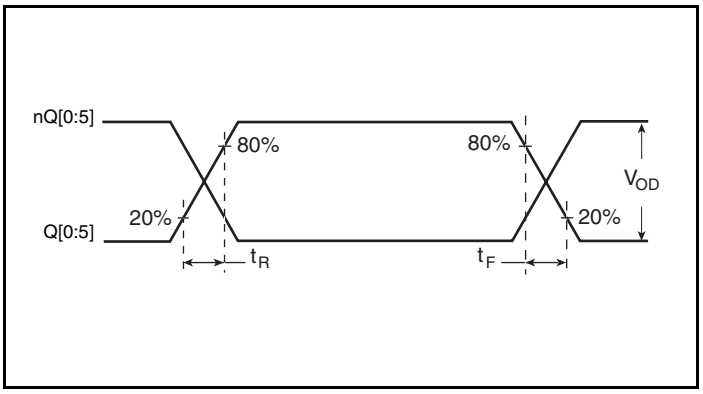
Parameter Measurement Information, continued



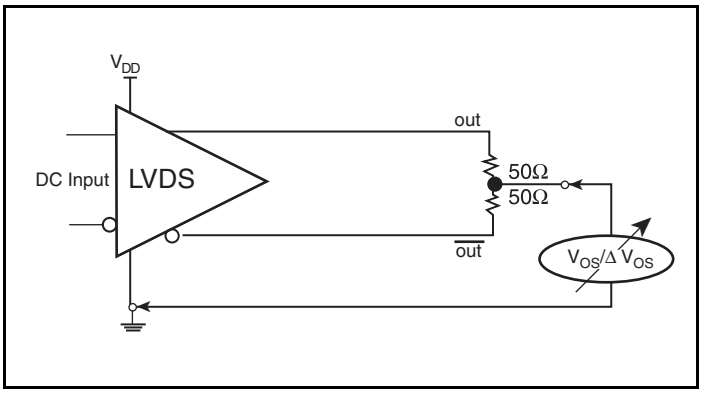
Propagation Delay (LVCMOS Input)



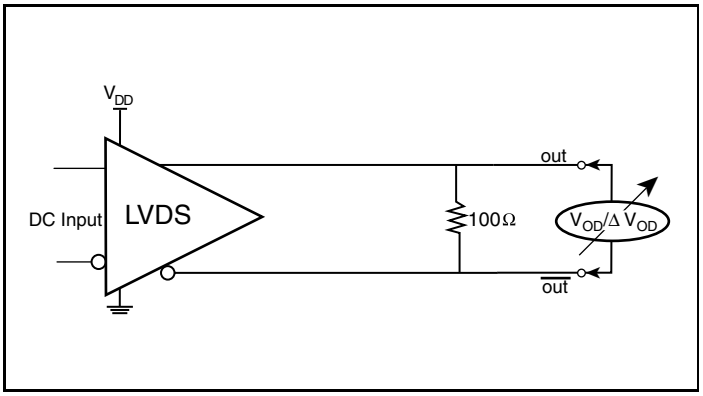
Differential Output Voltage Setup



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a test clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

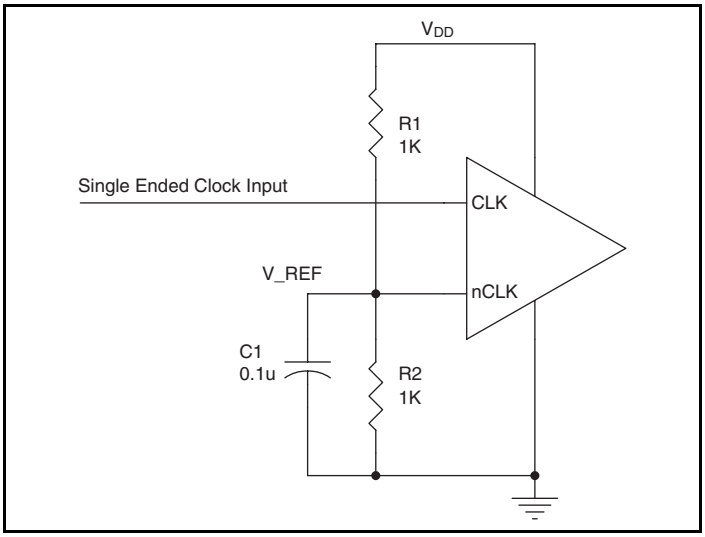


Figure 2. Single-Ended Signal Driving Differential Input

Crystal Input Interface

The ICS8546-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

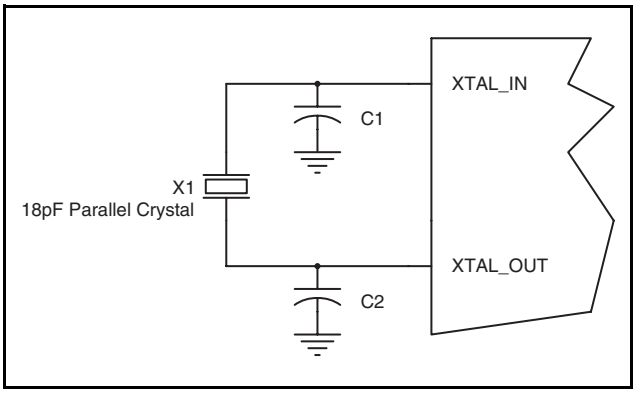


Figure 3. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

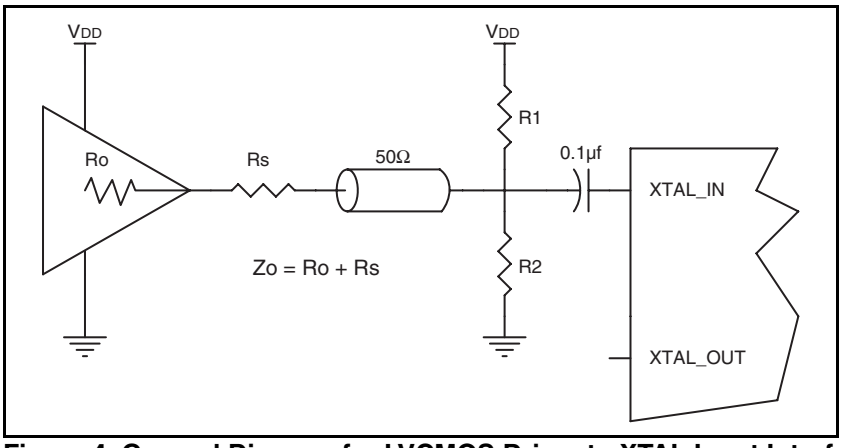


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

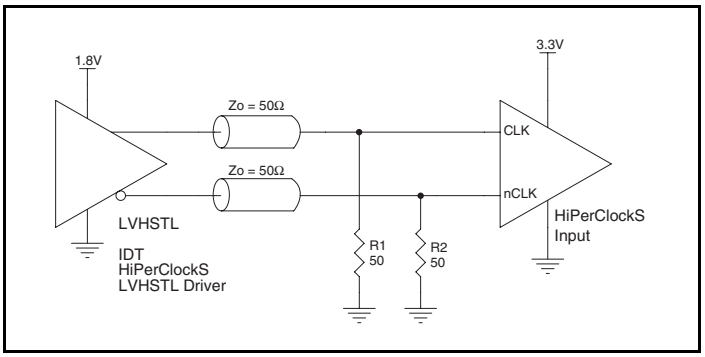


Figure 5A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

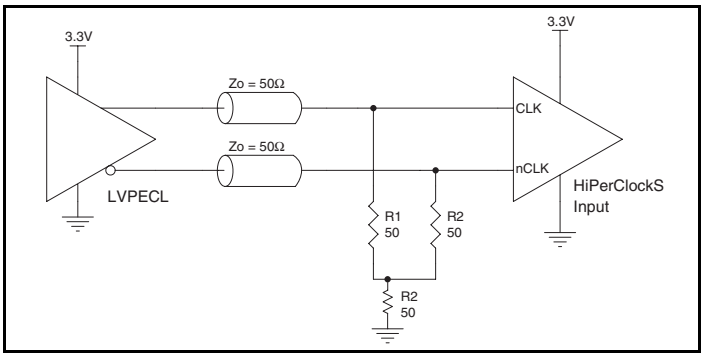


Figure 5B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

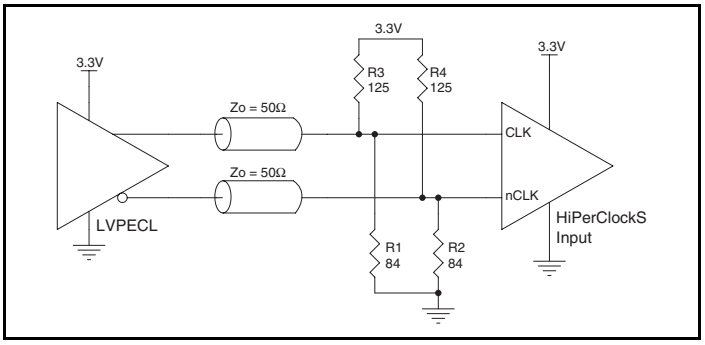


Figure 5C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

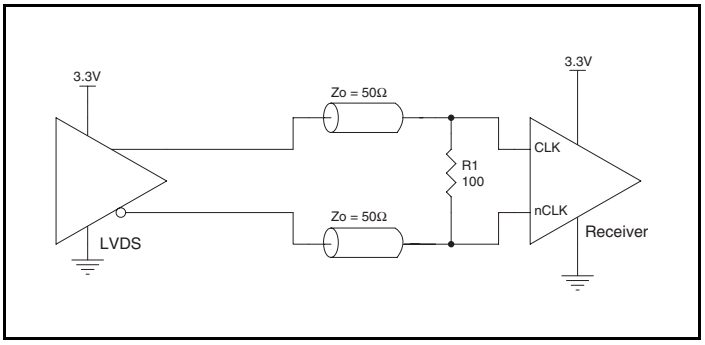


Figure 5D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

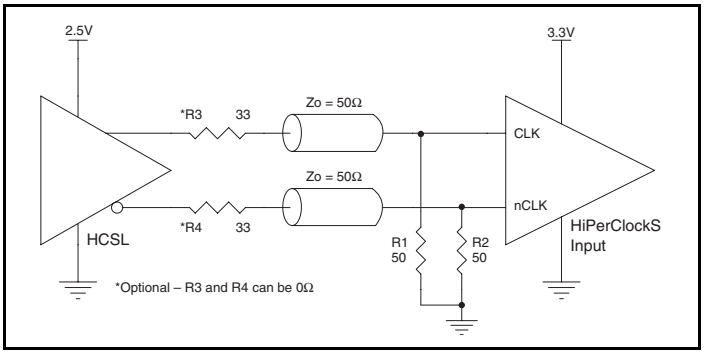


Figure 5E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

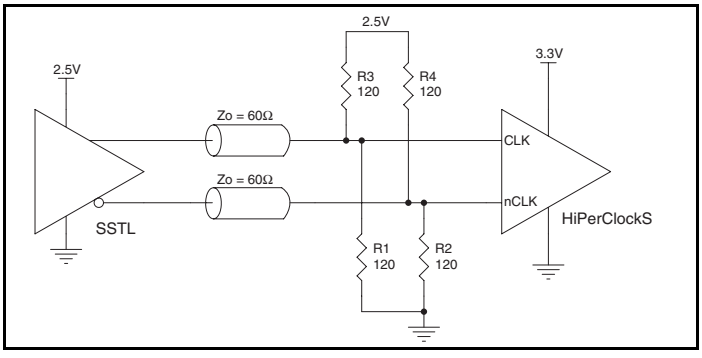


Figure 5F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 6.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

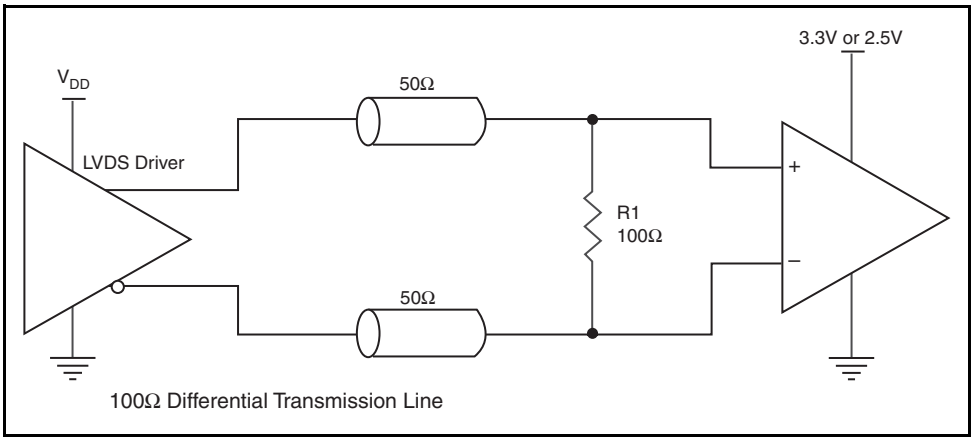


Figure 6. Typical LVDS Driver Termination

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

Transistor Count

The transistor count for ICS8546-01 is: 513

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

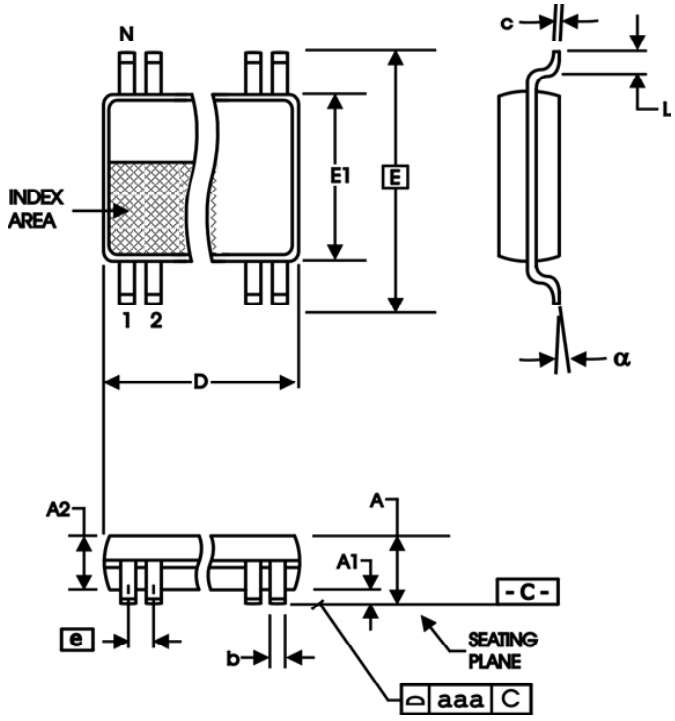


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8546AG-01	ICS8546AG-01	24 Lead TSSOP	Tube	0°C to 70°C
8546AG-01T	ICS8546AG-01	24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
8546AG-01LF	TBD	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
8546AG-01LFT	TBD	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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