DS1284/DS1286
Watchdog Timekeepers

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GENERAL DESCRIPTION

The DS1284/DS1286 watchdog timekeepers are self-contained real-time clocks, alarms, watchdog timers, and interval timers in a 28-pin JEDEC DIP and encapsulated DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal, which eliminates the need for any external circuitry. The DS1284 requires an external quartz crystal and a V_{BAT} source, which could be a lithium battery. Data contained within 64 8-bit registers can be read or written in the same manner as byte-wide static RAM. Data is maintained in the watchdog timekeeper by intelligent control circuitry that detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over 10 years in the absence of V_{CC}. Watchdog timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap year. The DS1284/DS1286 operate in either 24-hour or 12-hour format with an AM/PM indicator. The devices provide alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real-time alarm provides for preset times of up to one week.

FEATURES

- Keeps Track of Hundredths of Seconds, Seconds, Minutes, Hours, Days, Date of the Month, Months, and Years; Valid Leap Year Compensation Up to 2100
- Watchdog Timer Restarts an Out-of-Control Processor
- Alarm Function Schedules Real-Time-Related Activities
- Embedded Lithium Energy Cell Maintains Time, Watchdog, User RAM, and Alarm Information
- Programmable Interrupts and Square-Wave Outputs Maintain JEDEC Footprint
- All Registers are Individually Addressable via the Address and Data Bus
- Accuracy is Better than ±1 Minute/Month at +25°C (EDIP)
- Greater than 10 Years of Timekeeping in the Absence of V_{CC}
- 50 Bytes of User NV RAM
- Underwriters Laboratory (UL) Recognized
- -40°C to +85°C Industrial Temperature Range Option

Pin Configurations appear at end of data sheet.

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1284	0°C to +70°C	5.0	28 DIP (600 mils)	DS1284
DS1284N	-40°C to +85°C	5.0	28 DIP (600 mils)	DS1284 N
DS1284Q	0°C to +70°C	5.0	28 PLCC	DS1284Q
DS1284Q+	0°C to +70°C	5.0	28 PLCC	DS1284Q
DS1284Q/T&R	0°C to +70°C	5.0	28 PLCC/Tape and Reel	DS1284Q
DS1284Q+T&R	0°C to +70°C	5.0	28 PLCC/Tape and Reel	DS1284Q
DS1284QN	-40°C to +85°C	5.0	28 PLCC	DS1284QN
DS1284QN+	-40°C to +85°C	5.0	28 PLCC	DS1284QN
DS1284QN/T&R	-40°C to +85°C	5.0	28 PLCC/Tape and Reel	DS1284QN
DS1284QN+T&R	-40°C to +85°C	5.0	28 PLCC/Tape and Reel	DS1284QN
DS1286	0°C to +70°C	5.0	28 EDIP (720 mils)	DS1286
DS1286I	-40°C to +85°C	5.0	28 EDIP (720 mils)	DS1286 IND
DS1286I+	-40°C to +85°C	5.0	28 EDIP (720 mils)	DS1286 IND

+ Denotes a lead(Pb)-free/RoHS-compliant package.

** A "+" anywhere on the top mark indicates a lead-free package.*

OPERATION—READ REGISTERS

The DS1284/DS1286 execute a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) and $\overline{OE}$ (output enable) are active (low). The unique address specified by the six address inputs (A0–A5) defines which of the 64 registers is to be accessed. Valid data is available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable, provided that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION—WRITE REGISTERS

The DS1284/DS1286 are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active-low state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient data setup (t_{DS}) and data hold time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION

The watchdog timekeeper provides full functional capability when V_{CC} is greater than V_{TP}. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1284/DS1286 constantly monitor V_{CC}. Should the supply voltage decay, the watchdog timekeeper automatically write protects itself, and all inputs to the registers become “don’t care.” Both $\overline{INTA}$ and $\overline{INTB}$ (INTB) are open-drain outputs. The two interrupts and the internal clock continue to run regardless of the level of V_{CC}. However, it is important to ensure that the pullup resistors used with the interrupt pins are never pulled up to a value greater than V_{CC} + 0.3V. As V_{CC} falls below the battery voltage, a power-switching circuit turns on the lithium energy source to maintain the clock and timer data functionality. Also ensure that during this time (battery-backup mode), the voltage present at $\overline{INTA}$ and $\overline{INTB}$ (INTB) never exceeds the battery voltage. If the active-high mode is selected for $\overline{INTB}$ (INTB), this pin only goes high in the presence of V_{CC}. During power-up, when V_{CC} rises above approximately 3.0V, the power-switching circuit connects external V_{CC} and disconnects the V_{BAT} energy source. Normal operation can resume after V_{CC} exceeds V_{TP} for t_{REC}.

WATCHDOG TIMEKEEPER REGISTERS

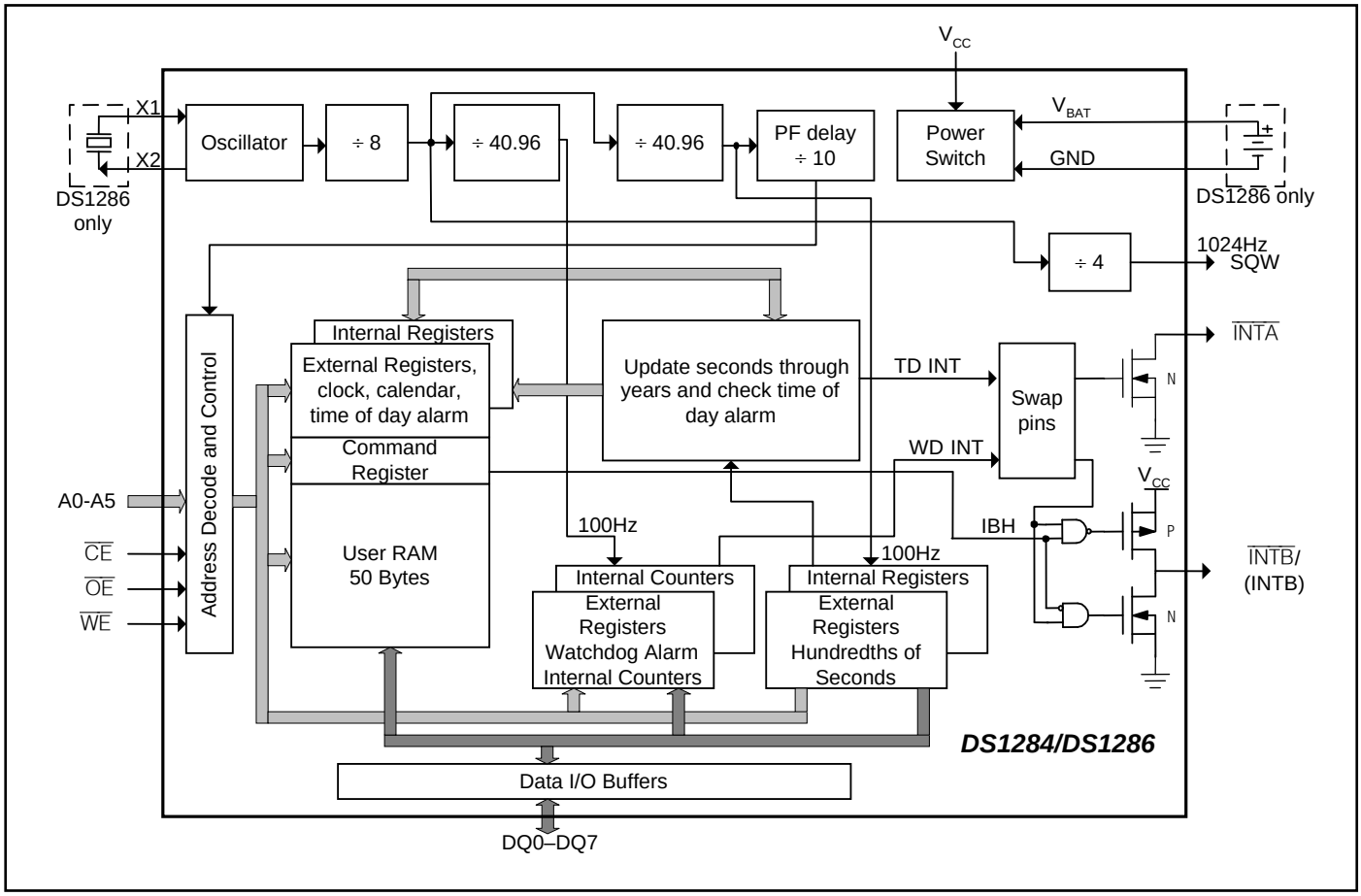
The watchdog timekeeper has 64 8-bits-wide registers that contain all the timekeeping, alarm, watchdog, control, and data information. The clock, calendar, alarm, and watchdog registers are memory locations that contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions, except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The command register bits are affected by both internal and external functions. This register is discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time-of-day and date information (see Figure 2). Time-of-day information is stored in binary-coded decimal (BCD). Registers 3, 5, and 7 contain the time-of-day alarm information. Time-of-day alarm information is stored in BCD. Register B is the command register and information in this register is binary. Registers C and D are the watchdog alarm registers and information stored in these two registers is in BCD. Registers E to 3F are user bytes and can be used to contain data at the user’s discretion.

PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	EDIP	PLCC		
1	1	1	$\overline{\text{INTA}}$	Active-Low Interrupt Output A. This open-drain pin requires a pullup resistor for proper operation.
2, 3	—	2, 3	X1, X2	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real Time Clocks.*
4	2, 3, 4, 21, 24, 25	4	N.C.	No Connection
5–10	5–10	5–10	A5–A0	Address Inputs
11, 12, 13, 15, 16–19	11, 12, 13, 15, 16–19	11, 12, 13, 15, 16–19	DQ0, DQ1, DQ2, DQ3, DQ4–DQ7	Data Input/Output
14, 21	14	14, 21	GND	Ground
20	20	20	$\overline{\text{CE}}$	Active-Low Chip-Enable Input
22	22	22	$\overline{\text{OE}}$	Active-Low Output-Enable Input
23	23	23	SQW	Square-Wave Output. Push-pull output. High impedance when V_{CC} is below V_{TP}.
24	—	24	$\overline{\text{RCLR}}$	Active-Low RAM Clear. Used to clear (set to logic 1) all 50 bytes of user NV RAM, but does not affect the registers involved with time, alarm, and watchdog functions. To clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic 0 (-0.3V to +0.8V) during battery-backup mode when V_{CC} is not applied. The $\overline{\text{RCLR}}$ function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.
25	—	25	V_{BAT}	Input for Any Standard 3V Lithium Cell or Other Energy Source. Input voltage must be held between the minimum and maximum limits for proper operation. The supply should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the V_{BAT} pin. Furthermore, a diode is not necessary because reverse charging current-protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing. This pin should be grounded but can be left floating.
26	26	26	$\overline{\text{INTB}}$ (INTB)	Active-Low (Active-High) Interrupt Output B. When the active-high state is selected (IBH = 1), an open-drain pullup transistor connected to V_{CC} sources current when the output is active. When the active-low state is selected (IBH = 0), an open-drain pulldown transistor connected to ground sinks current when the output is active. If active-high output operation is selected, a pulldown resistor is required for proper operation. When active-low output operation is selected, a pullup resistor is required for proper operation.
27	27	27	$\overline{\text{WE}}$	Active-Low Write-Enable Input

PIN			NAME	FUNCTION
DIP	EDIP	PLCC		
28	28	28	V_{CC}	Primary Power-Supply Input. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V_{CC} is below V_{TP}, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

Figure 1. Block Diagram



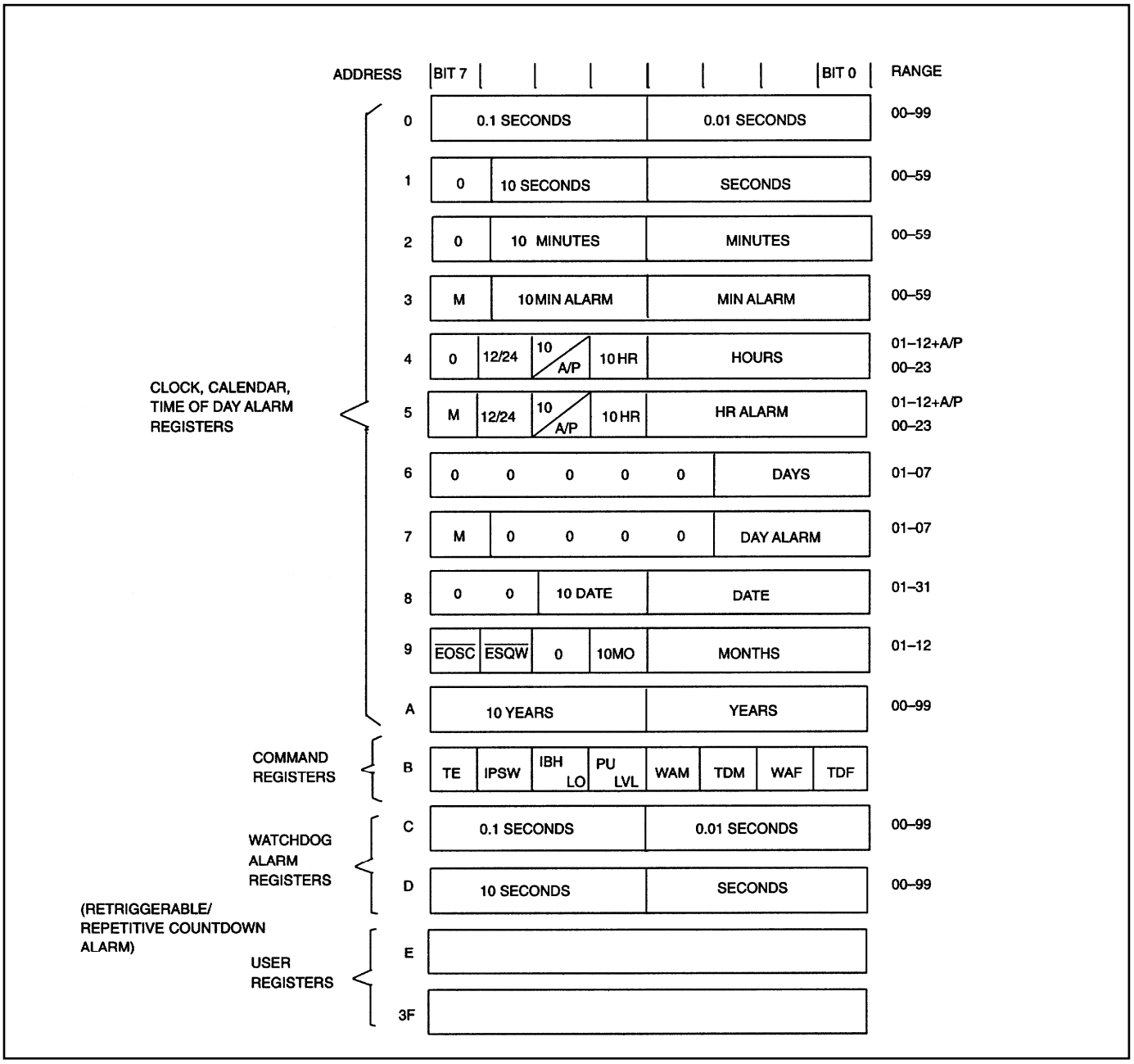
HUNDREDTHS-OF-SECONDS GENERATOR

The hundredths-of-seconds generator circuit shown in the *Block Diagram* (Figure 1) is a state machine that divides the incoming frequency (4096Hz) by 41 for 24 cycles and 40 for 1 cycle. This produces a 100Hz output that is slightly off during the short term, and is exactly correct every 250ms. The divide ratio is given by:

$$\text{Ratio} = [41 \times 24 + 40 \times 1] / 25 = 40.96$$

Thus, the long-term average frequency output is exactly 100Hz.

Figure 2. Watchdog Timekeeper Registers



TIME-OF-DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain time-of-day data in BCD. Ten bits within these eight registers are not used and always read 0 regardless of how they are written. Bits 6 and 7 in the months register (9) are binary bits. When set to logic 0, $\overline{\text{EOSC}}$ (bit 7) enables the RTC oscillator. This bit is set to logic 1 as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. The user normally turns this bit on during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the square-wave output (pin 23). When set to logic 0, the square-wave output pin outputs a 1024Hz square-wave signal. When set to logic 1, the square-wave output pin is in a high-impedance state. Bit 6 of the hours register is defined as the 12- or 24-hour select bit. When set to logic 1, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The time-of-day registers are updated every 0.01 seconds from the RTC, except when the TE bit (bit 7 of register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the watchdog timekeeper is to access the command register by doing a write cycle to address location 0B and setting the TE (transfer enable) bit to a logic 0. Doing so freezes the external time-of-day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic 1, puts the time-of-day registers back to being updated every 0.01 second. No time is lost in the RTC because the internal copy of the time-of-day register buffers is continually incremented while the external memory registers are frozen.

An alternate method of reading and writing the time-of-day registers is to ignore synchronization. However, any single read may give erroneous data as the RTC may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and time-of-day alarm is checked during the period that hundreds of seconds read 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the watchdog timekeeper.

TIME-OF-DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the time-of-day alarm registers. Bits 3, 4, 5, and 6 of register 7 always read 0 regardless of how they are written. Bit 7 of registers 3, 5, and 7 are mask bits (Figure 3). When all the mask bits are logic 0, a time-of-day alarm only occurs when registers 2, 4, and 6 match the values stored in registers 3, 5, and 7. An alarm is generated every day when bit 7 of register 7 is set to logic 1. Similarly, an alarm is generated every hour when bit 7 of registers 7 and 5 is set to logic 1. When bit 7 of registers 7, 5, and 3 is set to logic 1, an alarm occurs every minute when register 1 (seconds) rolls from 59 to 00.

Time-of-day alarm registers are written and read in the same format as the time-of-day registers. The time-of-day alarm flag and interrupt is always cleared when alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the watchdog alarm. The two registers contain a time count from to 99.99 seconds in BCD. The value written into the watchdog alarm registers can be written or read in any order. Any access to Registers C or D causes the watchdog alarm to reinitialize and clears the watchdog flag bit and the watchdog interrupt output. When a new value is entered or the watchdog registers are read, the watchdog timer starts counting down from the entered value to 0. When 0 is reached, the watchdog interrupt output goes to the active state. The watchdog timer countdown is interrupted and reinitialized back to the entered value every time either of the registers is accessed. In this manner, controlled periodic accesses to the watchdog timer can prevent the watchdog alarm from ever going to an active level. If access does not occur, the countdown alarm is repetitive. The watchdog alarm registers always read the entered value. The actual countdown register is internal and is not readable. Writing Registers C and D to 0 disables the watchdog alarm feature.

COMMAND REGISTER (0Bh)

Bit #:	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Name:	TE	IPSW	IBH	PU/LVL	WAM	TDM	WAF	TDF

Note: *The initial state of these bits is not defined.*

Bit 7: Transfer Enable (TE). This bit when set to logic 1 allows the internal time and date counters to update the user accessible registers. When set to logic 0, the external, user-accessible time and date registers remain static when being read or written, while the internal counters continue to run. The function of this bit is further described in the time-of-day registers section

Bit 6: Interrupt Pin Swap (IPSW). This bit directs which type of interrupt is present on interrupt pins $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ (INTB). When set to logic 1, $\overline{\text{INTA}}$ becomes the time-of-day alarm interrupt pin and $\overline{\text{INTB}}$ (INTB) becomes the watchdog interrupt pin. When bit 6 is set to logic 0, the interrupt functions are reversed such that the time-of-day alarm is output on $\overline{\text{INTB}}$ (INTB) and the watchdog interrupt is output on $\overline{\text{INTA}}$. Caution should be exercised when dynamically setting this bit as the interrupts are reversed even if in an active state.

Bit 5: Interrupt B Active High/Low (IBH). When bit 5 is set to logic 1, the B interrupt output sources current when active. When bit 5 is set to logic 0, the B interrupt output sinks current when active.

Bit 4: Pulse/Level Output (PU/LVL). When set to logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ sinks current for a minimum of 3ms and then releases. Output $\overline{\text{INTB}}$ (INTB) either sinks or sources current for a minimum of 3ms depending on the level of bit 5. The watchdog timer continues to run and WAF is cleared at the end of the pulse. When set to a logic 0, both $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ (INTB), when active, output an active low ($\overline{\text{INTB}}$ (INTB) active high when IBH = 1) until the interrupt is cleared.

Bit 3: Watchdog Alarm Mask (WAM). When this bit is written to logic 1, the watchdog interrupt output is deactivated regardless of the state of WAF. When WAM is set to logic 0 and the WAF bit is set to a 1, the watchdog interrupt output goes to the active state, which is determined by bits 1, 4, 5, and 6 of the command register.

Bit 2: Time-of-Day Alarm Mask (TDM). When this bit is written to logic 1, the time-of-day alarm-interrupt output is deactivated regardless of the state of TDF. When TDM is set to logic 0, the time-of-day

interrupt output goes to the active state, which is determined by bits 0, 4, 5, and 6 of the command register.

Bit 1: Watchdog Alarm Flag (WAF). When this bit is set internally to logic 1, a watchdog alarm has occurred. This bit is read-only and writing this register has no effect on the bit. The bit is reset when any of the watchdog alarm registers are accessed. The WAM bit has no effect on the operation of this bit. If pulse mode (PU/LVL = 1) is selected, the watchdog continues to run and the flag is internally written to 0 at the end of the pulse. The WAM bit has no effect on the operation of this bit.

Bit 0: Time-of-Day Alarm Flag (TDF). When this bit is set internally to a logic 1, indicates that a match with the time-of-day alarm registers has occurred. This bit is read-only and writing this register has no effect on the bit. The time of the alarm can be determined by reading the time-of-day alarm registers. The bit is reset when any of the time-of-day alarm registers are read. The TDM bit has no effect on the operation of this bit.

Figure 3. Time-of-Day Alarm Mask Bits

REGISTER			FUNCTION
(03h) MINUTES	(05h) HOURS	(07h) DAYS	
1	1	1	Alarm once per minute
0	1	1	Alarm when minutes match
0	0	1	Alarm when hours and minutes match
0	0	0	Alarm when hours, minutes, and days match

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Operating Temperature Range
Commercial……..0°C to +70°C
Industrial……...-40°C to +85°C
Storage Temperature Range……...-40°C to +85°C
Soldering Temperature……..……...See IPC/JEDEC J-STD-020 Specification (Note 13)

Stresses beyond those listed as "Absolute Maxim Ratings" may cause permanent damage to the device. These are stress ratings only, any functional operation of the device at these or any other conditions beyond the those indicated in operations section of the specifications is no implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C or 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10
V_{BAT} Input Voltage	V_{BAT}	2.4	3.0	3.5	V	10

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -40°C to +85°C or 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{LIO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE} > V_{CC}$ - 0.5	I_{CCS2}			4.0	mA	
Active Current	I_{CC}			15	mA	
Write-Protection Voltage	V_{TP}	1.088 x V_{BAT}	1.26 x V_{BAT}	1.324 x V_{BAT}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, V_{BAT} = 2.4V to 3.5V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current ($\overline{EOSC}$ = 0)	I_{BAT}		+0.5	+0.6	µA	

CAPACITANCE

(T_A = +25°C)

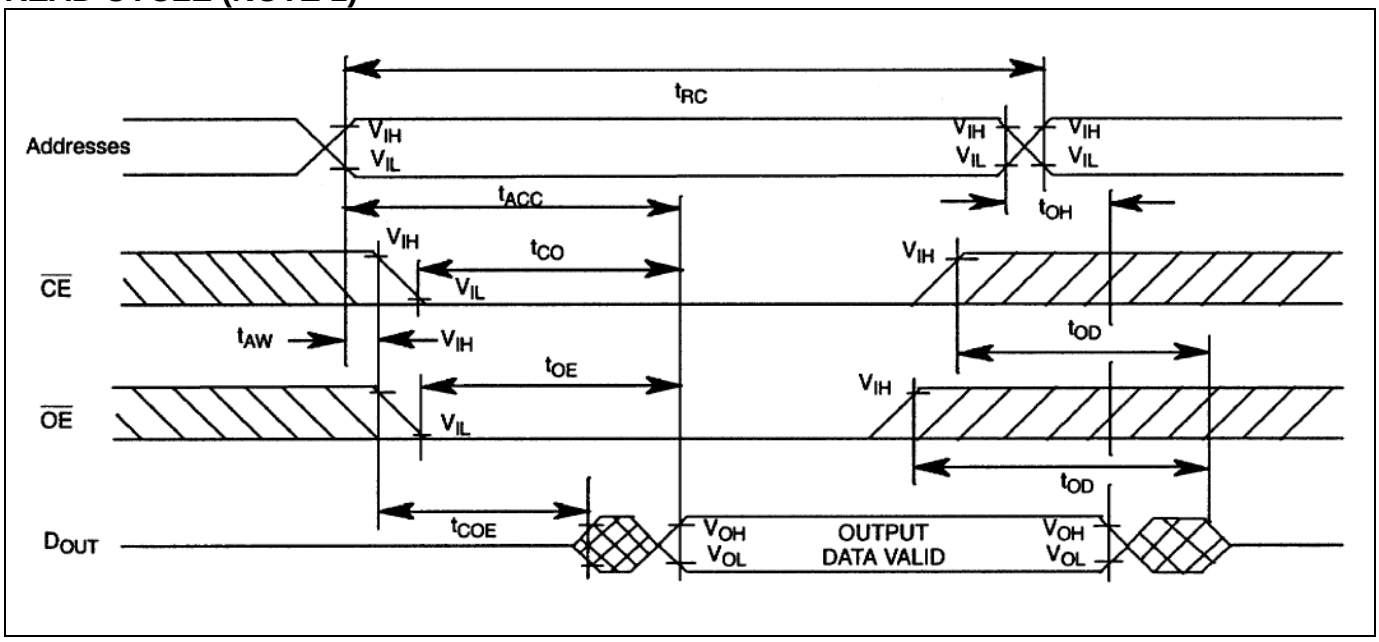
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	10	pF	
Output Capacitance	C_{OUT}		7	10	pF	
Input/Output Capacitance	$C_{I/O}$		7	10	pF	

AC ELECTRICAL CHARACTERISTICS

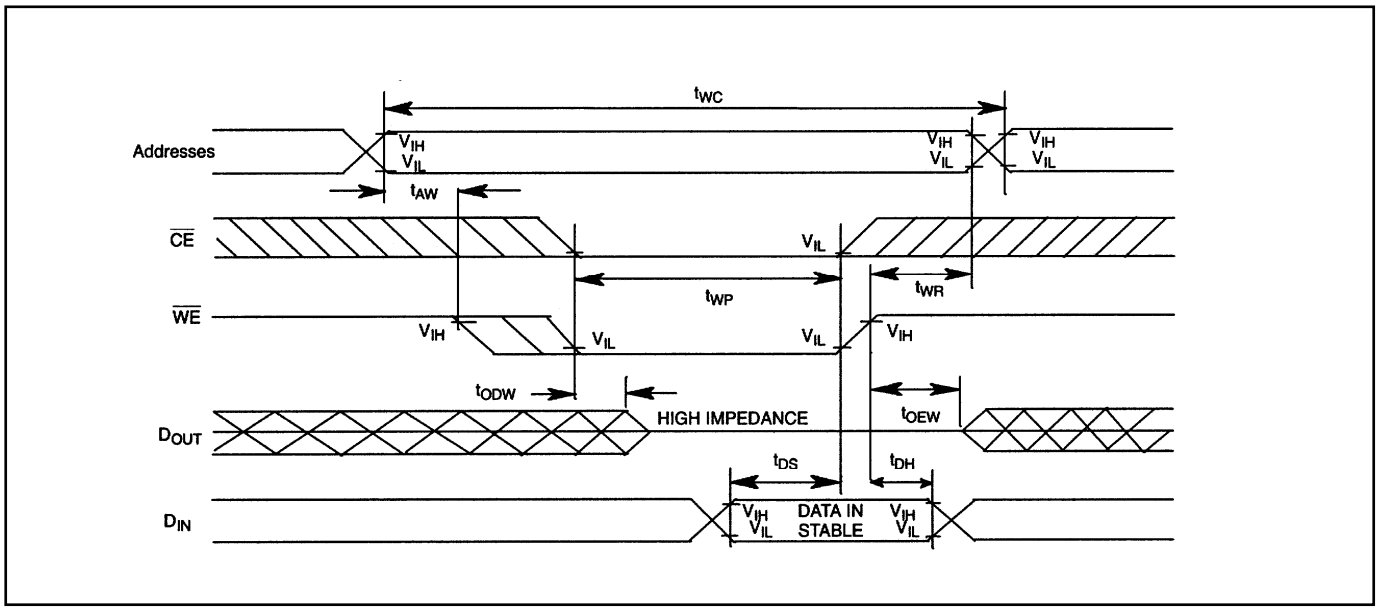
(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C or 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	1
Address Access Time	t_{ACC}			150	ns	
$\overline{CE}$ Access Time	t_{CO}			150	ns	
$\overline{OE}$ Access Time	t_{OE}			60	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High-Z from Deselect	t_{OD}			60	ns	
Output Hold from Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	140			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10			ns	
Data Setup Time	t_{DS}	45			ns	4
Data Hold Time	t_{DH}	0			ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3			ms	11,12

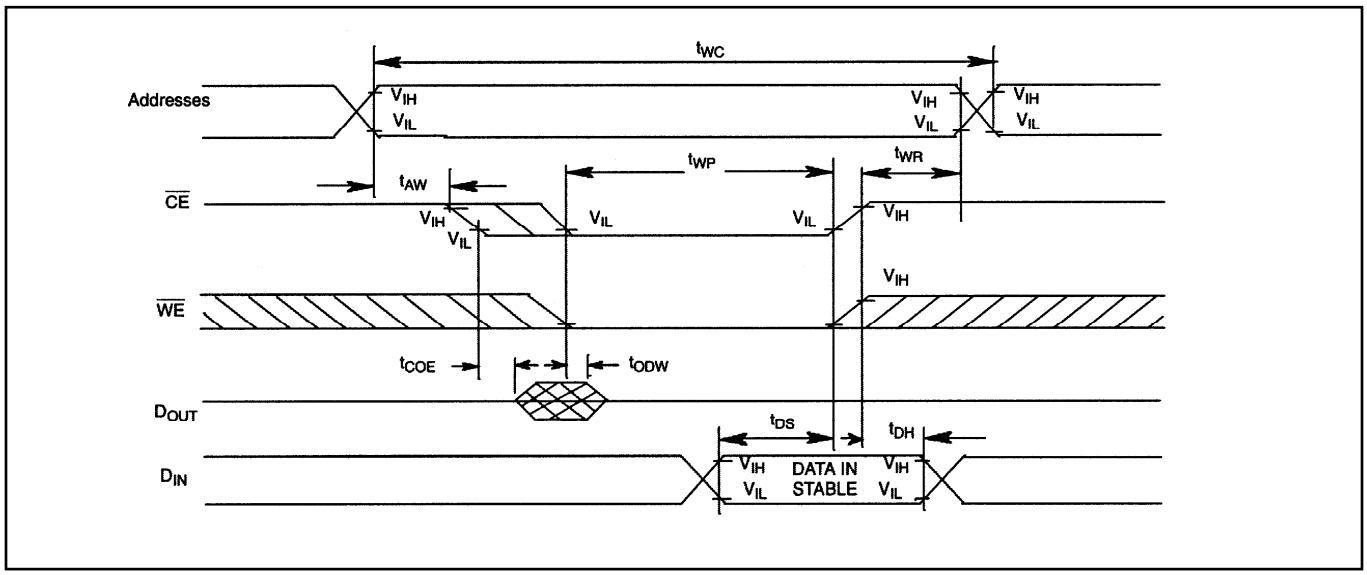
READ CYCLE (NOTE 1)



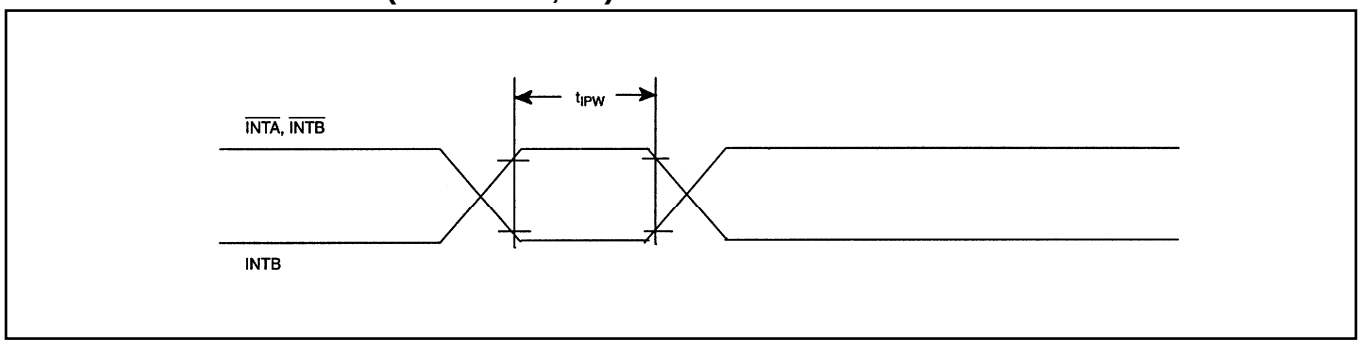
WRITE CYCLE 1 (NOTES 2, 6, 7)



WRITE CYCLE 2 (NOTES 2, 8)



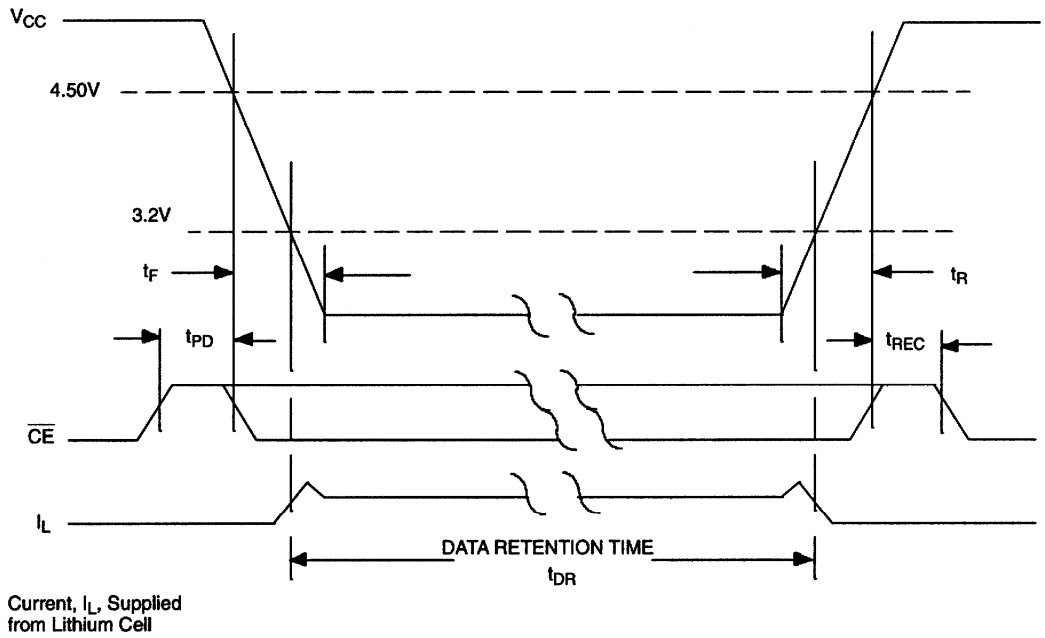
TIMING DIAGRAM: INTERRUPT OUTPUTS PULSE MODE (NOTES 11, 12)



POWER-UP/POWER-DOWN CONDITION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	350			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	100			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			150	ns	

POWER-DOWN/POWER-UP CONDITION



(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time (DS1286)	t_{DR}	10			years	9

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1284/DS1286 is marked with a four-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100ns on the alarm condition existing.
13. RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibrations are not used to prevent crystal damage.

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

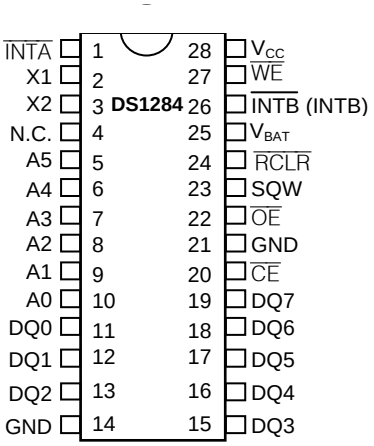
PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

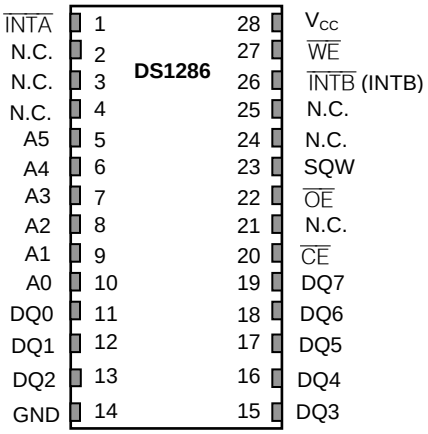
PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 PDIP	P28+9	**21-0044**
28 PLCC	Q28+11	**21-0049**
28 EDIP	MDP28+1	**21-0241**

PIN CONFIGURATIONS

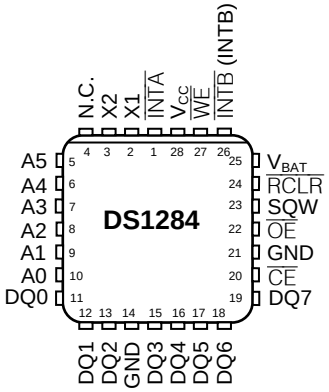
TOP VIEW



DIP
(600 mils)

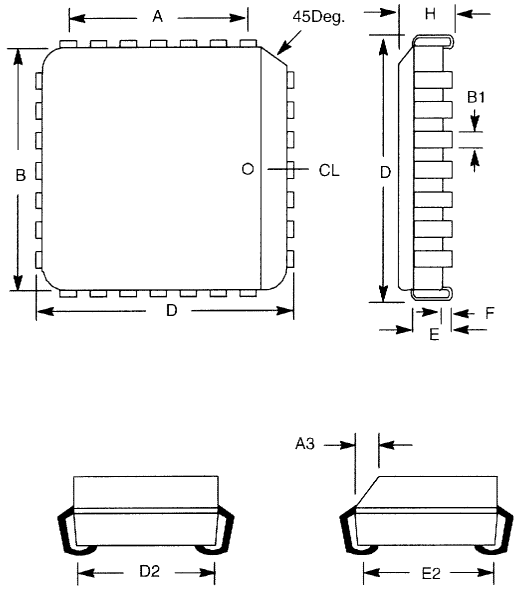


EDIP
(720 mils)



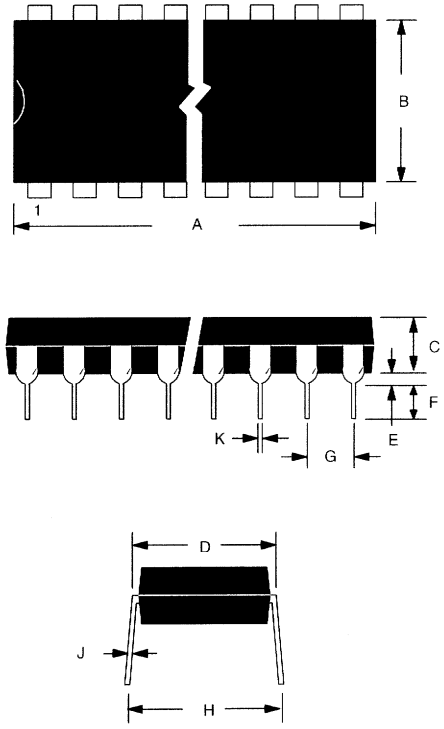
PLCC

PACKAGE INFORMATION



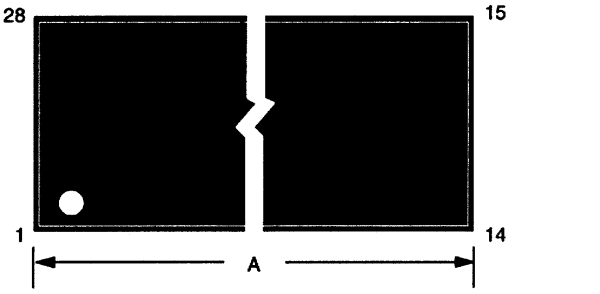
PKG	28-PIN PLCC	
DIM	MIN	MAX
A IN.	0.300 BSC	
MM	7.62	
B IN.	0.442	0.462
MM	17.68	11.73
D IN.	0.480	0.500
MM	12.2	12.7
D2 IN.	0.390	0.430
MM	9.91	10.92
E IN.	0.090	0.120
MM	2.29	3.05
E2 IN.	0.390	0.430
MM	9.91	10.92
F IN.	0.015	0.020
MM	0.38	0.518
H IN.	0.100	0.020
MM	2.54	0.518

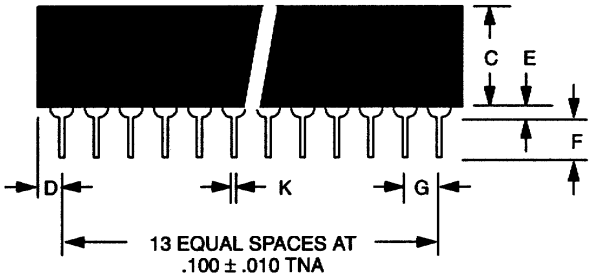
PACKAGE INFORMATION (continued)

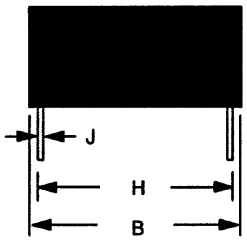


PKG	28-PIN DIP	
DIM	MIN	MAX
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

PACKAGE INFORMATION (continued)







PKG	28-PIN EDIP	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52`
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 21, 24, AND 25 ARE MISSING BY DESIGN.