

TPS54325 Step-Down Converter Evaluation Module User's Guide



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1 Introduction

This user's guide contains background information for the TPS54325 as well as support documentation for the TPS54325EVM evaluation module. Also included are the performance specifications, schematic and the bill of materials for the TPS54325EVM.

1.1 Background

The TPS54325 is a single, adaptive on-time D-CAP2™ mode synchronous buck converter. System designers may use the TPS54325 to complete various end equipment dc/dc converters with a low cost, low component count, low standby current solution. The main control loop for the TPS54325 uses the D-CAP2™ mode that optimized for low ESR output capacitors such as POSCAP, SP-CAP, High Polymer Chemistry or ceramic types. This control loop implementation provides fast transient response with no external compensation components. The TPS54325 dc/dc synchronous converter is designed to provide up to a 3-A output from an input control voltage source (VCC) of 4.5 V to 18 V, input power voltage source (VIN) of 2.0 V to 18 V and output voltage from 0.76 V to 5.5 V. Rated input voltage and output current range for the evaluation module are given in [Table 1-1](#).

Table 1-1. EVM Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54325EVM	V _{IN} = 5 V to 17 V	0 A to 3 A

1.2 Performance Specification Summary

A summary of the EVM performance specifications is provided in [Table 1-2](#). Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.05 V, unless otherwise noted. The VIN and VCC input voltage pins are connected on the EVM using a 0-Ω resistor (R9). The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 1-2. TPS54325EVM Performance Specifications Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range (V _{IN})		5	12	17	V
Output voltage			1.05		V
Operating frequency	V _{IN} = 12 V, I _{out1} = 1 A		700		kHz
Output current range		0		3	A
Over current limit	V _{IN} = 12 V		4.1		A
Output ripple voltage	V _{IN} = 12 V, I _{out1} = 3 A		9		mVp-p
Efficiency	V _{IN} = 12 V, V _{OUT} = 3.3 V, I _{OUT} = 1.2 A		91		%

1.3 Modifications

These evaluation modules are designed to provide access to the feature set of the TPS54325. Some modification can be made to these modules.

1.3.1 Output Voltage Set Point

The output voltage of the EVM is set using the voltage divider of R1 + R4 and R2. To change the output voltage of the EVMs, it is necessary to change the value of resistors R1 and R4 while leaving R2 fixed. Changing the value of R1 and R4 can change the output voltage above 0.765 V. The value of R1 and R4 for a specific output voltage basically can be calculated using [Equation 1](#).

$$V_O = 0.765 \cdot \left(1 + \frac{R1 + R4}{R2}\right) \quad (1)$$

[Table 1-3](#) lists the each R1 and R4 value for some common output voltages. C9 is used for faster load transient response and is not normally used. Note that the values given in [Table 1-3](#) are standard values, and not the exact value calculated using [Table 1-3](#).

Table 1-3. Output Voltages

Output Voltage (V)	R1(Ω)	R4(Ω)	R2(Ω)	C9(pF)	L1(H)
1.0	6.8 k	100	22 k		1.5 μ
1.05	8.2 k	220	22 k		1.5 μ
1.2	12 k	820	22 k		1.5 μ
1.8	27 k	3.0 k	22 k	10 - 22	2.2 μ
2.5	47 k	3.0 k	22 k	10 - 22	2.2 μ
3.3	68 k	4.7 k	22 k	10 - 22	2.2 μ
5	120 k	1.2 k	22 k	10 - 22	3.3 μ

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54325 EVM. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start up and switching frequency.

2.1 Test Setup

Connect test equipment and TPS54325EVM board as shown in Figure 2-1.

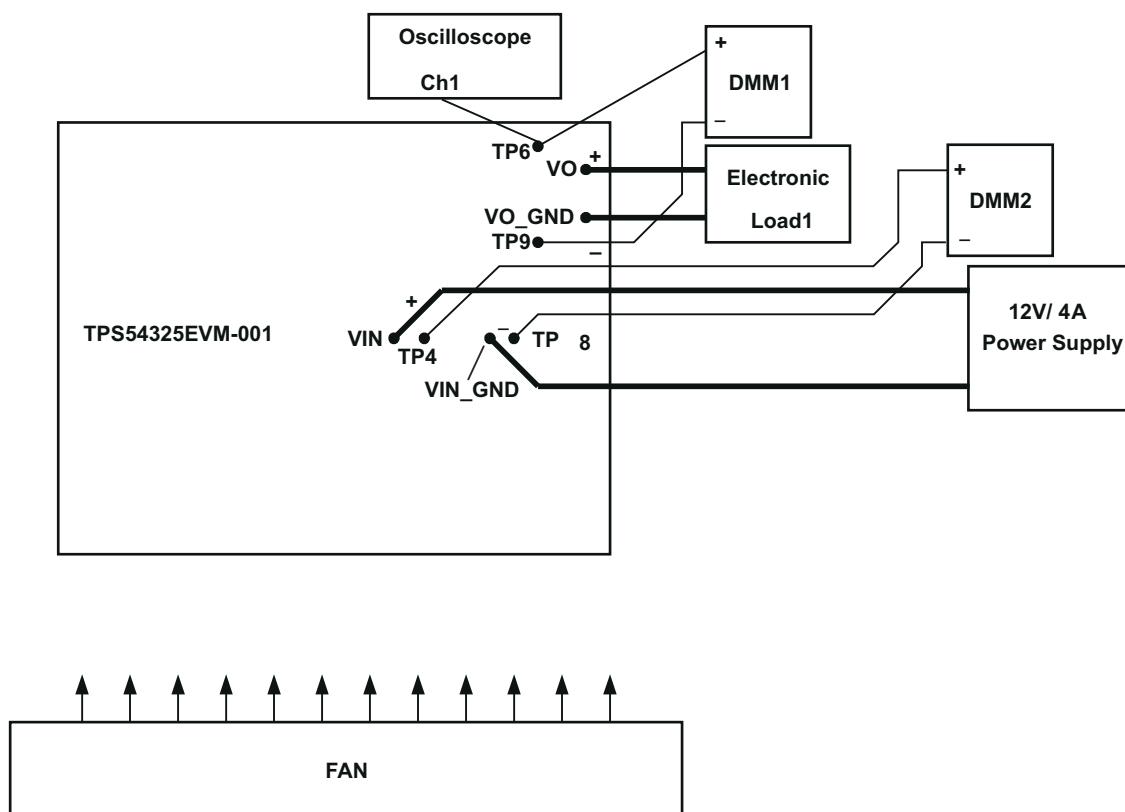


Figure 2-1. Equipment Setup for TPS54325EVM Board

2.2 Test Procedure

1. Make sure the switch SW1 (EN) is in the "OFF" position.
2. Apply the appropriate V_{IN} voltage to VIN and VIN_GND terminals.
3. Turn on SW1 (EN) to enable the EVM output voltage.

2.3 Efficiency

Figure 2-2 shows the efficiency for the TPS54325EVM at an ambient temperature of 25°C. The EVM was modified for operation at 3.3-, 2.5- and 1.8-V output using the R1 and R4 values in Table 1-3.

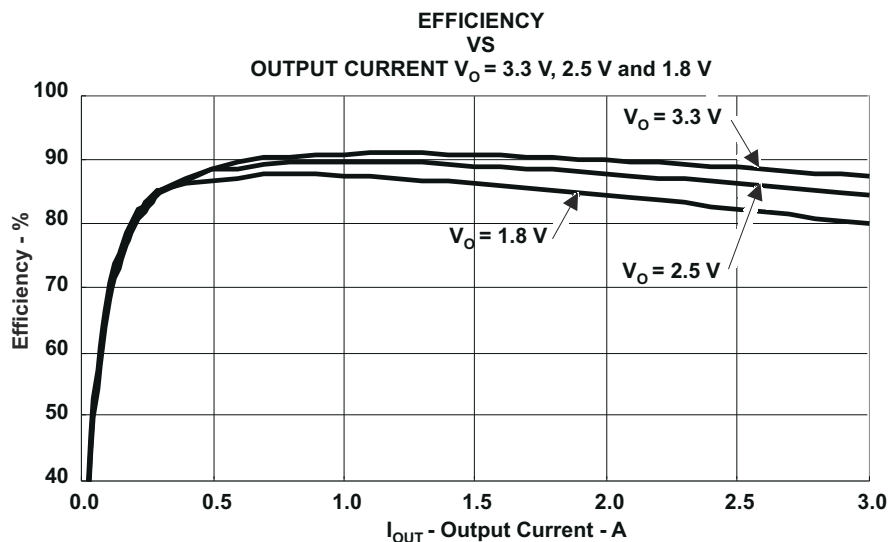


Figure 2-2. TPS54325EVM Efficiency

2.4 Load Regulation

The load regulation for the TPS54325EVM is shown Figure 2-3.

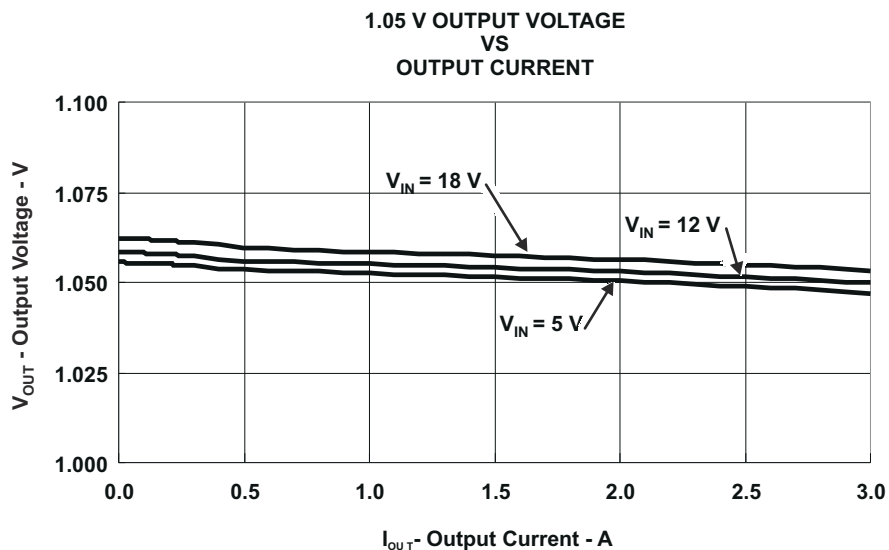


Figure 2-3. TPS54325EVM Load Regulation

2.5 Line Regulation

The line regulation for the TPS54325EVM is shown [Figure 2-4](#).

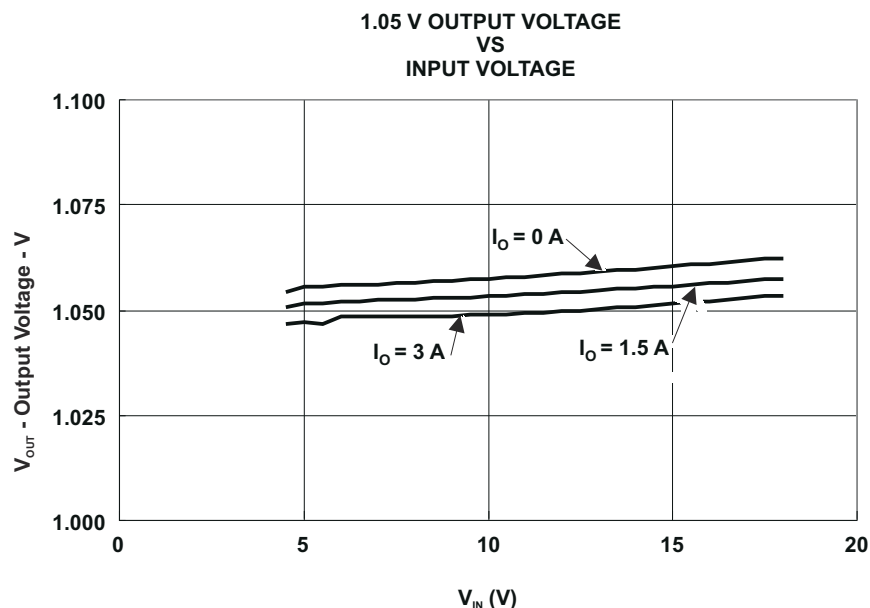


Figure 2-4. TPS54325EVM Line Regulation

2.6 Load Transient Response

The TPS54325EVM response to load transient is shown in [Figure 2-5](#). The current step is from 0 A to 3 A of maximum rated load. Total peak to peak voltage variation is as shown.

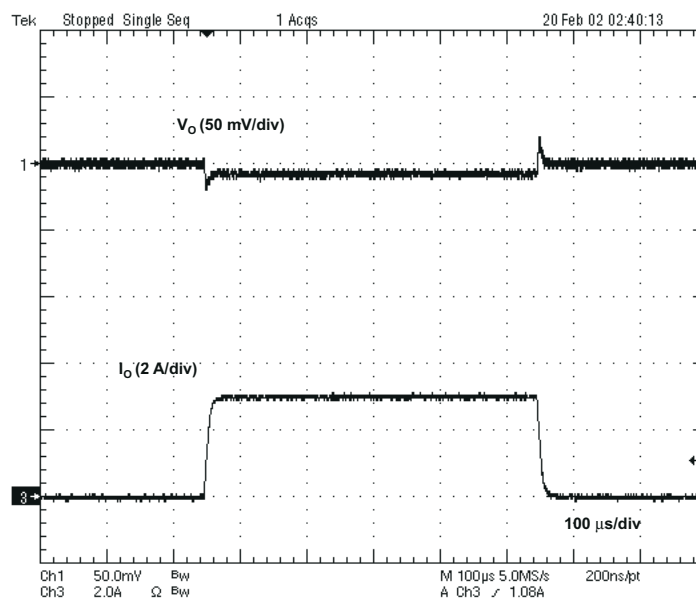


Figure 2-5. TPS54325EVM Load Transient Response

2.7 Output Voltage Ripple

The TPS54325EVM output voltage ripple is shown in Figure 2-6. The output current is the rated full load of 3 A.

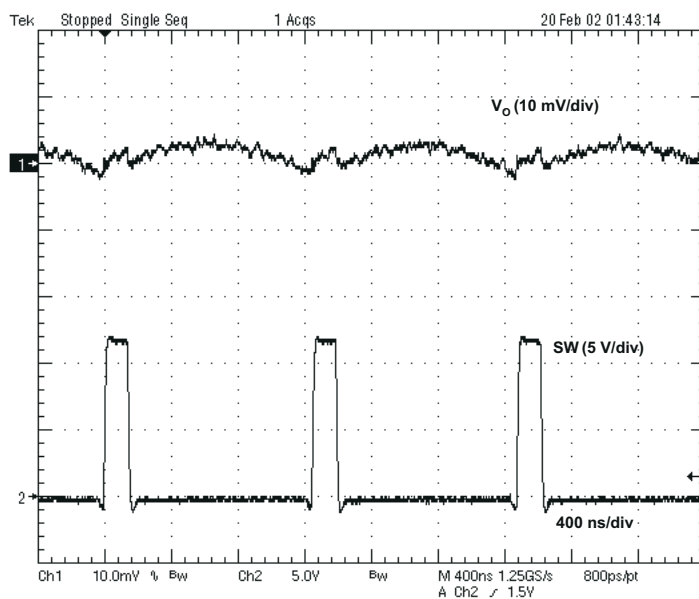


Figure 2-6. TPS54325EVM Output Voltage Ripple

2.8 Input Voltage Ripple

The TPS54325EVM input voltage ripple is shown in Figure 2-7. The output current is the rated full load of 3 A.

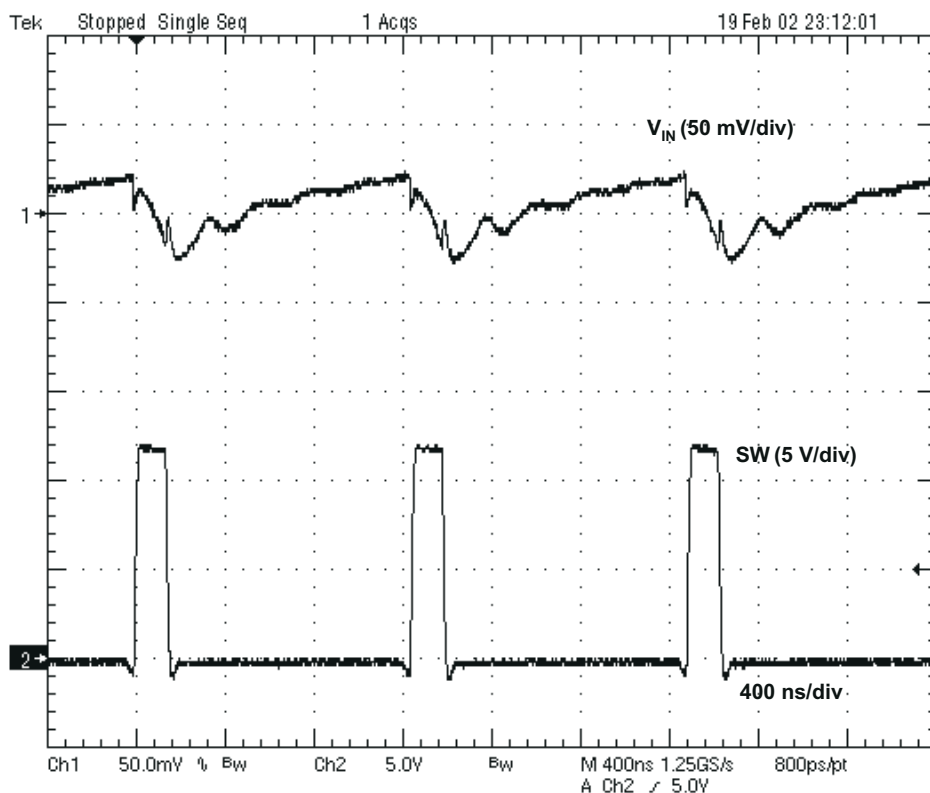


Figure 2-7. TPS54325EVM Input Voltage Ripple

2.9 Start Up

The TPS54325EVM start up waveform is shown in [Figure 2-8](#).

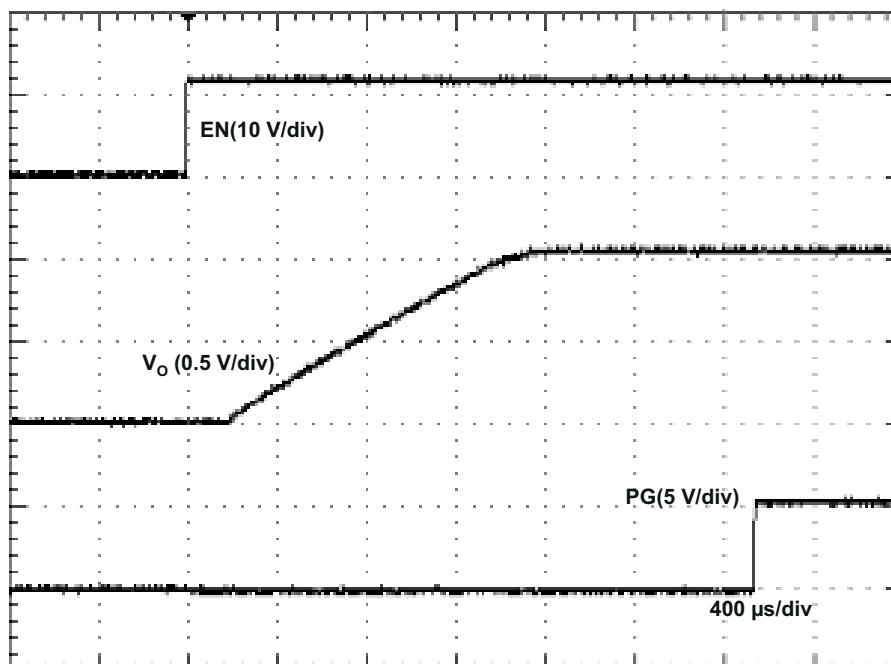


Figure 2-8. TPS54325EVM Start Up

2.10 Switching Frequency

The TPS54325EVM switching frequency is shown in [Figure 2-9](#).

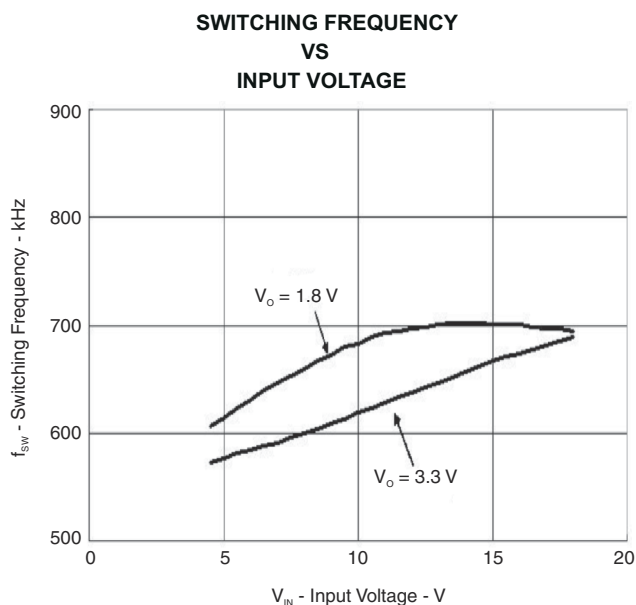


Figure 2-9. TPS54325EVM Switching Frequency

3 Board Layout

This section provides description of the TPS54325EVM, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54325EVM and is shown in [Figure 3-1](#) through [Figure 3-6](#). The top layer contains the main power traces for V_{IN} , V_{OUT} and the SW1 and SW2 nodes. Also on the top layer are connections for the pins of the TPS54325 and a large area filled with power ground (PGND) connected to pins 8 and 9 of the TPS54325. The first internal layer is a split ground plane containing a large power ground (PGND) area and a smaller signal ground (GND) area. The second internal layer contains an additional V_{IN} trace and a connection from switch SW1 to V_{CC} . The remainder of the second internal layer is power ground (PGND) area. The bottom layer contains the remainder of the circuit interconnect traces and the signal ground plane (GND) that is connected to pin 5 of the TPS54325 through a via near the pin. The signal ground and power ground are electrically common. They are connected together on the pcb at the pin 5 and the powerpad of the TPS54325. The bottom assembly layer is shown as looking from the back side of the printed circuit board.

The input decoupling capacitor and all parts are located as close to the IC as possible.

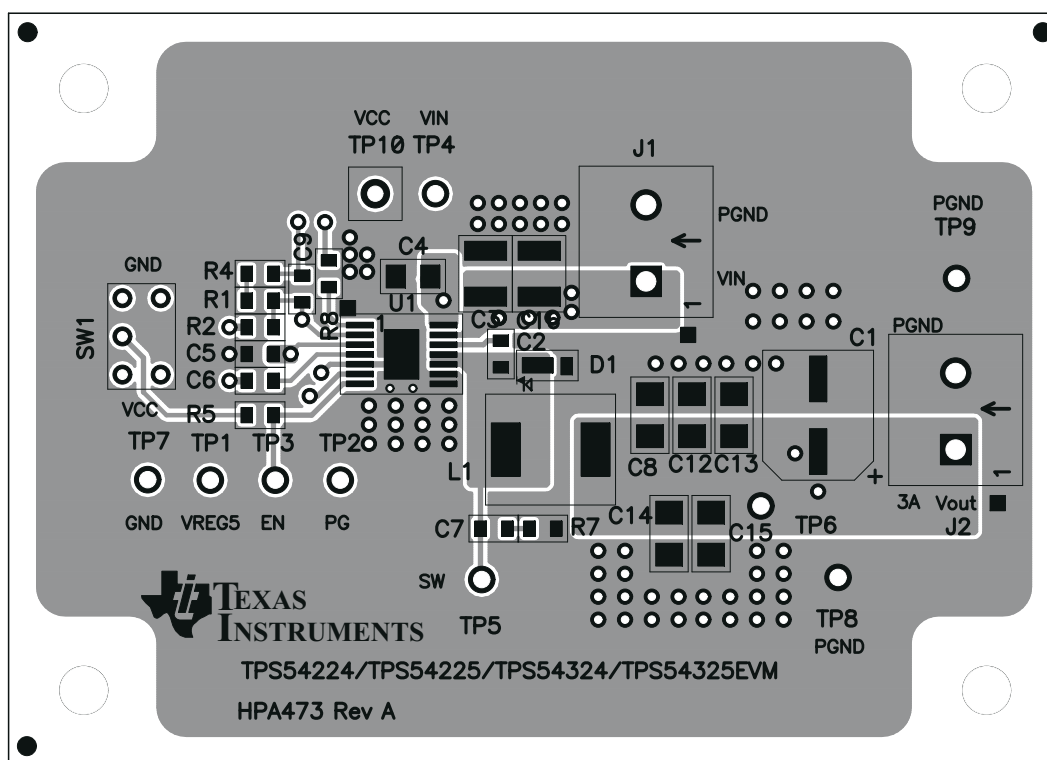


Figure 3-1. Top Assembly

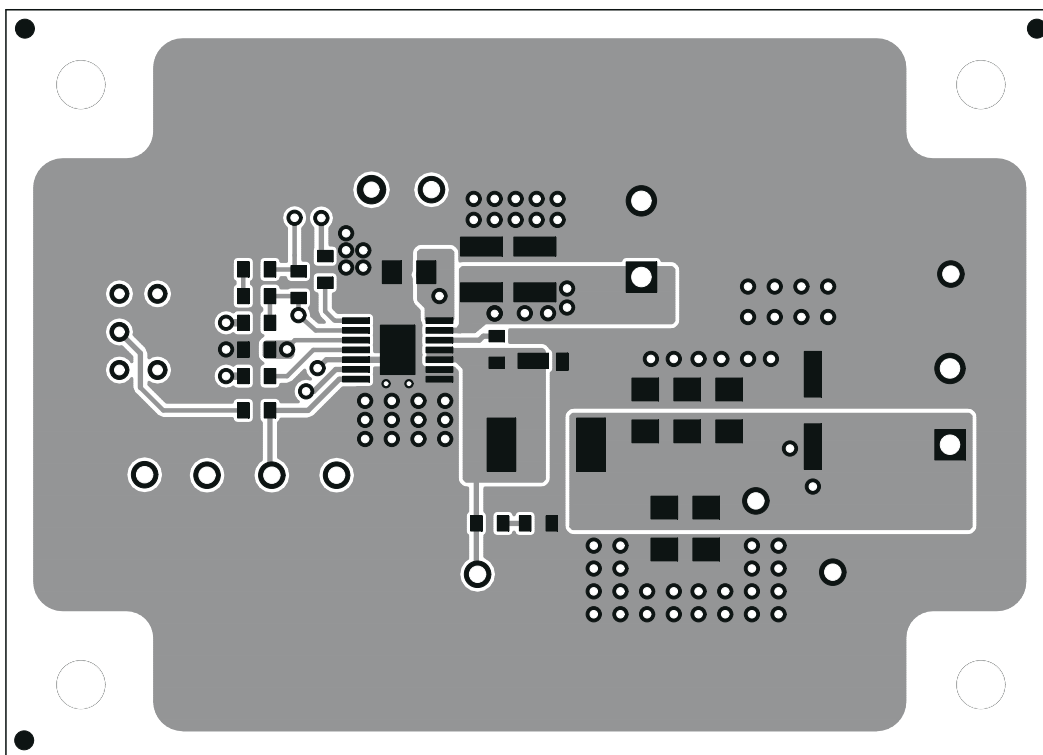


Figure 3-2. Top Layer

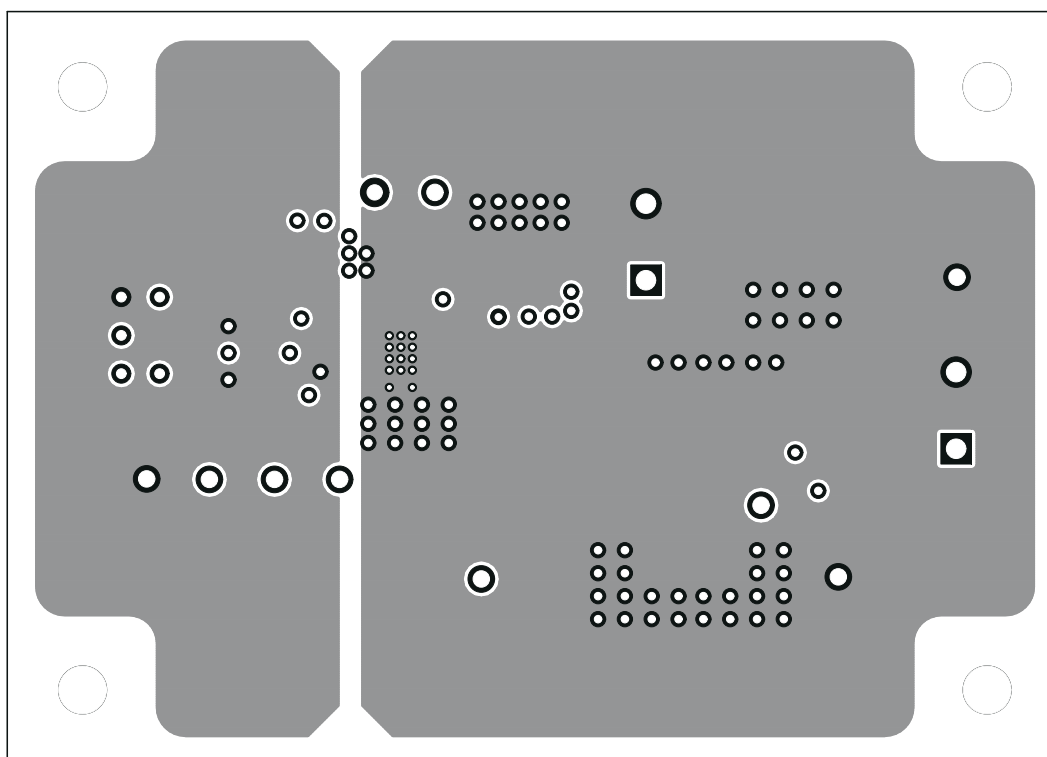


Figure 3-3. Internal Layer 1

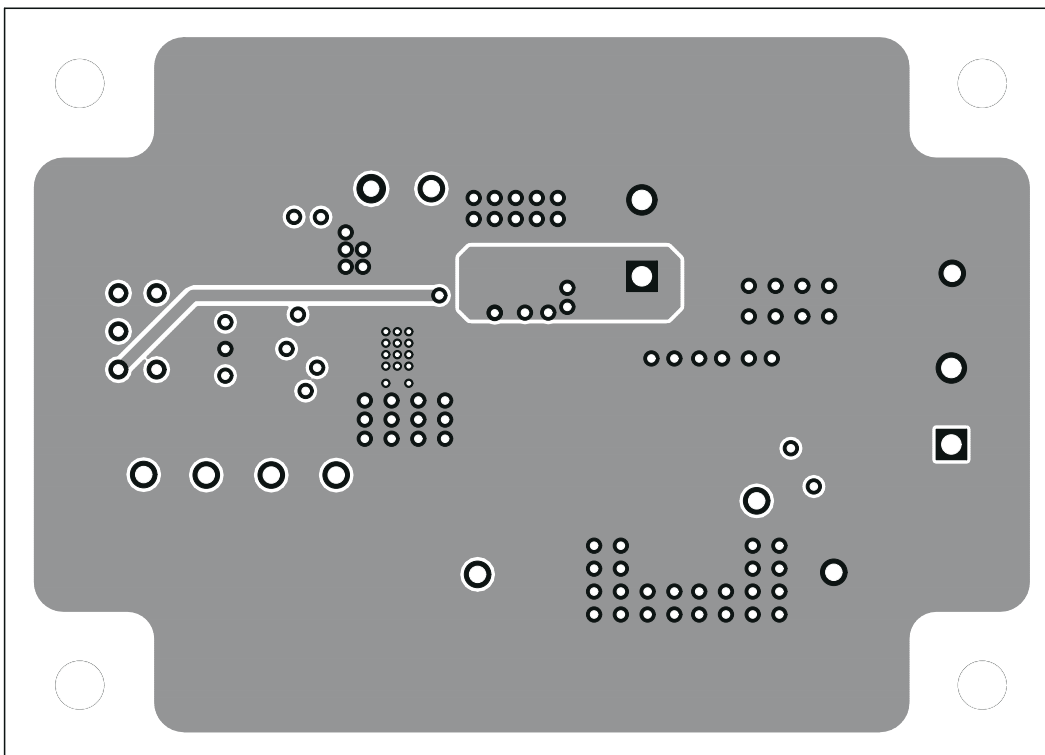


Figure 3-4. Internal Layer 2

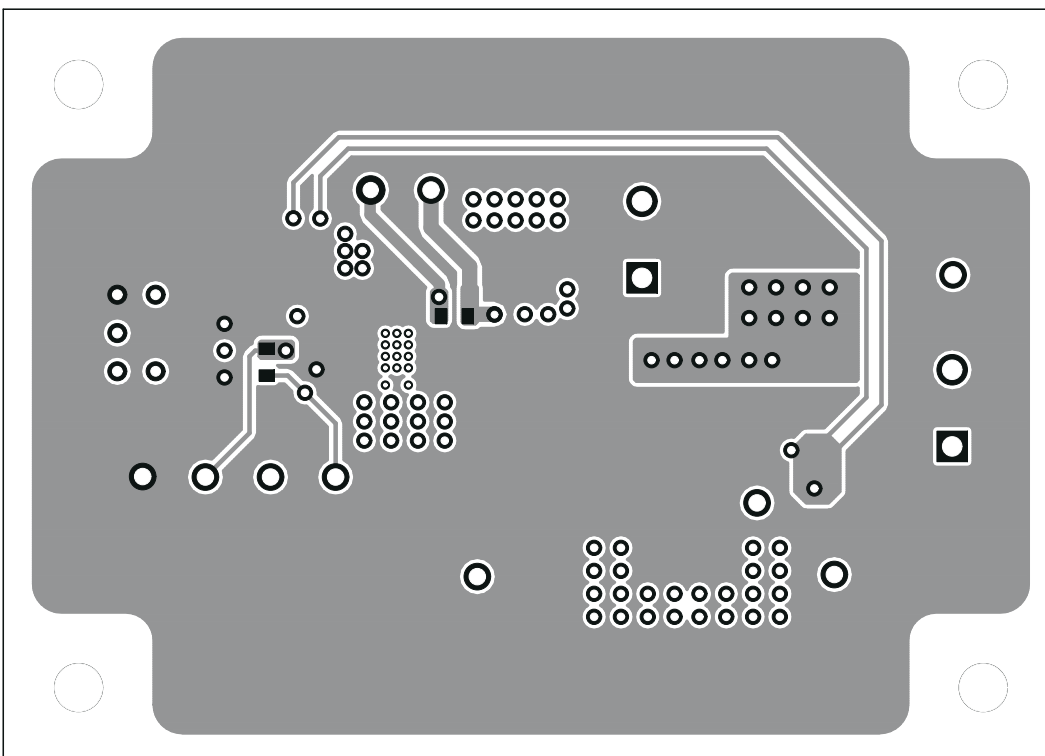


Figure 3-5. Bottom Layer

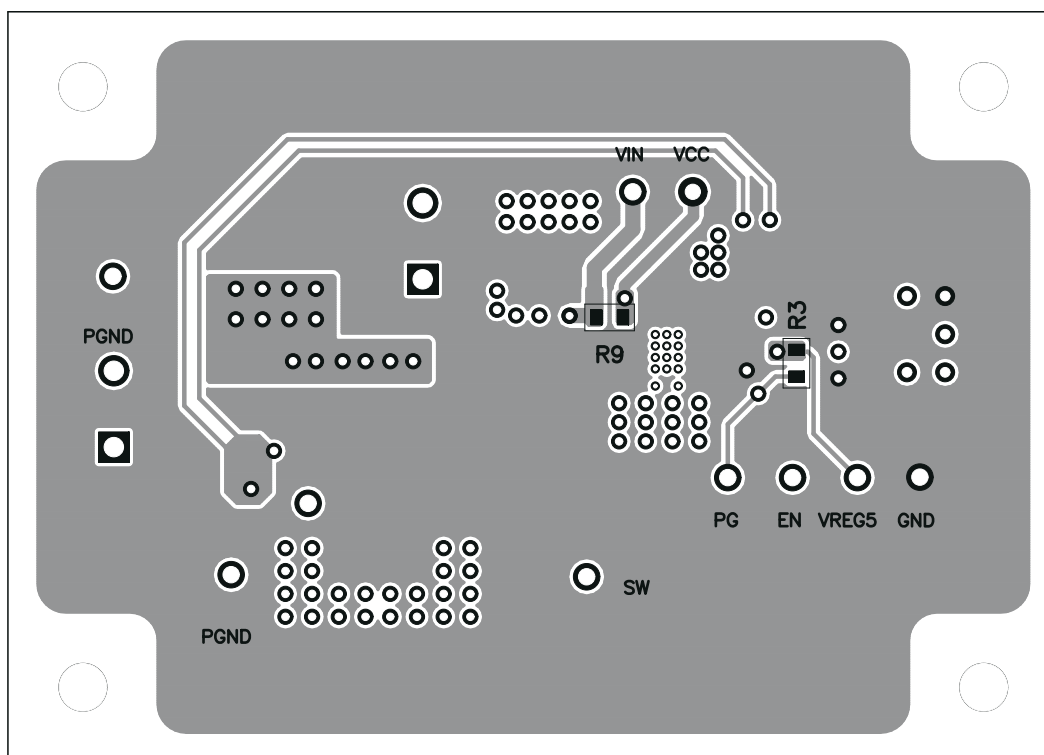


Figure 3-6. Bottom Assembly (as Viewed from Back Side)

4 Schematic and Bill of Materials

This section presents the TPS54325EVM schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54325EVM.

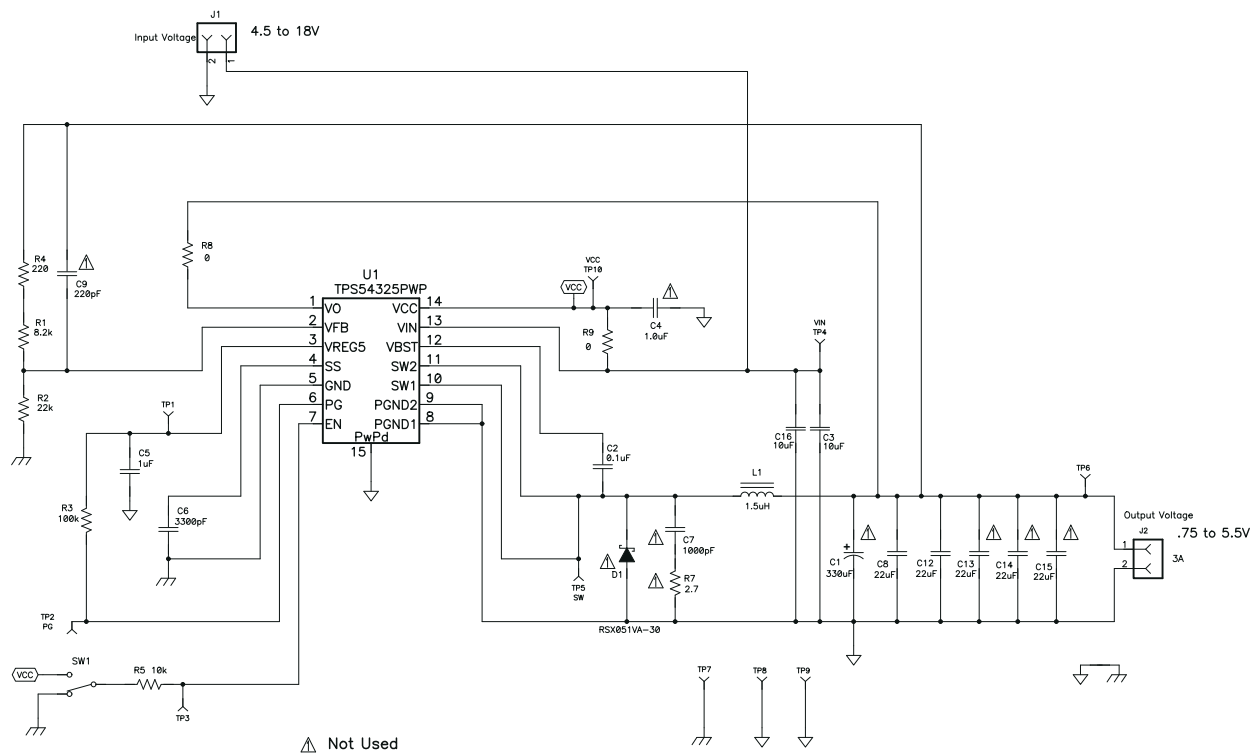


Figure 4-1. TPS54325EVM Schematic Diagram

4.2 Bill of Materials

Table 4-1. Bill of Materials

Reference Designator	QTY	Description	Size	Mfr	Part Number
C1	0	Capacitor, NPCAP, 330 μ F, 6.3-Vdc 14-m Ω , 20%	6.6 x 7.2 mm	NIPPON CHEMI- CON	APXE6R3ARA331 MF80G
C2	1	Capacitor, Ceramic, 0.1 μ F, 50 V, B, 10%	0603	TDK	C1608JB1H104K
C3, C16	2	Capacitor, Ceramic, 10 μ F, 25 V, X5R, 10%	1210	TDK	C3225X5R1E106 K
C4	0	Capacitor, Ceramic, 1 μ F, 25 V, X5R, 10%	0805	TDK	C2012X5R1E105 K
C5	1	Capacitor, Ceramic, 1 μ F, 16V, B, 10%	0603	TDK	C1608JB1C105K
C6	1	Capacitor, Ceramic, 3300 pF, 50 V, CH, 10%	0603	TDK	C1608CH1H332J
C7	0	Capacitor, Ceramic	0603	STD	STD
C8, C12	2	Capacitor, Ceramic, 22 μ F, 6.3 V, B, 20%	1206	TDK	C3216JB0J226M
C9	0	Capacitor, Ceramic, 220 pF, 50 V, CH, 10%	0603	TDK	C1608CH1H221J
C13, C14, C15	0	Capacitor, Ceramic, 22 μ F, 6.3 V, B, 20%	1206	TDK	C3216JB0J226M
D1	0	Diode, Schottky, 1 A, 30 V	SMA	-	-
J1, J2	2	Terminal Block, 2-pin, 15 A, 5.1mm	0.40 x 0.35 inch	Phoenix Contact	MKDSN1.5/2-5.08
L1	1	Inductor, 1.5 μ H, 10.0 A, 10.67 m Ω	6.5 x 7.1 mm	TDK	SPM6530T-1R5M
R1	1	Resistor, Chip, 8.2 k Ω , 1/16 W, 1%	0603	STD	STD
R2	1	Resistor, Chip, 22 k Ω , 1/16 W, 1%	0603	STD	STD
R3	1	Resistor, Chip, 100 k Ω , 1/16 W, 1%	0603	STD	STD
R4	1	Resistor, Chip, 220 Ω , 1/16 W, 1%	0603	STD	STD
R5	1	Resistor, Chip, 10 k Ω , 1/16 W, 1%	0603	STD	STD
R7	0	-	0603	STD	STD
R8, R9	2	Resistor, Chip, 0 Ω , 1/16 W, 1%	0603	STD	STD
SW1	1	Switch, ON-ON Mini Toggle	0.28 x 0.18 inch	NKK	633-G12AP
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9	Test Point, Yellow, Thru Hole	0.13 x 0.13 inch	MAC8SDK	LC-2-G
TP10	1	Test Point, White, Thru Hole	0.1 x 0.1 inch	Keystone	5000
U1	1	IC, 3-A Single Synchronous Converter with Integrated Hi Side and Low Side MOS FET	PWP14	TI	TPS54325PWP

5 References

Texas Instruments, [TPS54325 4.5-V to 18-V, 3-A Output Synchronous Step-Down SWIFT™ Controller Data Sheet](#)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2009) to Revision A (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.....	3

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