FULLY-INTEGRATED, 8-CHANNEL ANALOG FRONT-END FOR ULTRASOUND
0.89nV/√Hz, 12-Bit, 40MSPS, 101mW/Channel

Check for Samples: AFE5804

FEATURES

- **8-Channel Complete Analog Front-End:**
  - **LNA, VCA, PGA, LPF, and ADC**
- **Mode Control for Power/Noise Optimization:**
  - **Low Noise (Full-Channel):**
    0.89nV/√Hz (TGC Mode I)
    1.23nV/√Hz (TGC Mode II)
    1.03nV/√Hz (PW Mode)
  - **Ultra-Low Power:**
    101mW/Channel (TGC Mode II)
    65mW/Channel (CW Mode)
- **Low-Noise Pre-Amp (LNA):**
  - **0.75nV/√Hz**
  - **20dB Fixed Gain**
  - **280mV$_{PP}$ Linear Input Range**
- **Variable-Gain Amplifier:**
  - **Gain Control Range: 46dB**
- **PGA Gain Settings: 20dB, 25dB, 27dB, 30dB**
- **Low-Pass Filter:**
  - **Selectable BW: 12.5MHz, 17MHz**
  - **2nd-Order, Bessel**
- **Gain Error: ±0.5dB**
- **Channel Matching: ±0.25dB**
- **Clamping**
- **Fast Overload Recovery: Two Clock Cycles**
- **12-Bit Analog-to-Digital Converter:**
  - **10MSPS to 50MSPS**
  - **69dB SNR at 10MHz**
  - **Serial LVDS Interface**
- **Integrated CW Switch Matrix**
- **15mm × 9mm, 135-BGA Package:**
  - **Pb-Free (RoHS-Compliant) and Green**

APPLICATIONS

- **Medical Imaging, Ultrasound**
  - **Portable Systems**
  - **Battery-Powered Systems**

DESCRIPTION

The AFE5804 is a complete analog front-end device specifically designed for ultrasound systems that require low power and small size.

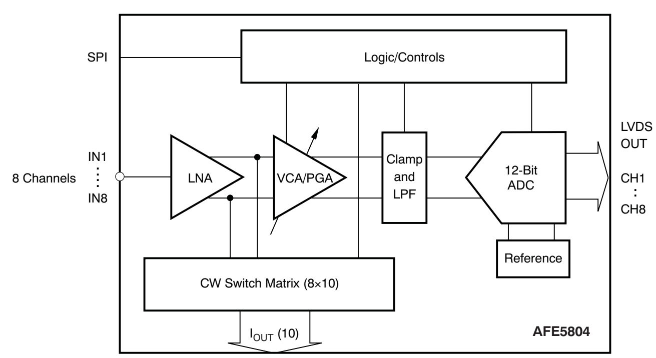
The AFE5804 consists of eight channels, including a low-noise amplifier (LNA), voltage-controlled attenuator (VCA), programmable gain amplifier (PGA), low-pass filter (LPF), and a 12-bit analog-to-digital converter (ADC) with low voltage differential signaling (LVDS) data outputs.

The LNA gain is set for 20dB gain and has excellent noise and signal handling capabilities, including fast overload recovery. VCA gain can vary over a 46dB range with a 0V to 1.2V control voltage common to all channels of the AFE5804.

The PGA can be programmed for gains of 20dB, 25dB, 27dB, and 30dB. The internal low-pass filter can also be programmed to 12.5MHz or 17MHz.

The LVDS outputs of the ADC reduce the number of interface lines to an ASIC or FPGA, thereby enabling the high system integration densities desired for portable systems. The ADC can either be operated with internal or external references. The ADC also features a signal-to-noise ratio (SNR) enhancement mode that can be useful at high gains.

The AFE5804 is available in a 15mm × 9mm, 135-ball BGA package that is Pb-free (RoHS-compliant) and green. It is specified for operation from 0°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1) (2)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY	ECO STATUS
AFE5804	μFBGA-135	ZCF	0°C to +85°C	AFE5804ZCFR	Tape and Reel, 1000	Pb-Free, Green
				AFE5804ZCFT	Tape and Reel, 250	
				AFE5804ZCF	Tray, 160	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1%of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		AFE5804	UNIT
Supply voltage range, AVDD1		–0.3 to +3.9	V
Supply voltage range, AVDD2		–0.3 to +3.9	V
Supply voltage range, AVDD_5V		–0.3 to +6	V
Supply voltage range, DVDD		–0.3 to +3.9	V
Supply voltage range, LVDD		–0.3 to +2.2	V
Voltage between AVSS1 and LVSS		–0.3 to +0.3	V
Voltage at analog inputs		–0.3 to minimum [3.6, (AVDD2 + 0.3)]	V
External voltage applied to REFT-pin		–0.3 to +3	V
External voltage applied to REFB-pin		–0.3 to +2	V
Voltage at digital inputs		–0.3 to minimum [3.9, (AVDD2 + 0.3)]	V
Peak solder temperature(2)		+260	°C
Maximum junction temperature, T_J		+125	°C
Storage temperature range		–55 to +150	°C
Operating temperature range		0 to +85	°C
ESD ratings	HBM	2000	V
	CDM	750	V
	MM	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to *absolute maximum conditions* for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Device complies with JSTD-020D.

ELECTRICAL CHARACTERISTICS

At AVDD_5V = 5.0V, AVDD1 = AVDD2 = DVDD = 3.3V, LVDD = 1.8V, TGC mode I, single-ended input into LNA, ac-coupled (1.0µF), V_{CNTL} = 1.0V, f_{IN} = 5MHz, Clock = 40MSPS, 50% duty cycle, LPF = 12.5MHz, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, and ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE5804			UNIT
			MIN	TYP	MAX	
PREAMPLIFIER (LNA)						
Gain	A	SE-input to differential output		20		dB
Input voltage (TGC, PW modes)	V_{IN}	Linear operation (HD2 ≤ 40dB)		280		mV_{PP}
(CW mode)		Linear operation		220		mV_{PP}
Maximum input voltage		Limited by internal diodes		600		mV_{PP}
Input voltage noise (TGC)	e_n (RTI)	R_S = 0Ω, f = 2MHz		0.75		nV/√Hz
Input current noise	I_n (RTI)	TGC mode I		3		pA/√Hz
		TGC mode II		1.7		pA/√Hz
Common-mode voltage, input	V_{CMI}	Internally generated		2.4		V
Bandwidth	BW	Small-signal, –3dB		55		MHz
Input resistance	R_{IN}	At 2.5MHz		8		kΩ
Input capacitance	C_{IN}	Includes internal ESD and clamping diodes		16		pF
FULL-SIGNAL CHANNEL (LNA + VCA + LPF + ADC)						
Input voltage noise (TGC mode I)	e_n	R_S = 0Ω, f = 2MHz, PGA = 30dB		0.89		nV/√Hz
Input voltage noise (TGC mode II)		R_S = 0Ω, f = 2MHz, PGA = 30dB		1.23		nV/√Hz
Input voltage noise (PW mode)		R_S = 0Ω, f = 2MHz, PGA = 30dB		1.03		nV/√Hz
Noise figure	NF	R_S = 200Ω, f = 2MHz		1.1		dB
Low-pass filter bandwidth	LPF	At –3dB, selectable through SPI		12.5, 17		MHz
Bandwidth tolerance				±10		%
High-pass filter	HPF	(First-order, due to internal ac-coupling)		200		kHz
Group delay variation		1MHz to 10MHz		±3		ns
Overload recovery		≤ 6dB overload to within 3%, V_{CNTL} = 0V to 1.2V		2		Clock Cycles
ACCURACY						
Gain (PGA)		Selectable through SPI		20, 25, 27, 30		dB
Total gain, max (1)		LNA + PGA gain, V_{CNTL} = 1.2V	47.5	49	50.5	dB
Gain range		V_{CNTL} = 0V to 1.2V		46		dB
		V_{CNTL} = 0.1V to 1.0V		40		dB
Gain error, absolute (2)		0V < V_{CNTL} < 0.1V		±0.5		dB
		0.1V < V_{CNTL} < 1.0V	–1.5	±0.5	+1.5	dB
		1.0V < V_{CNTL} < 1.2V		±0.5		dB
Gain matching		Channel-to-channel	–0.5	±0.25	+0.5	dB
Offset error		V_{CNTL} = 1.2V, PGA = 30dB	–39		+39	LSB
Offset error drift (tempco)				±5		ppm/°C
Clamp level		Level internally fixed before LPF		2.3		V_{PP}
GAIN CONTROL (VCA)						
Input voltage range	V_{CNTL}	Gain range = 46dB		0 to 1.2		V
Gain slope		V_{CNTL} = 0.1V to 1.0V		44.4		dB/V
Input resistance				25		kΩ
Response time		V_{CNTL} = 0V to 1.2V step; to 90% signal		0.5		µs

(1) Excludes digital gain within ADC.
(2) Excludes error of internal reference.

ELECTRICAL CHARACTERISTICS (continued)

At AVDD_5V = 5.0V, AVDD1 = AVDD2 = DVDD = 3.3V, LVDD = 1.8V, TGC mode I, single-ended input into LNA, ac-coupled (1.0µF), V_{CNTL} = 1.0V, f_{IN} = 5MHz, Clock = 40MSPS, 50% duty cycle, LPF = 12.5MHz, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, and ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE5804 MIN	AFE5804 TYP	AFE5804 MAX	UNIT
DYNAMIC PERFORMANCE						
Signal-to-noise ratio	SNR	f_{IN} = 2MHz; –1dBFS (V_{CNTL} = 1.0V, PGA = 30dB)		59.7		dBFS
		f_{IN} = 5MHz; –1dBFS		59.5		dBFS
		f_{IN} = 10MHz; –1dBFS		59.1		dBFS
Second-harmonic distortion	HD2	f_{IN} = 5MHz; –1dBFS (V_{CNTL} = 0.35V, PGA = 30dB)		–45		dBFS
		f_{IN} = 5MHz; –1dBFS (V_{CNTL} = 1V, PGA = 30dB)	–50	–70		dBFS
		f_{IN} = 5MHz; –6dBFS (V_{CNTL} = 1V, PGA = 20dB)	–61	–70		dBFS
Third-harmonic distortion	HD3	f_{IN} = 5MHz; –1dBFS (V_{CNTL} = 0.35V, PGA = 30dB)		–43		dBFS
		f_{IN} = 5MHz; –1dBFS (V_{CNTL} = 1V, PGA = 30dB)	–43	–50		dBFS
		f_{IN} = 5MHz; –6dBFS (V_{CNTL} = 1V, PGA = 20dB)	–61	–70		dBFS
Intermodulation distortion	IMD3	f_1 = 4.99MHz at –6dBFS, f_2 = 5.01MHz at –32dBFS		58		dBc
Crosstalk		f_{IN} ≤ 5MHz, V_{CNTL} = 0.6V, –6dBFS		–67		dBc
CW—SIGNAL CHANNELS						
Input voltage noise (CW)	e_n	R_S = 0Ω, f = 2MHz		1.1		nV/√Hz
Output noise correlation factor		Summing of eight channels		0.6		%
Output transconductance	I_{OUT}/V_{IN}	At V_{IN} = 100mV_{PP}		13.8		mA/V
		At V_{IN} = 270mV_{PP}		12.2		mA/V
Dynamic CW output current, max	I_{OUTAC}			2.9		mA_{PP}
Static CW output current (sink)	I_{OUTDC}			0.9		mA
Output common-mode voltage(3)	VCM			2.5		V
Output impedance				50		kΩ
Output capacitance				10		pF
INTERNAL REFERENCE VOLTAGES (ADC)						
Reference top	VREFT			0.5		V
Reference bottom	VREFB			2.5		V
VREFT – VREFB			1.95	2	2.05	V
Common-mode voltage (internal)	V_{CM}		1.425	1.5	1.575	V
V_{CM} output current				±2		mA

(3) CW outputs require an externally applied bias voltage of +2.5V.

ELECTRICAL CHARACTERISTICS (continued)

At AVDD_5V = 5.0V, AVDD1 = AVDD2 = DVDD = 3.3V, LVDD = 1.8V, TGC mode I, single-ended input into LNA, ac-coupled (1.0µF), V_{CNTL} = 1.0V, f_{IN} = 5MHz, Clock = 40MSPS, 50% duty cycle, LPF = 12.5MHz, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, and ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE5804 MIN	AFE5804 TYP	AFE5804 MAX	UNIT
EXTERNAL REFERENCE VOLTAGES (ADC)						
Reference top	VREFT		2.4	2.5	2.6	V
Reference bottom	VREFB		0.4	0.5	0.6	V
VREFT – VREFB			1.9		2.1	V
Switching current(4)				2.5		mA
POWER SUPPLY						
SUPPLY VOLTAGES		At 40MSPS				
AVDD1, AVDD2, DVDD		Operating	3.15	3.3	3.47	V
AVDD_5V		Operating	4.75	5	5.25	V
LVDD			1.7	1.8	1.9	V
SUPPLY CURRENTS						
IAVDD1 (ADC)				99	110	mA
IAVDD2 (VCA)		TGC mode I		123	136	mA
		CW mode		63	75	mA
IAVDD_5V (VCA)		TGC mode I		7	10	mA
		CW mode		54	61	mA
IDVDD (VCA)				1.5	3.0	mA
ILVDD (ADC)				68	80	mA
Power dissipation, total(5)		All channels, TGC mode I, no signal		896	985	mW
		All channels, TGC mode II, no signal		808	898	mW
		All channels, PW mode , no signal		840	925	mW
		All channels, CW mode, no signal(6)		525	575	mW
		No clock applied, no signal		528		mW
POWER-DOWN MODES						
Power-down dissipation, total		Complete power-down mode		52	68	mW
Power-down response time				1.0		µs
Power-up response time		PD to valid output (90% level)		50		µs
Power-down dissipation(7)		Partial power-down mode		95		mW
THERMAL CHARACTERISTICS						
Temperature range			0		85	°C
Thermal resistance, T_{JA}				32		°C/W
Thermal resistance, T_{JC}				4.2		°C/W

(4) Current drawn by the eight ADC channels from the external reference voltages; sourcing for VREFT, sinking for VREFB.
(5) Programmable power affects on the front-end; ADC power consumption remains constant at about 57mW/channel for 40MSPS.
(6) ADC powered-down during CW mode.
(7) At VCA_PD pin pulled high; see also Power-Down Timing diagram.

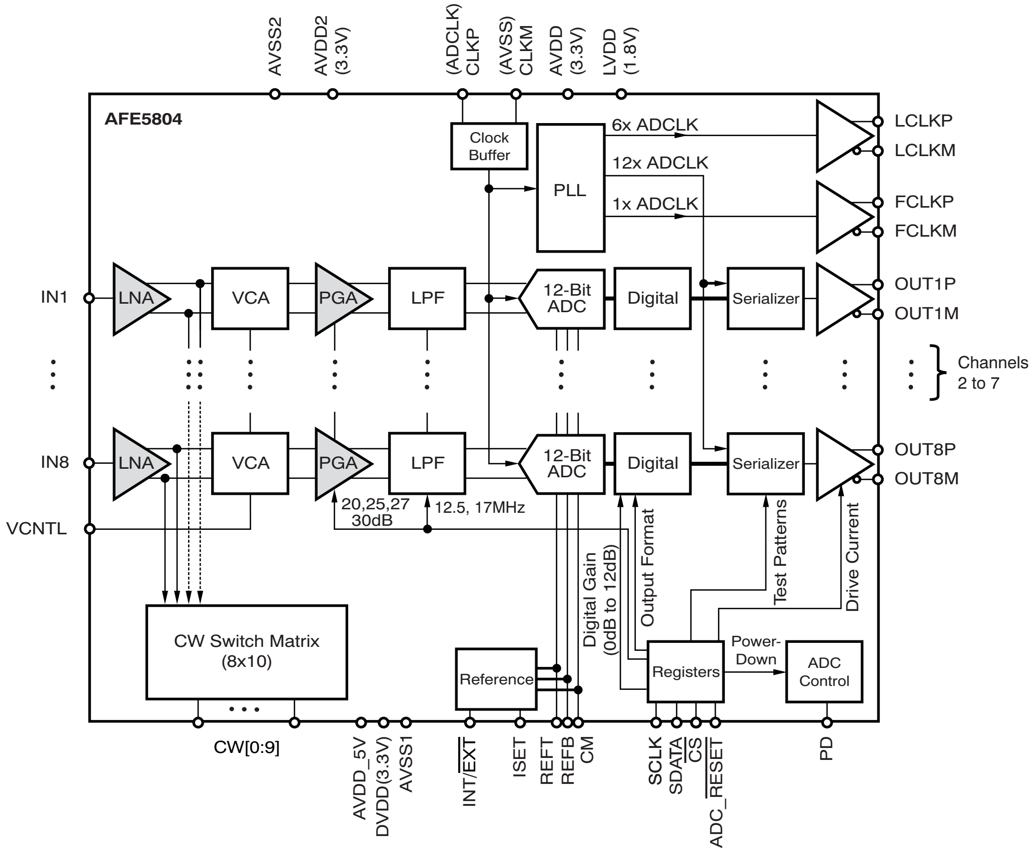
DIGITAL CHARACTERISTICS

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. At C_{LOAD} = 5pF (1), I_{OUT} = 3.5mA (2), R_{LOAD} = 100Ω (2), and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS	AFE5804 MIN	AFE5804 TYP	AFE5804 MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		1.4		3.3	V
Low-level input voltage		0		0.3	V
High-level input current			10		μA
Low-level input current (3)			–10		μA
Input capacitance			3		pF
LVDS OUTPUTS					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$			350		mV
V_{OS} output offset voltage (2)	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF
FCLKP and FCLKM		10	1x (clock rate)	50	MHz
LCLKP and LCLKM		60	6x (clock rate)	300	MHz
CLOCK					
Clock input rate		10		50	MSPS
Clock duty cycle			50		%
Clock input amplitude, differential (VCLKP – VCLKM)	Sine-wave, ac-coupled		3		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
Clock input amplitude, single-ended (VCLKP)					
High-level input voltage, V_{IH}	CMOS	2.2			V
Low-level input voltage, V_{IL}	CMOS			0.6	V

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(2) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
(3) Except pin J3 (INT/$\overline{EXT}$), which has an internal pull-up resistor (52kΩ) to 3.3V.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

ZCF PACKAGE
135-BGA
BOTTOM VIEW

Rows	1	2	3	4	5	6	7	8	9
R	OUT4M	OUT3M	OUT2M	OUT1M	LVSS	OUT5M	OUT6M	OUT7M	OUT8M
P	OUT4P	OUT3P	OUT2P	OUT1P	LVDD	OUT5P	OUT6P	OUT7P	OUT8P
N	LCLKP	LCLKM	LVSS	LVSS	LVSS	LVDD	LVDD	FCLKM	FCLKP
M	DNC	DNC	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	DNC	DNC
L	CLKP	AVDD1	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	AVDD1	EN_SM
K	CLKM	DNC	AVDD1	DNC	AVDD1	AVDD1	AVDD1	CM	ISET
J	AVSS1	AVDD1	INT/$\overline{\text{EXT}}$	AVSS2	AVSS2	AVSS2	AVDD1	REFT	REFB
H	ADS_PD	DNC	DNC	VCA_CS	RST	SCLK	$\overline{\text{CS}}$	SDATA	ADS_$\overline{\text{RESET}}$
G	CW5	AVDD2	VCM	AVSS2	AVSS2	AVSS2	VREFL	AVDD2	CW4
F	CW6	VB1	VB5	AVSS2	AVSS2	AVSS2	VREFH	VB6	CW3
E	CW7	AVDD_5V	VB3	AVSS2	AVSS2	AVSS2	VB4	AVDD_5V	CW2
D	CW8	VCNTL	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	VB2	CW1
C	CW9	AVDD2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	AVDD2	CW0
B	VBL1	VBL2	VBL3	VBL4	DNC	VBL8	VBL7	VBL6	VBL5
A	IN1	IN2	IN3	IN4	VCA_PD	IN8	IN7	IN6	IN5

Columns

ZCF PACKAGE
135-BGA
CONFIGURATION MAP (TOP VIEW)

	9	8	7	6	5	4	3	2	1
R	OUT8M	OUT7M	OUT6M	OUT5M	LVSS	OUT1M	OUT2M	OUT3M	OUT4M
P	OUT8P	OUT7P	OUT6P	OUT5P	LVDD	OUT1P	OUT2P	OUT3P	OUT4P
N	FCLKP	FCLKM	LVDD	LVDD	LVSS	LVSS	LVSS	LCLKM	LCLKP
M	DNC	DNC	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	DNC	DNC
L	EN_SM	AVDD1	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	AVDD1	CLKP
K	ISET	CM	AVDD1	AVDD1	AVDD1	DNC	AVDD1	DNC	CLKM
J	REFB	REFT	AVDD1	AVSS2	AVSS2	AVSS2	INT/$\overline{\text{EXT}}$	AVDD1	AVSS1
H	ADS_$\overline{\text{RESET}}$	SDATA	$\overline{\text{CS}}$	SCLK	RST	VCA_$\overline{\text{CS}}$	DNC	DNC	ADS_PD
G	CW4	AVDD2	VREFL	AVSS2	AVSS2	AVSS2	VCM	AVDD2	CW5
F	CW3	VB6	VREFH	AVSS2	AVSS2	AVSS2	VB5	VB1	CW6
E	CW2	AVDD_5V	VB4	AVSS2	AVSS2	AVSS2	VB3	AVDD_5V	CW7
D	CW1	VB2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	VCNTL	CW8
C	CW0	AVDD2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	AVDD2	CW9
B	VBL5	VBL6	VBL7	VBL8	DNC	VBL4	VBL3	VBL2	VBL1
A	IN5	IN6	IN7	IN8	VCA_PD	IN4	IN3	IN2	IN1

Legend:

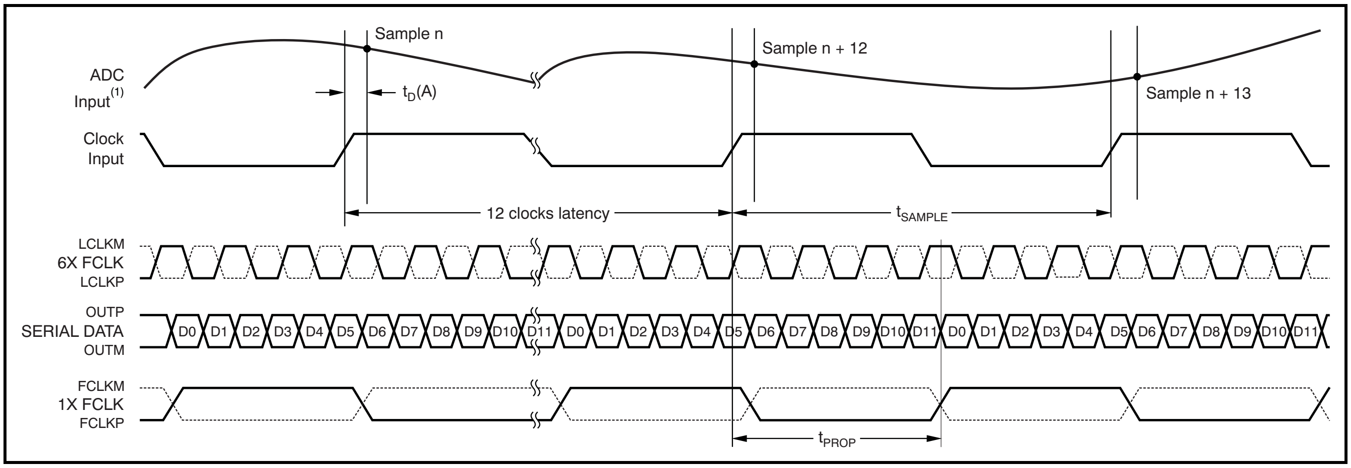
AVDD1	+3.3V; Analog
AVDD2	+3.3V; Analog
DVDD	+3.3V; Analog
LVDD	+1.8V; Digital
AVDD_5V	+5V; Analog
AVSS1	Analog Ground
AVSS2	Analog Ground
LVSS	Digital Ground

Table 1. TERMINAL FUNCTIONS

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
H7	$\overline{CS}$	Input	Chip select for serial interface; active low
H1	ADS_PD	Input	Power-down pin for ADS; active high
H9	ADS_$\overline{RESET}$	Input	RESET input for ADS; active low
H6	SCLK	Input	Serial clock input for serial interface
H8	SDATA	Input	Serial data input for serial interface
J2, L2, K7, J7, K3, L8, K5, K6	AVDD1	POWER	3.3V analog supply for ADS
L3, M3, L4, M4, L5, M5, L6, M6, L7, M7, J1	AVSS1	GND	Analog ground for ADS
P5, N6, N7	LVDD	POWER	1.8V digital supply for ADS
N3, N4, N5, R5	LVSS	GND	Digital ground for ADS
C5, D5	DVDD	POWER	3.3V digital supply for the VCA; connect to the 3.3V analog supply (AVDD2).
C2, C8, G2, G8	AVDD2	POWER	3.3V analog supply for VCA
E2, E8	AVDD_5V	POWER	5V supply for VCA
C3, D3, C4, D4, E4, F4, G4, E5, F5, G5, C6, D6, E6, F6, G6, C7, D7, J4, J5, J6	AVSS2	GND	Analog ground for VCA
K1	CLKM	Input	Negative clock input for ADS (connect to *Ground* in single-ended clock mode)
L1	CLKP	Input	Positive clock input for ADS
K8	CM	Input/Output	1.5V common-mode I/O for ADS. Becomes input pin in one of the external reference modes.
C9	CW0	Output	CW output 0
D9	CW1	Output	CW output 1
E9	CW2	Output	CW output 2
F9	CW3	Output	CW output 3
G9	CW4	Output	CW output 4
G1	CW5	Output	CW output 5
F1	CW6	Output	CW output 6
E1	CW7	Output	CW output 7
D1	CW8	Output	CW output 8
C1	CW9	Output	CW output 9
L9	EN_SM	Input	Enables access to the VCA register. Active high. Connect permanently to 3.3V (AVDD1).
N8	FCLKM	Output	LVDS frame clock (negative output)
N9	FCLKP	Output	LVDS frame clock (positive output)
A1	IN1	Input	LNA input Channel 1
A2	IN2	Input	LNA input Channel 2
A3	IN3	Input	LNA input Channel 3
A4	IN4	Input	LNA input Channel 4
A9	IN5	Input	LNA input Channel 5
A8	IN6	Input	LNA input Channel 6
A7	IN7	Input	LNA input Channel 7
A6	IN8	Input	LNA input Channel 8
J3	INT/$\overline{EXT}$	Input	Internal/ external reference mode select for ADS; internal = high
K9	ISET	Input	Current bias pin for ADS. Requires 56kΩ to ground.
N2	LCLKM	Output	LVDS bit clock (6x); negative output
N1	LCLKP	Output	LVDS bit clock (6x); positive output
R4	OUT1M	Output	LVDS data output (negative), Channel 1
P4	OUT1P	Output	LVDS data output (positive), Channel 1
R3	OUT2M	Output	LVDS data output (negative), Channel 2
P3	OUT2P	Output	LVDS data output (positive), Channel 2
R2	OUT3M	Output	LVDS data output (negative), Channel 3
P2	OUT3P	Output	LVDS data output (positive), Channel 3

Table 1. TERMINAL FUNCTIONS (continued)

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
R1	OUT4M	Output	LVDS data output (negative), Channel 4
P1	OUT4P	Output	LVDS data output (positive), Channel 4
R6	OUT5M	Output	LVDS data output (negative), Channel 5
P6	OUT5P	Output	LVDS data output (positive), Channel 5
R7	OUT6M	Output	LVDS data output (negative), Channel 6
P7	OUT6P	Output	LVDS data output (positive), Channel 6
R8	OUT7M	Output	LVDS data output (negative), Channel 7
P8	OUT7P	Output	LVDS data output (positive), Channel 7
R9	OUT8M	Output	LVDS data output (negative), Channel 8
P9	OUT8P	Output	LVDS data output (positive), Channel 8
J9	REFB	Input/Output	0.5V Negative reference of ADS. Decoupling to ground. Becomes input in external ref mode.
J8	REFT	Input/Output	2.5V Positive reference of ADS. Decoupling to ground. Becomes input in external ref mode.
H5	RST	Input	RESET input for VCA. Connect to the VCA_$\overline{\text{CS}}$ pin (H4).
H4	VCA_$\overline{\text{CS}}$	Output	Connect to RST–pin (H5)
F2	VB1	Output	Internal bias voltage. Bypass to ground with 2.2µF.
D8	VB2	Output	Internal bias voltage. Bypass to ground with 0.1µF.
E3	VB3	Output	Internal bias voltage. Bypass to ground with 0.1µF.
E7	VB4	Output	Internal bias voltage. Bypass to ground with 0.1µF
F3	VB5	Output	Internal bias voltage. Bypass to ground with 0.1µF.
F8	VB6	Output	Internal bias voltage. Bypass to ground with 0.1µF.
B1	VBL1	Input	Complementary LNA input Channel 1; bypass to ground with 0.1µF.
B2	VBL2	Input	Complementary LNA input Channel 2; bypass to ground with 0.1µF.
B3	VBL3	Input	Complementary LNA input Channel 3; bypass to ground with 0.1µF.
B4	VBL4	Input	Complementary LNA input Channel 4; bypass to ground with 0.1µF.
B9	VBL5	Input	Complementary LNA input Channel 5; bypass to ground with 0.1µF.
B8	VBL6	Input	Complementary LNA input Channel 6; bypass to ground with 0.1µF.
B7	VBL7	Input	Complementary LNA input Channel 7; bypass to ground with 0.1µF.
B6	VBL8	Input	Complementary LNA input Channel 8; bypass to ground with 0.1µF.
A5	VCA_PD	Input	Power-down pin for VCA; low = normal mode, high = power-down mode.
G3	VCM	Output	VCA reference voltage. Bypass to ground with 0.1µF.
D2	VCNTL	Input	VCA control voltage input
F7	VREFH	Output	Clamp reference voltage (2.7V). Bypass to ground with 0.1µF.
G7	VREFL	Output	Clamp reference voltage (2.0V). Bypass to ground with 0.1µF.
B5, H2, H3, K2, K4, M1, M2, M8, M9	DNC		Do not connect



(1) Referenced to ADC Input (internal node) for illustration purposes only.

Figure 1. LVDS Timing Diagram

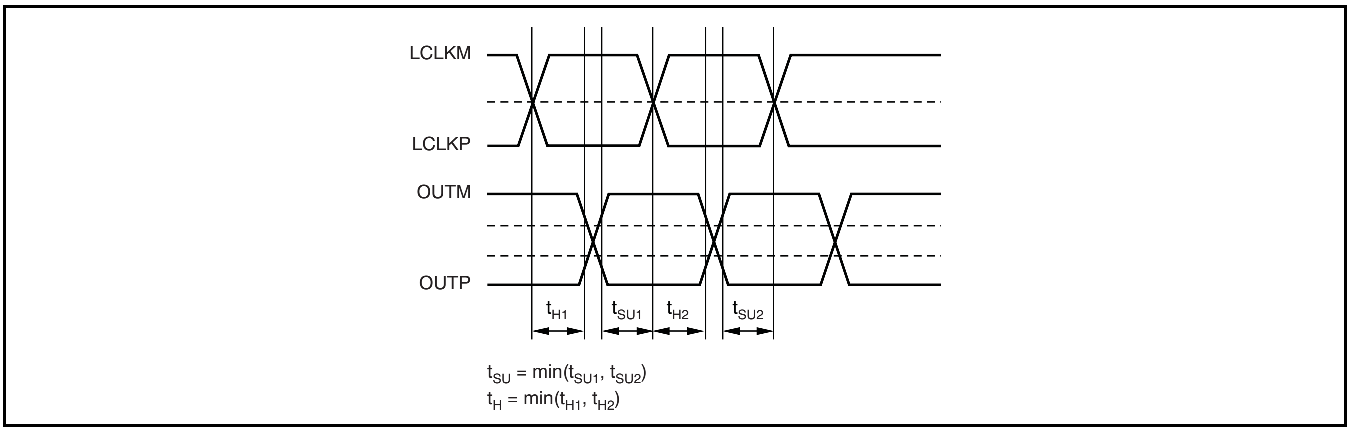


Figure 2. Definition of Setup and Hold Times

TIMING CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	AFE5804 MIN	AFE5804 TYP	AFE5804 MAX	UNIT
$t_{D(A)}$	ADC aperture delay		1.5		4.5	ns
	Aperture delay variation	Channel-to-channel within the same device (3σ)		±20		ps
t_J	Aperture jitter			400		f_S, rms
t_{WAKE}	Wake-up time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		50		µs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		2		µs
		Time to valid data after stopping and restarting the input clock		40		µs
	Data latency			12		Clock cycles

(1) Timing parameters are ensured by design and characterization; not production tested.

LVDS OUTPUT TIMING CHARACTERISTICS(1) (2)

Typical values are at +25°C, minimum and maximum values over specified temperature range of T_{MIN} = 0°C to T_{MAX} = +85°C, sampling frequency = as specified, C_{LOAD} = 5pF(3), I_{OUT} = 3.5mA, R_{LOAD} = 100Ω(4), and no internal termination, unless otherwise noted.

PARAMETER		TEST CONDITIONS(5)	AFE5804 40MSPS MIN	40MSPS TYP	40MSPS MAX	50MSPS MIN	50MSPS TYP	50MSPS MAX	UNIT
t_{SU}	Data setup time(6)	Data valid(7) to zero-crossing of LCLKP	0.67			0.47			ns
t_H	Data hold time(6)	Zero-crossing of LCLKP to data becoming invalid(7)	0.85			0.65			ns
t_{PROP}	Clock propagation delay	ADC input clock rising edge cross-over to output clock (FCLKP) rising edge cross-over	10	14	16.6	10	12.5	14.1	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLKP – LCLKM)	45.5	50	53	45	50	53.5	
	Bit clock cycle-to-cycle jitter			250			250		ps, pp
	Frame clock cycle-to-cycle jitter			150			150		ps, pp
t_{RISE}, t_{FALL}	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	ns

(1) All characteristics are at the maximum rated speed for each speed grade.
(2) Timing parameters are ensured by design and characterization; not production tested.
(3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(4) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
(6) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
(7) Data valid refers to a logic high of +100mV and a logic low of –100mV.

LVDS OUTPUT TIMING CHARACTERISTICS(1) (2)

Typical values are at +25°C, minimum and maximum values over specified temperature range of T_{MIN} = 0°C to T_{MAX} = +85°C, sampling frequency = as specified, C_{LOAD} = 5pF(3), I_{OUT} = 3.5mA, R_{LOAD} = 100Ω(4), and no internal termination, unless otherwise noted.

PARAMETER		TEST CONDITIONS(5)	AFE5804 30MSPS MIN	30MSPS TYP	30MSPS MAX	20MSPS MIN	20MSPS TYP	20MSPS MAX	10MSPS MIN	10MSPS TYP	10MSPS MAX	UNIT
t_{SU}	Data setup time(6)	Data valid(7) to zero-crossing of LCLKP	0.8			1.5			3.7			ns
t_H	Data hold time(6)	Zero-crossing of LCLKP to data becoming invalid(7)	1.2			1.9			3.9			ns
t_{PROP}	Clock propagation delay	ADC input clock rising edge cross-over to output clock (FCLKP) rising edge cross-over	9.5	13.5	17.3	9.5	14.5	17.3	10	14.7	17.1	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLKP – LCLKM)	46.5	50	52	48	50	51	49	50	51	
	Bit clock cycle-to-cycle jitter			250			250			750		ps, pp
	Frame clock cycle-to-cycle jitter			150			150			500		ps, pp
t_{RISE}, t_{FALL}	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns

(1) All characteristics are at the speeds other than the maximum rated speed for each speed grade.
(2) Timing parameters are ensured by design and characterization; not production tested.
(3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(4) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
(6) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
(7) Data valid refers to a logic high of +100mV and a logic low of –100mV.

TYPICAL CHARACTERISTICS

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

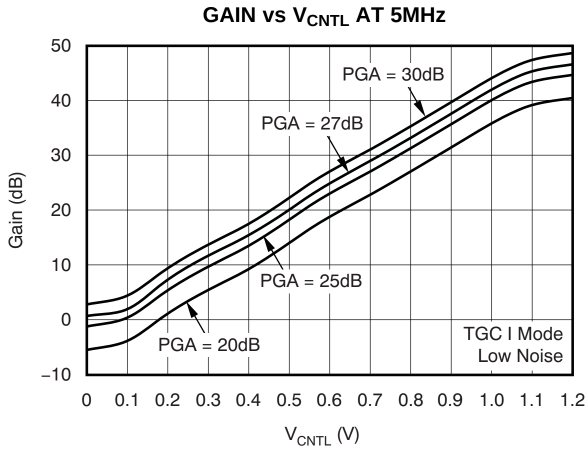


Figure 3.

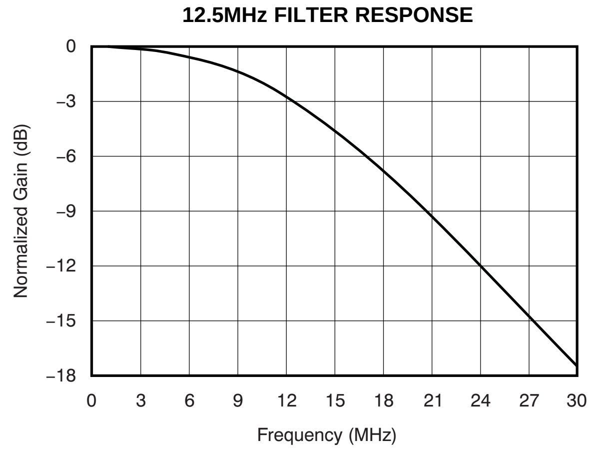


Figure 4.

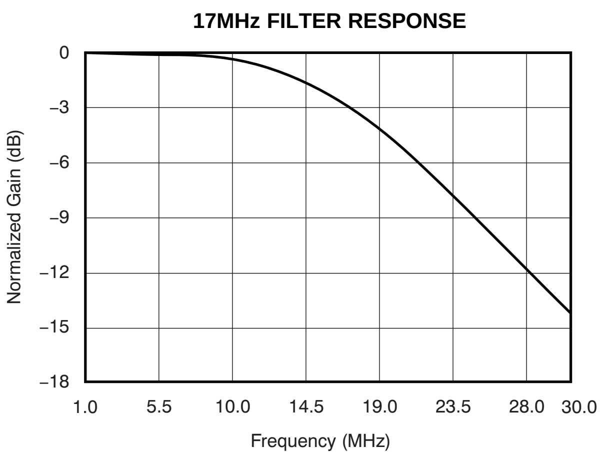


Figure 5.

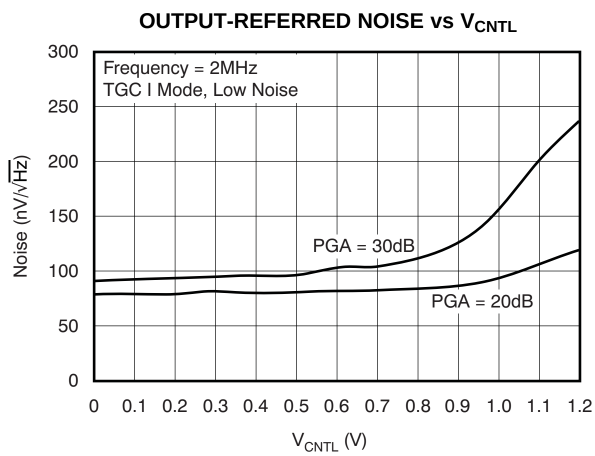


Figure 6.

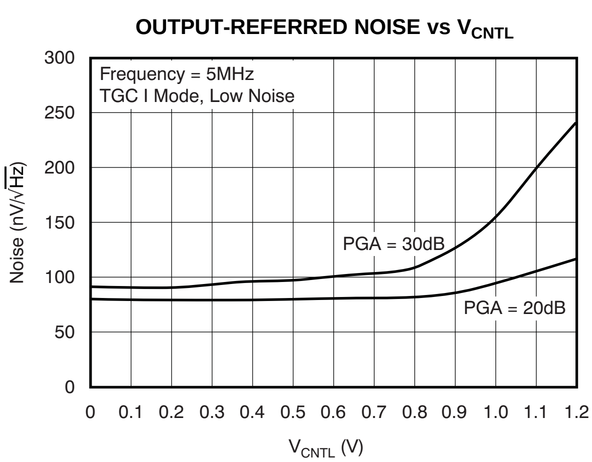


Figure 7.

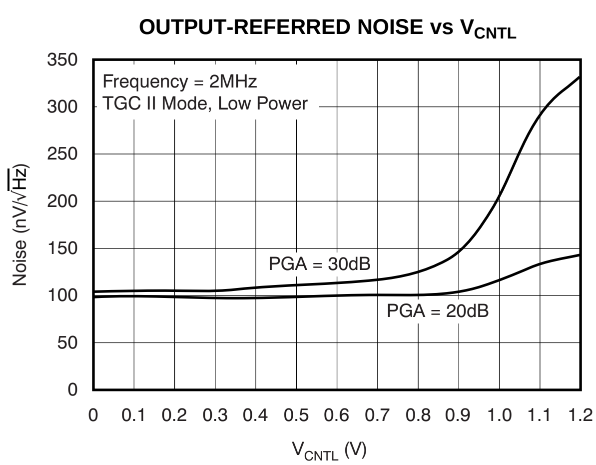


Figure 8.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

OUTPUT-REFERRED NOISE vs V_{CNTL}

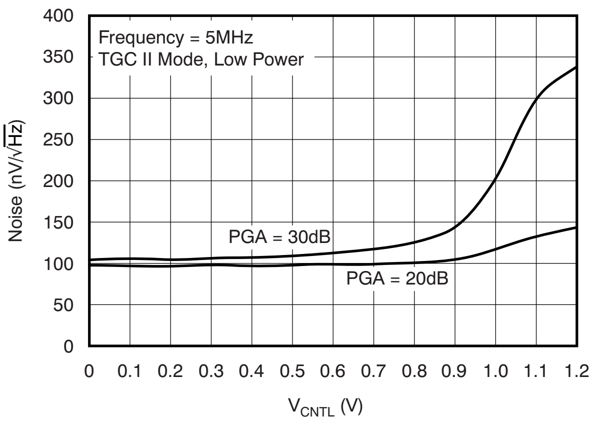


Figure 9.

OUTPUT-REFERRED NOISE vs V_{CNTL}

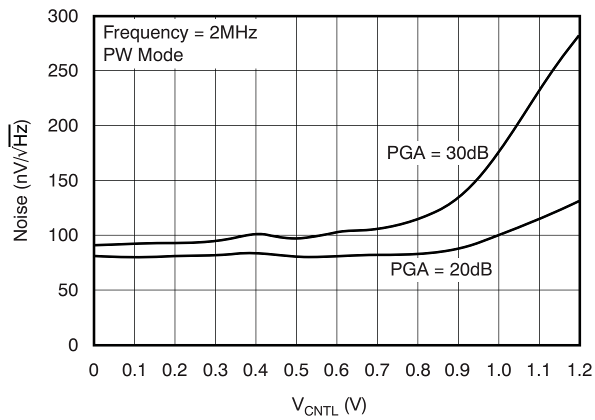


Figure 10.

OUTPUT-REFERRED NOISE vs V_{CNTL}

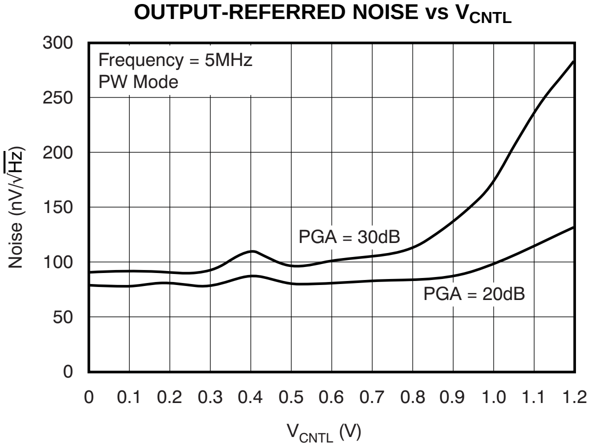


Figure 11.

INPUT-REFERRED NOISE vs V_{CNTL}

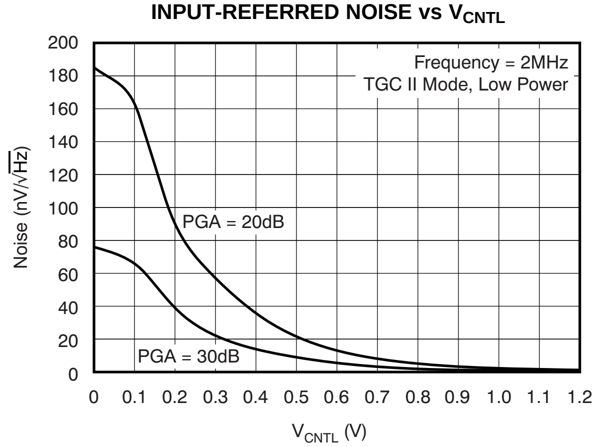


Figure 12.

INPUT-REFERRED NOISE vs V_{CNTL}

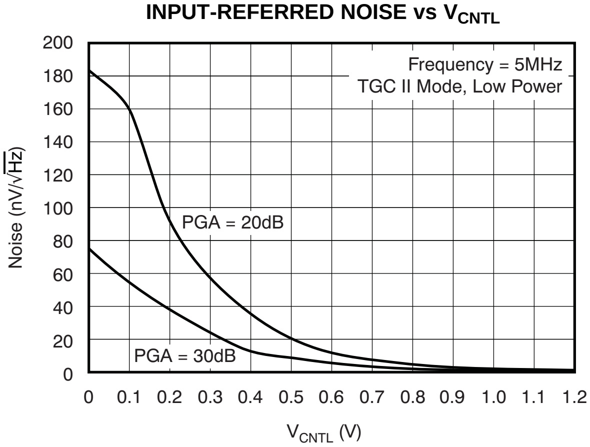


Figure 13.

INPUT-REFERRED NOISE vs V_{CNTL}

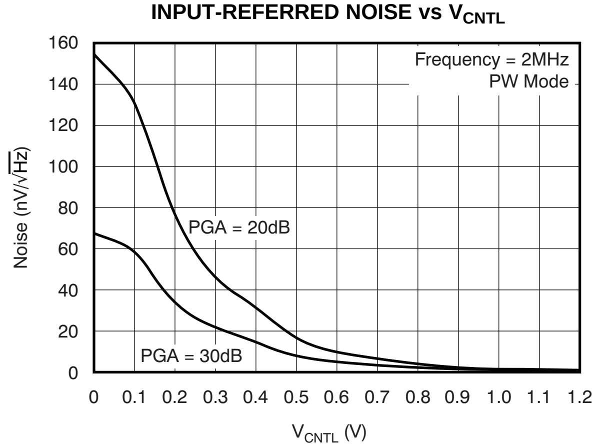


Figure 14.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

INPUT-REFERRED NOISE vs V_{CNTL}

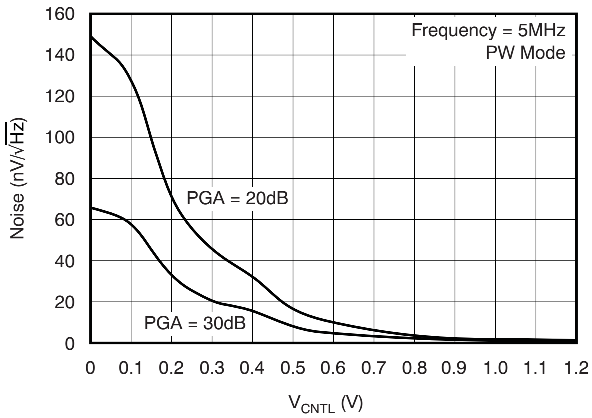


Figure 15.

NOISE FIGURE vs FREQUENCY AND R_S

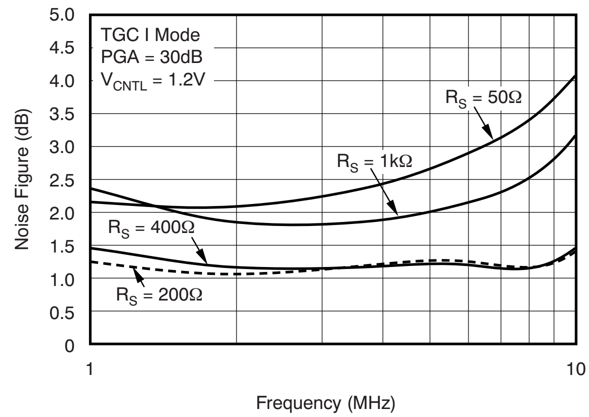


Figure 16.

INPUT-REFERRED NOISE vs FREQUENCY AND R_S

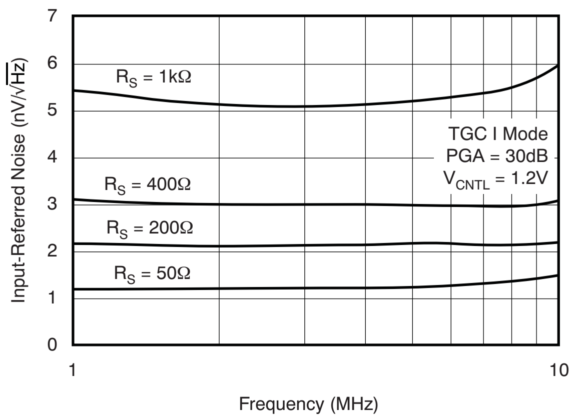


Figure 17.

OUTPUT-REFERRED NOISE vs FREQUENCY AND R_S

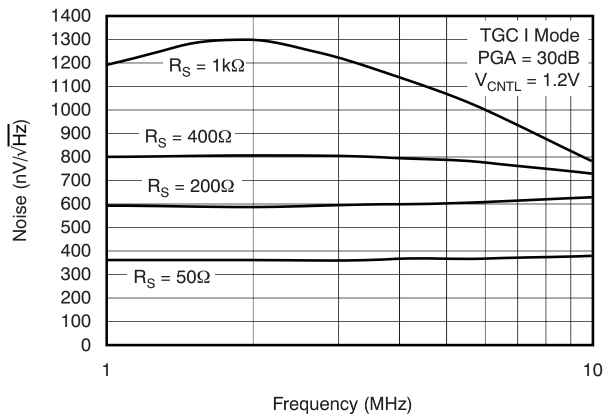


Figure 18.

OUTPUT-REFERRED NOISE vs FREQUENCY AND R_S

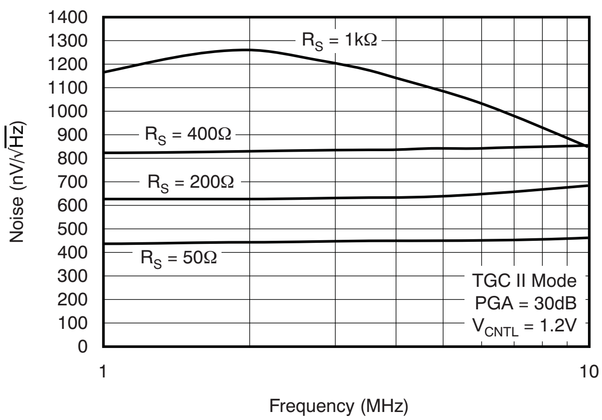


Figure 19.

OUTPUT-REFERRED NOISE vs FREQUENCY AND R_S

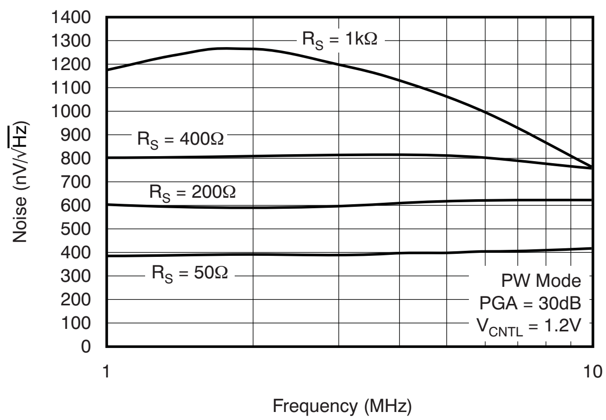


Figure 20.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

INPUT-REFERRED NOISE vs PGA

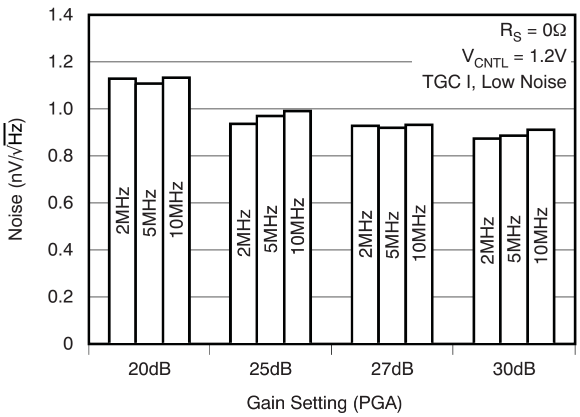


Figure 21.

INPUT-REFERRED NOISE vs PGA

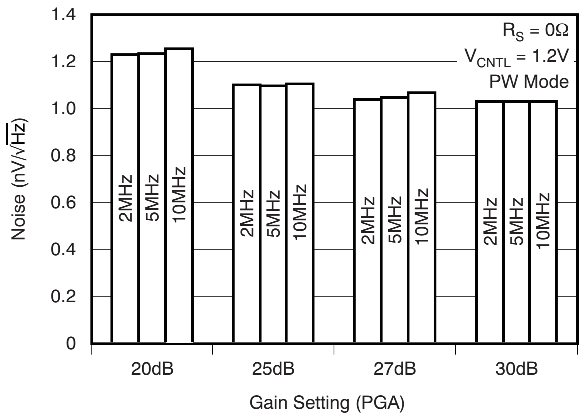


Figure 22.

INPUT-REFERRED NOISE vs PGA

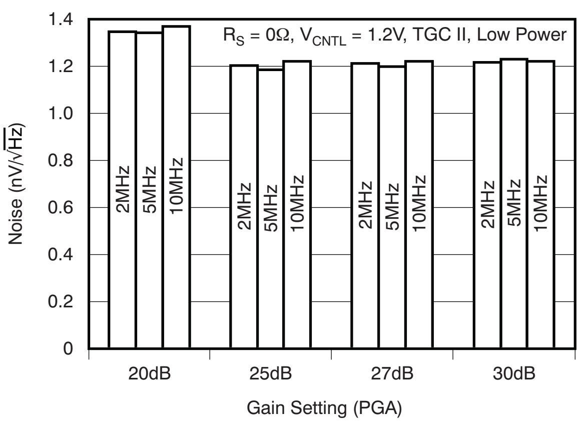


Figure 23.

GAIN MATCH HISTOGRAM (V_{CNTL} = 0.1V)

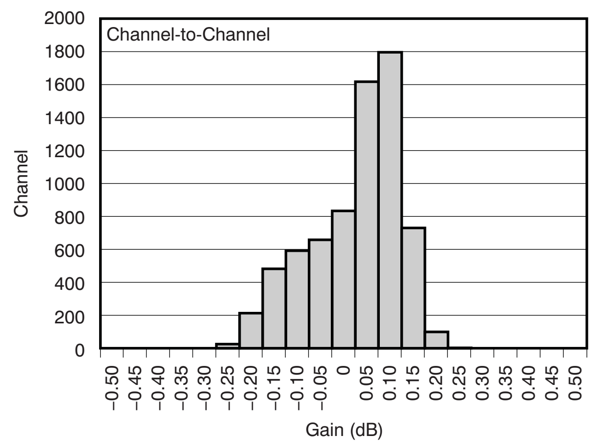


Figure 24.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

GAIN MATCH HISTOGRAM (V_{CNTL} = 0.6V)

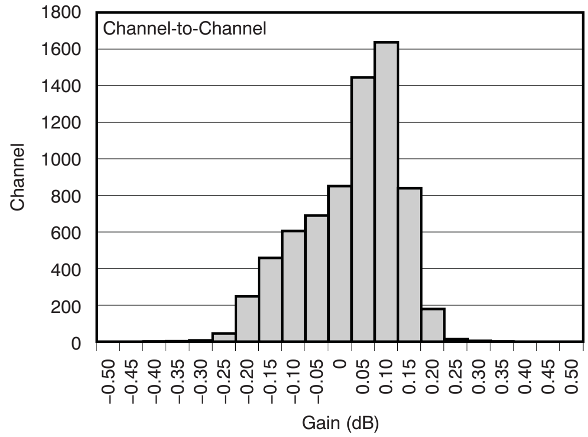


Figure 25.

GAIN MATCH HISTOGRAM (V_{CNTL} = 1.0V)

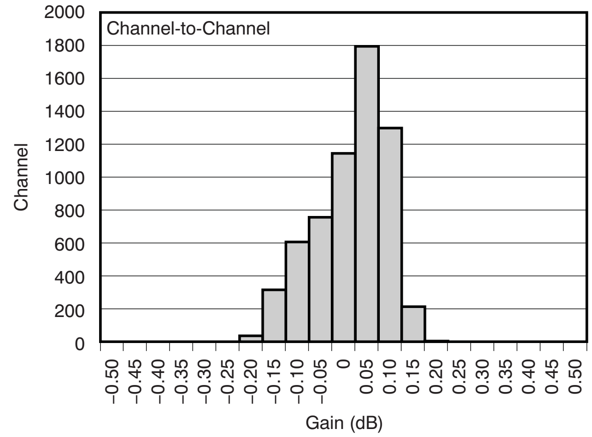


Figure 26.

CW ACCURACY HISTOGRAM

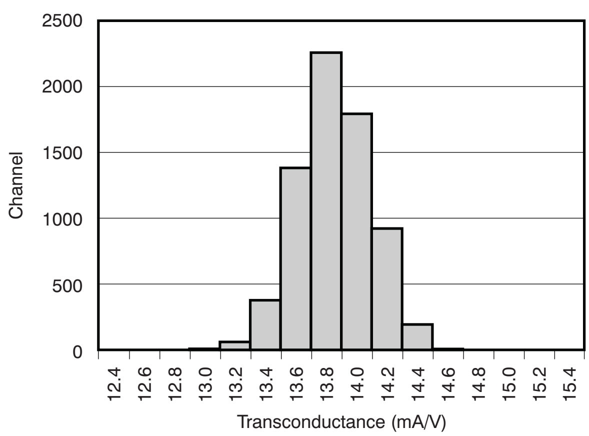


Figure 27.

OUTPUT OFFSET HISTOGRAM

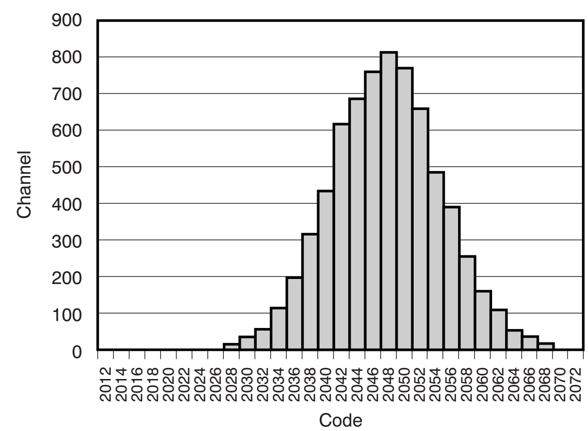


Figure 28.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

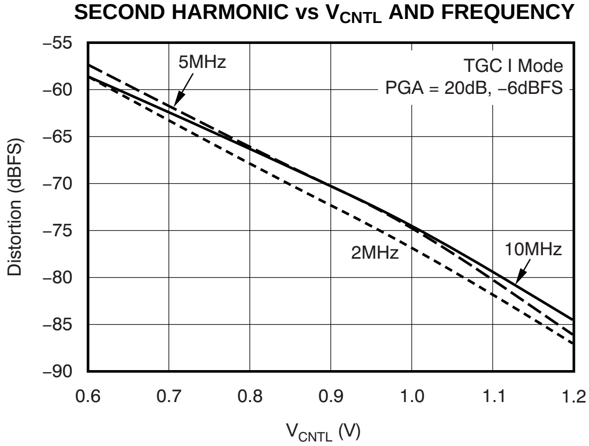


Figure 29.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

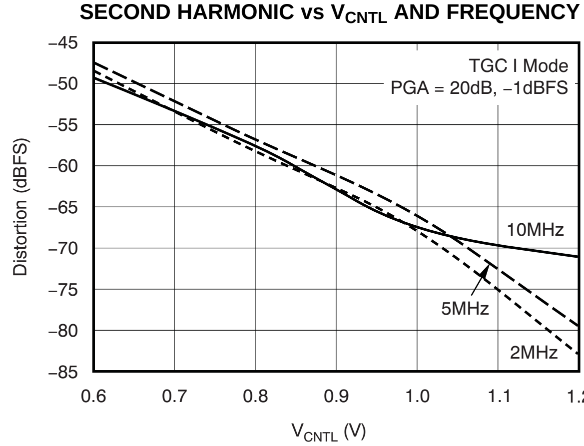


Figure 30.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

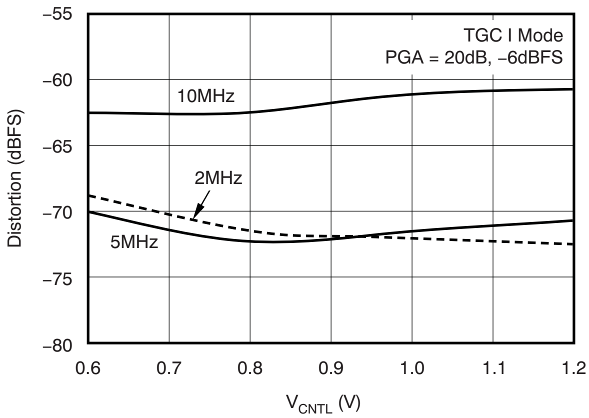


Figure 31.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

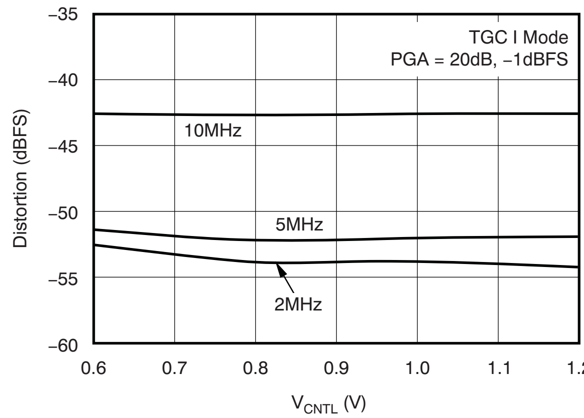


Figure 32.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

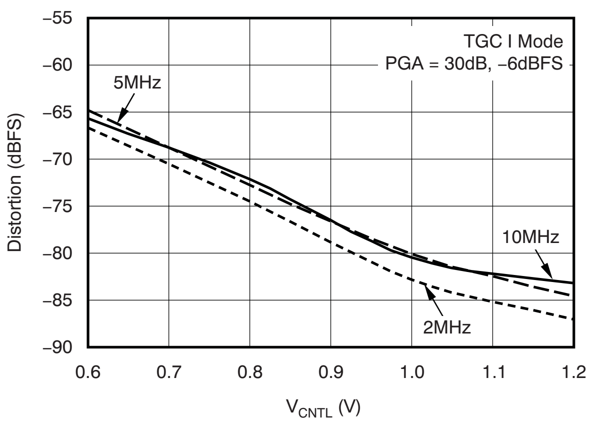


Figure 33.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

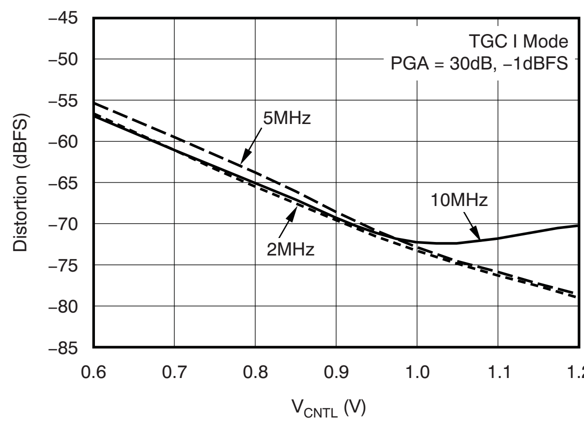


Figure 34.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

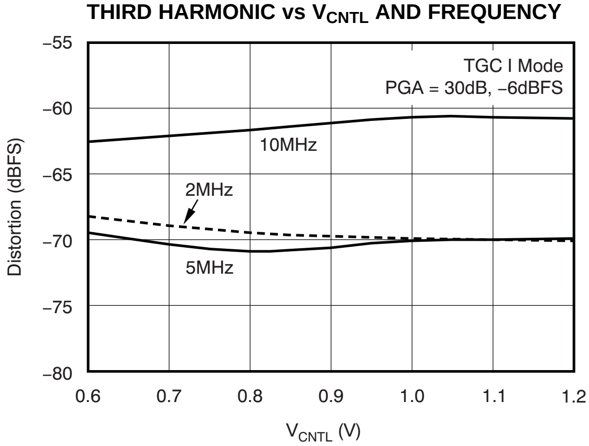


Figure 35.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

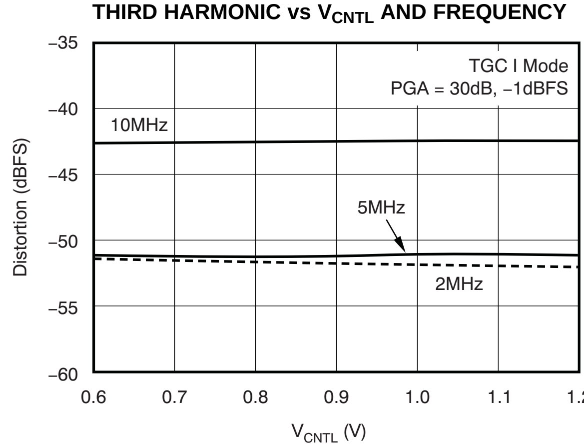


Figure 36.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

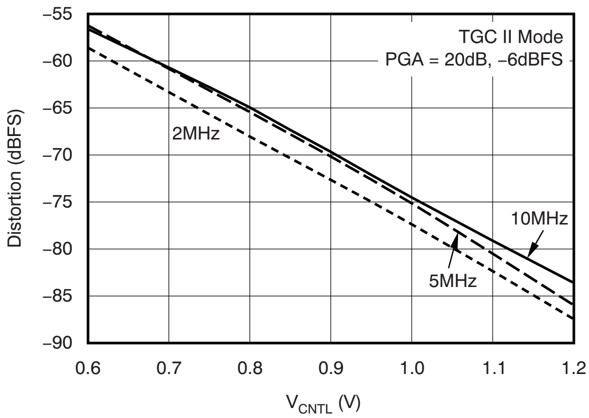


Figure 37.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

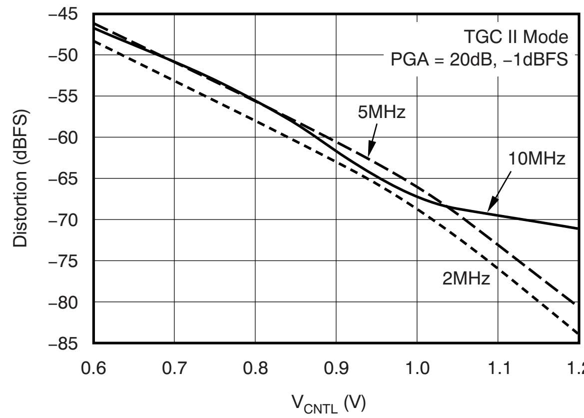


Figure 38.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

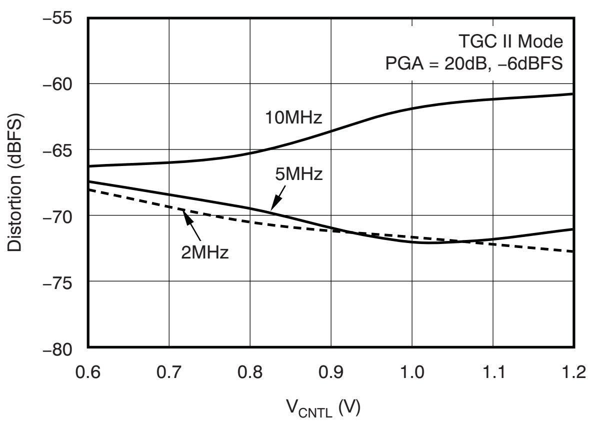


Figure 39.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

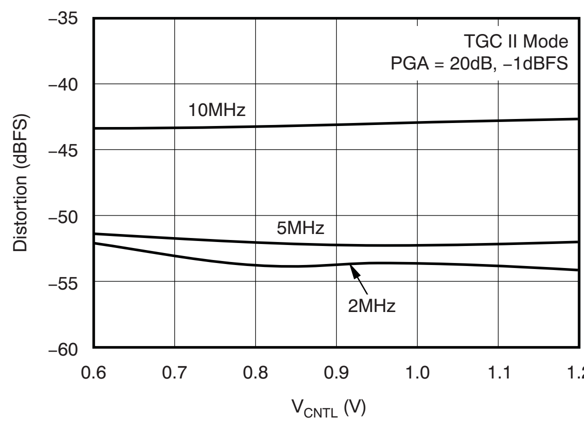


Figure 40.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

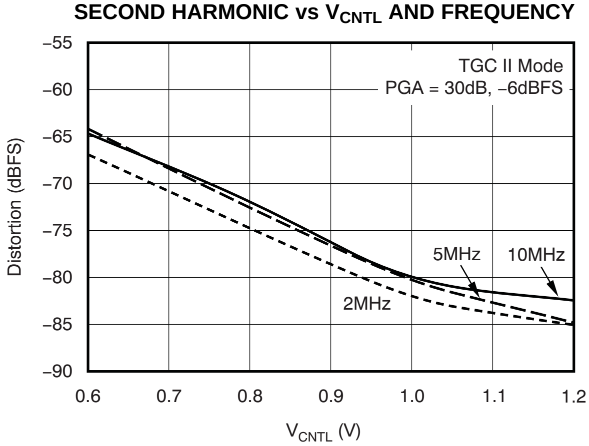


Figure 41.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

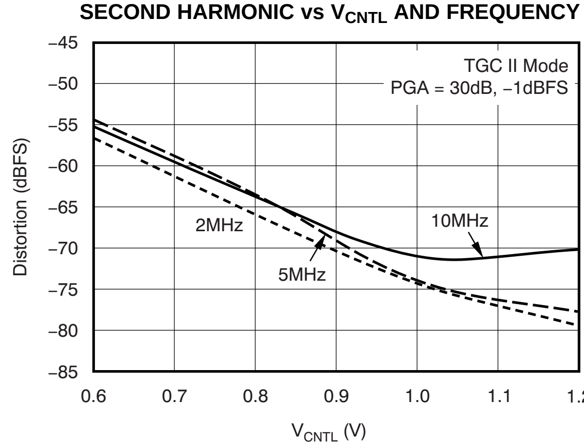


Figure 42.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

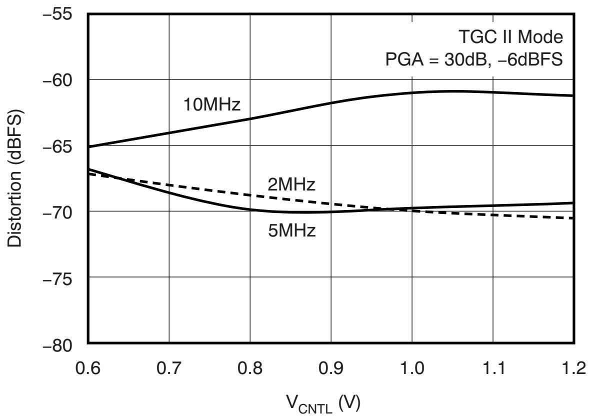


Figure 43.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

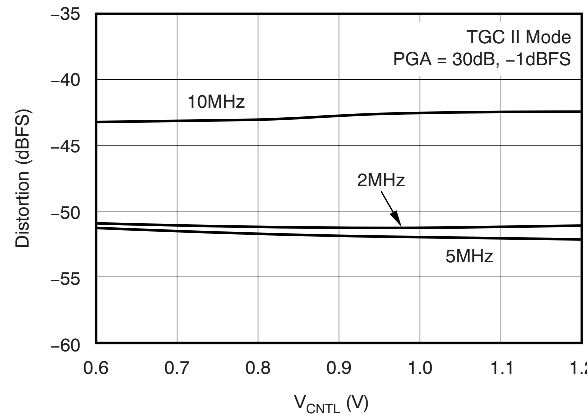


Figure 44.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

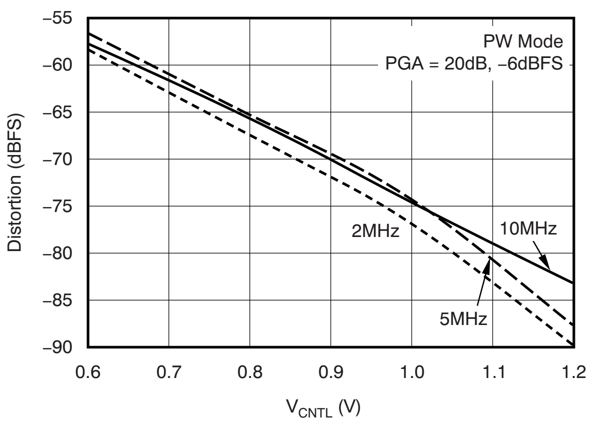


Figure 45.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

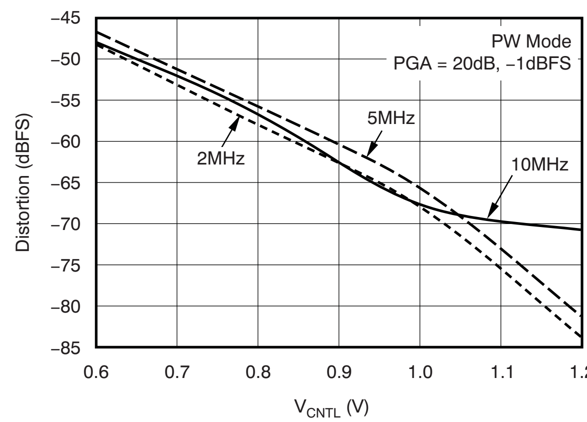


Figure 46.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

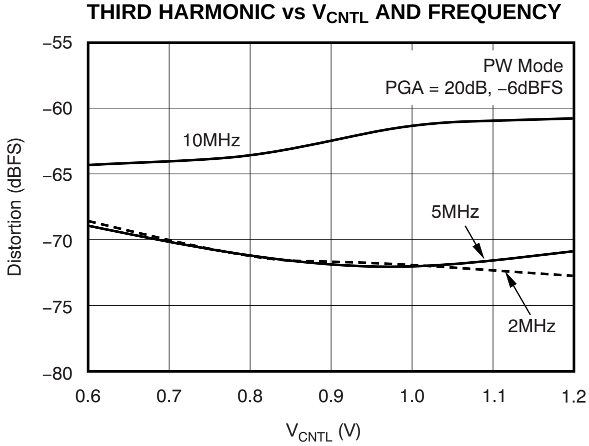


Figure 47.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

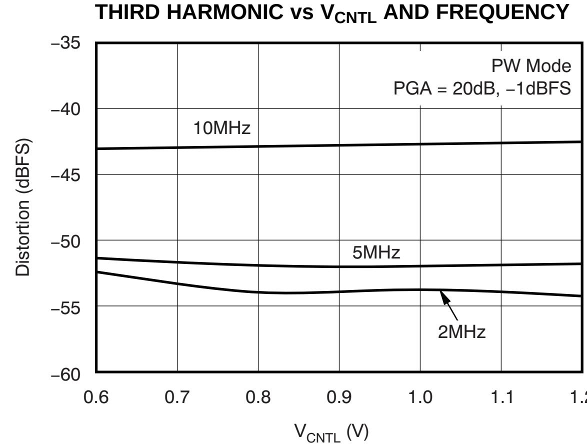


Figure 48.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

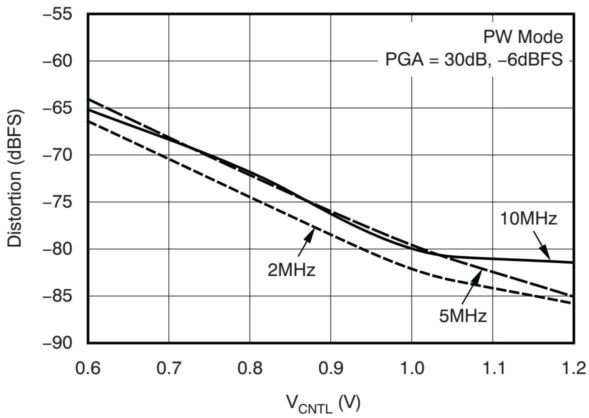


Figure 49.

SECOND HARMONIC vs V_{CNTL} AND FREQUENCY

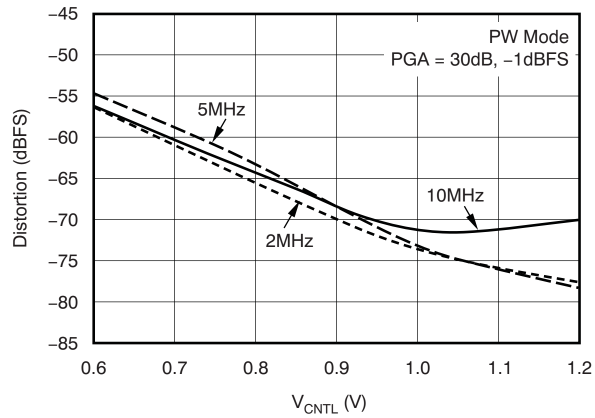


Figure 50.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

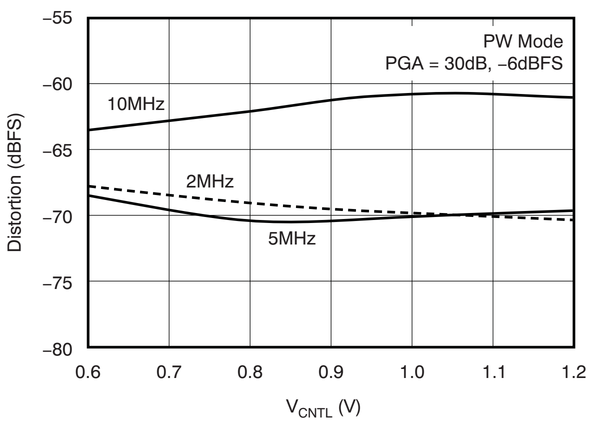


Figure 51.

THIRD HARMONIC vs V_{CNTL} AND FREQUENCY

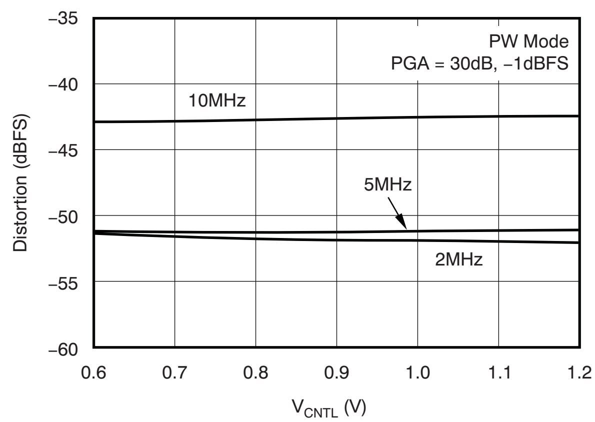


Figure 52.

CROSSTALK vs V_{CNTL}

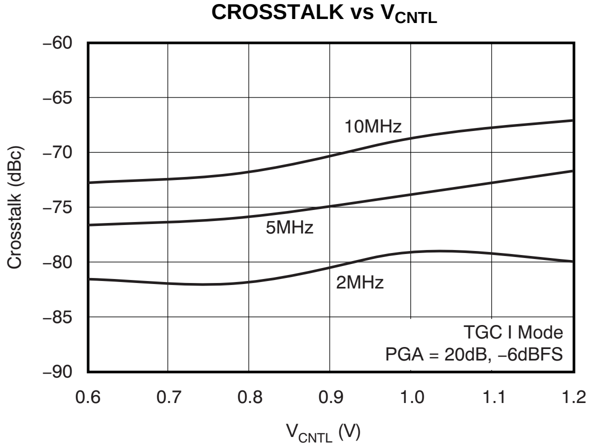


Figure 53.

CROSSTALK vs V_{CNTL}

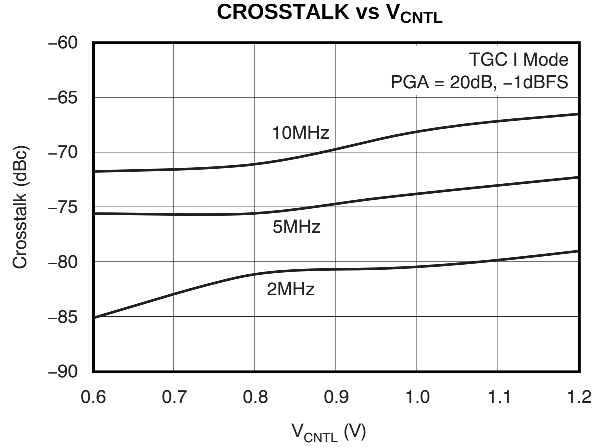


Figure 54.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

CROSSTALK vs V_{CNTL}

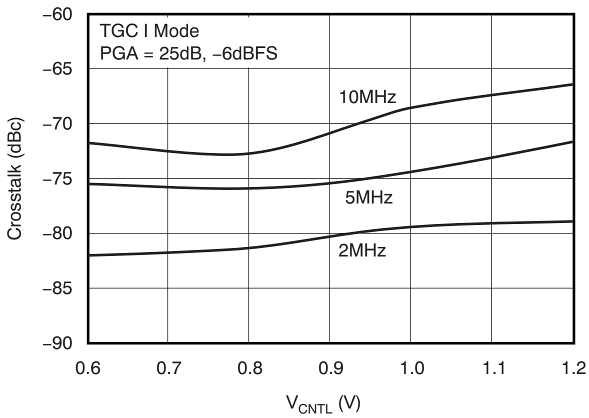


Figure 55.

CROSSTALK vs V_{CNTL}

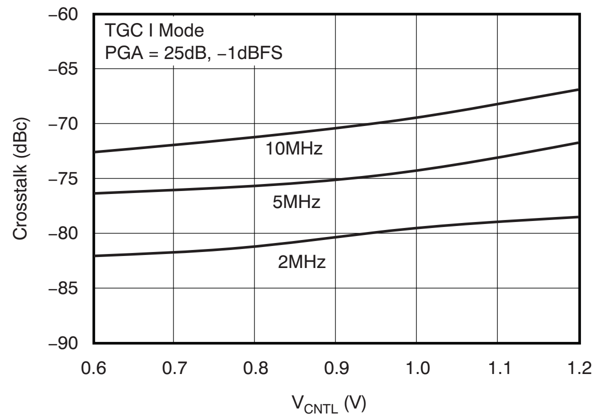


Figure 56.

CROSSTALK vs V_{CNTL}

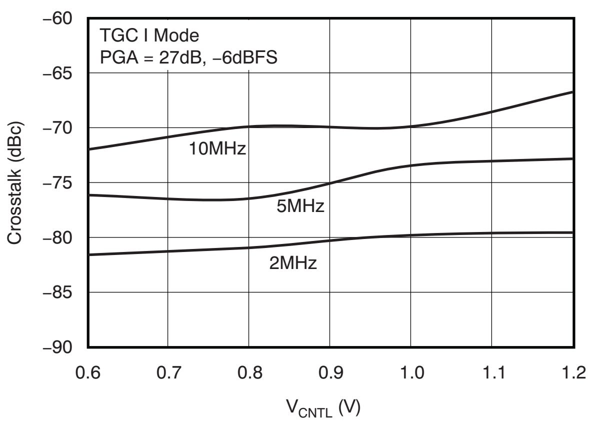


Figure 57.

CROSSTALK vs V_{CNTL}

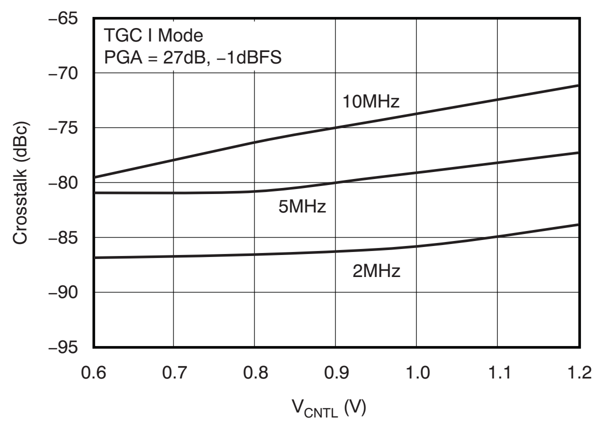


Figure 58.

CROSSTALK vs V_{CNTL}

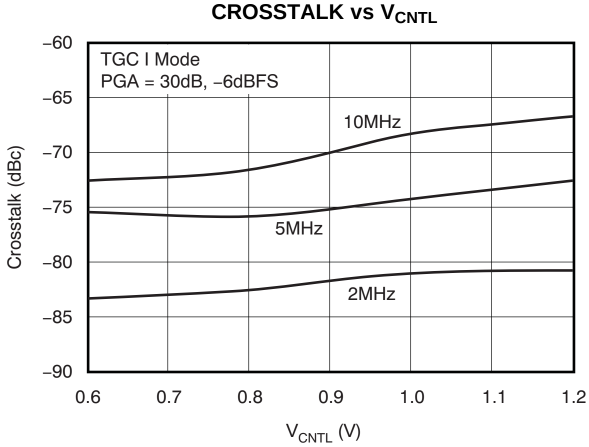


Figure 59.

CROSSTALK vs V_{CNTL}

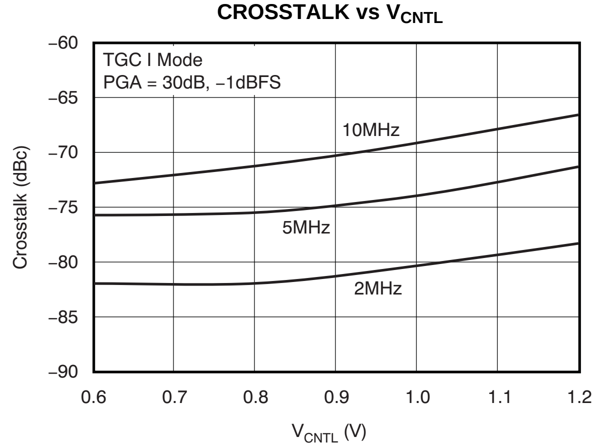


Figure 60.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

CROSSTALK vs V_{CNTL}

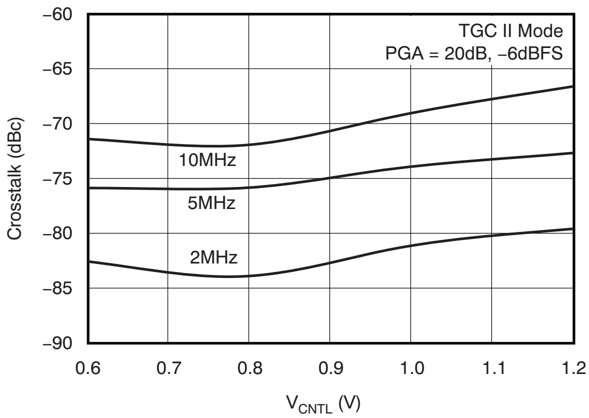


Figure 61.

CROSSTALK vs V_{CNTL}

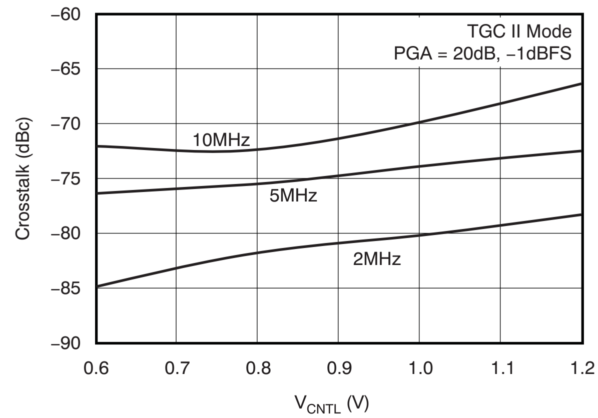


Figure 62.

CROSSTALK vs V_{CNTL}

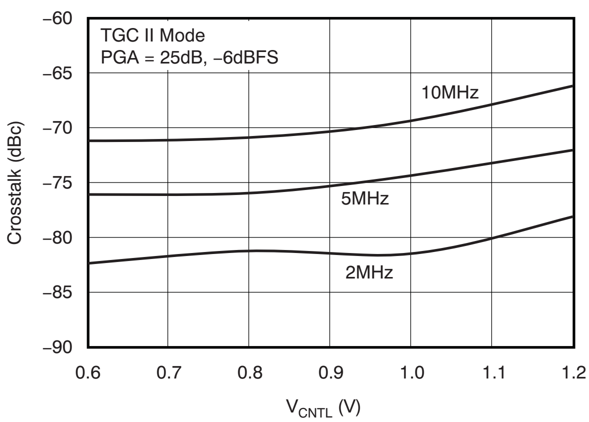


Figure 63.

CROSSTALK vs V_{CNTL}

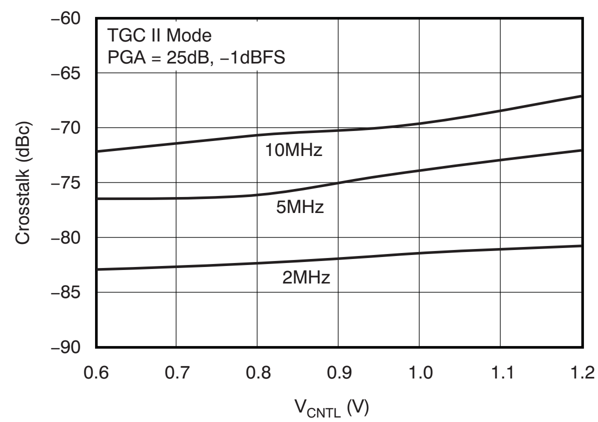


Figure 64.

CROSSTALK vs V_{CNTL}

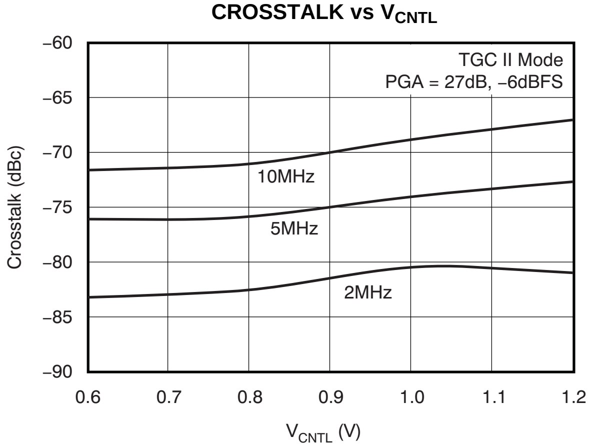


Figure 65.

CROSSTALK vs V_{CNTL}

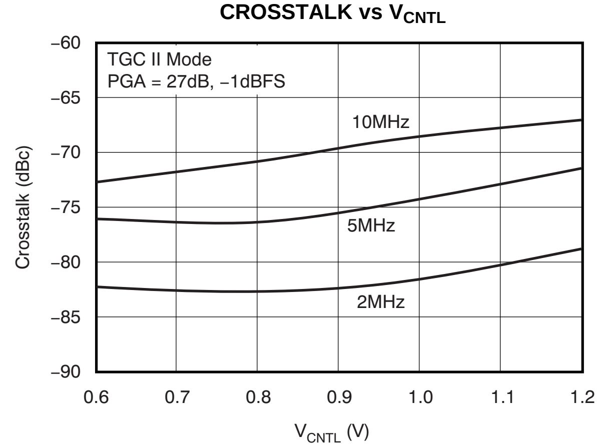


Figure 66.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

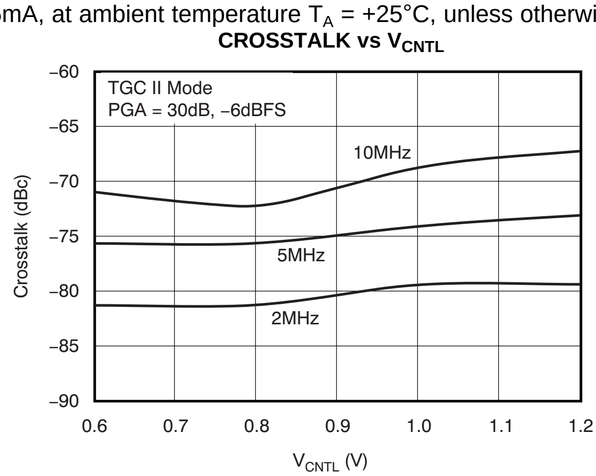


Figure 67.

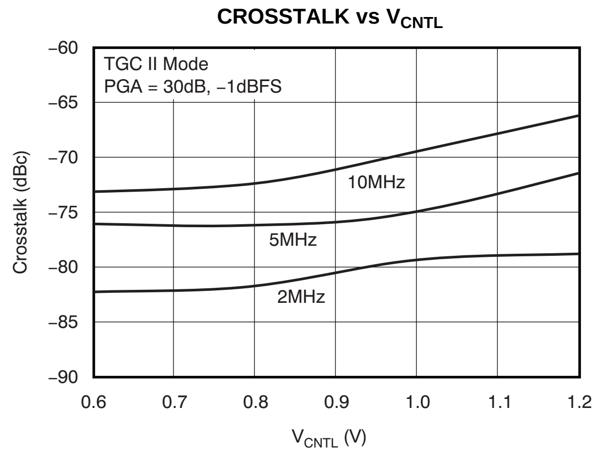


Figure 68.

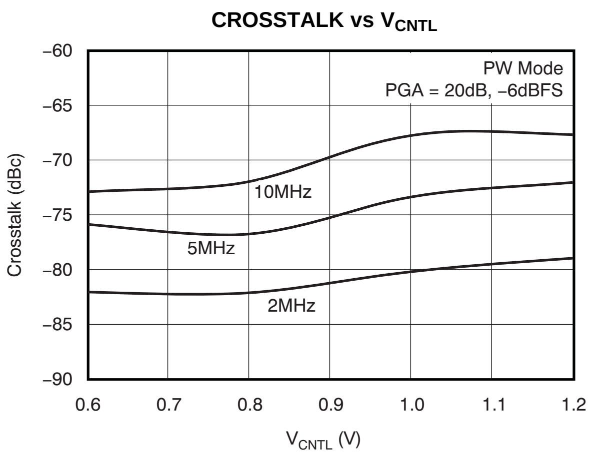


Figure 69.

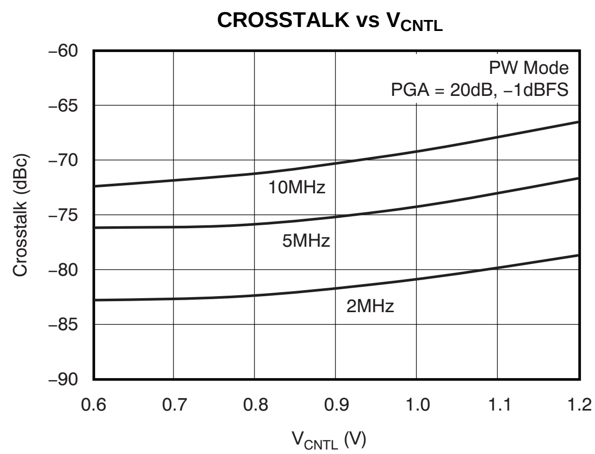


Figure 70.

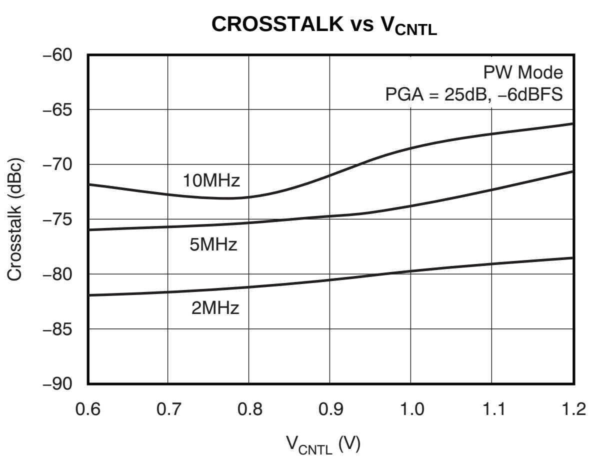


Figure 71.

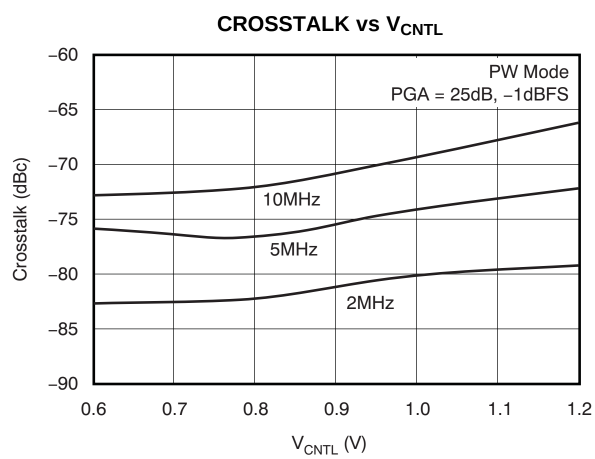


Figure 72.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

CROSSTALK vs V_{CNTL}

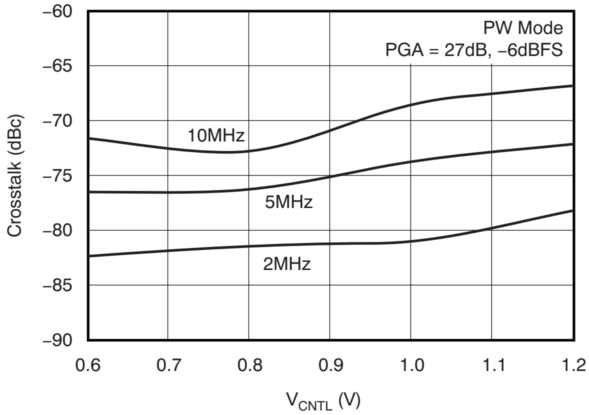


Figure 73.

CROSSTALK vs V_{CNTL}

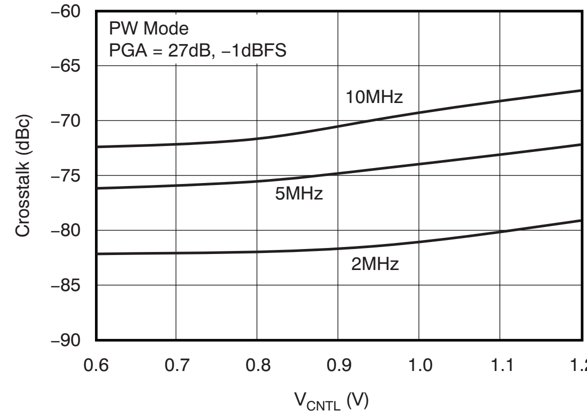


Figure 74.

CROSSTALK vs V_{CNTL}

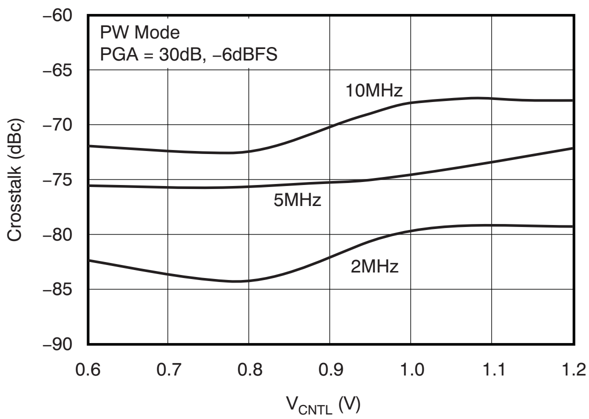


Figure 75.

CROSSTALK vs V_{CNTL}

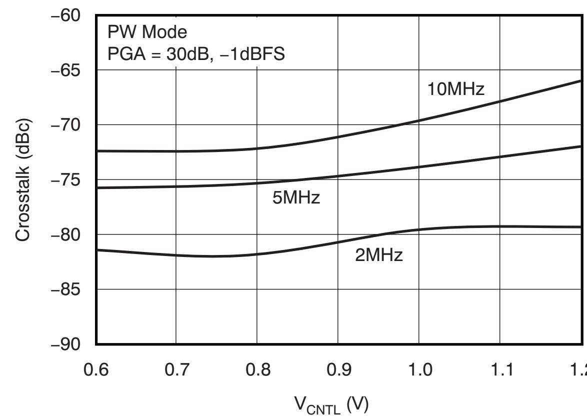


Figure 76.

OVERLOAD RECOVERY

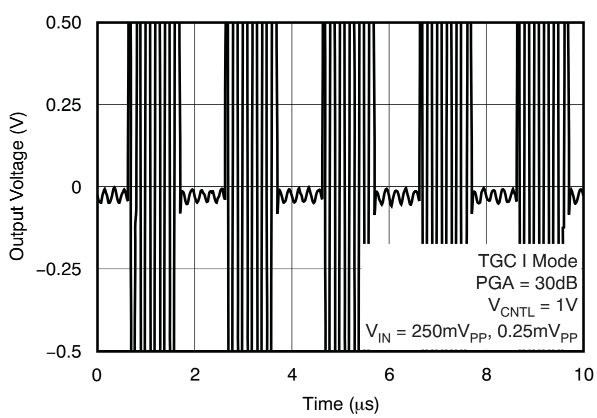


Figure 77.

OVERLOAD RECOVERY

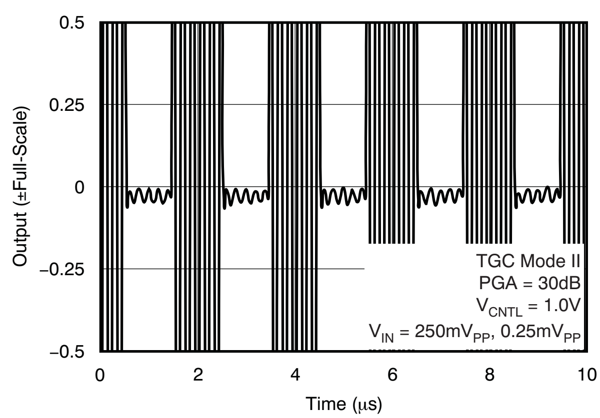


Figure 78.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

LNA OVERLOAD

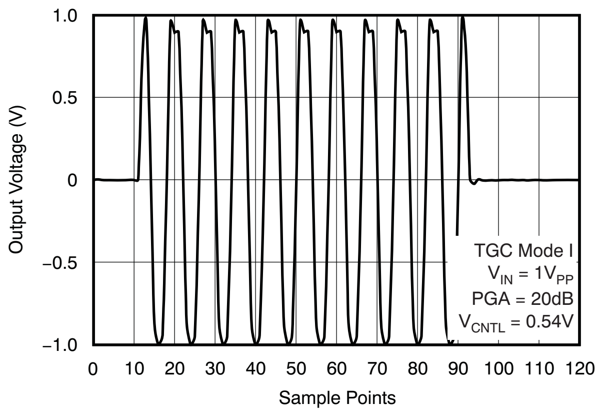


Figure 79.

FULL-CHANNEL OVERLOAD

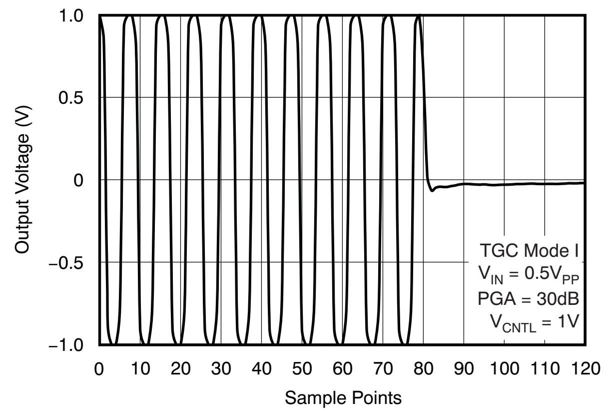


Figure 80.

V_{CNTL} RESPONSE TIME

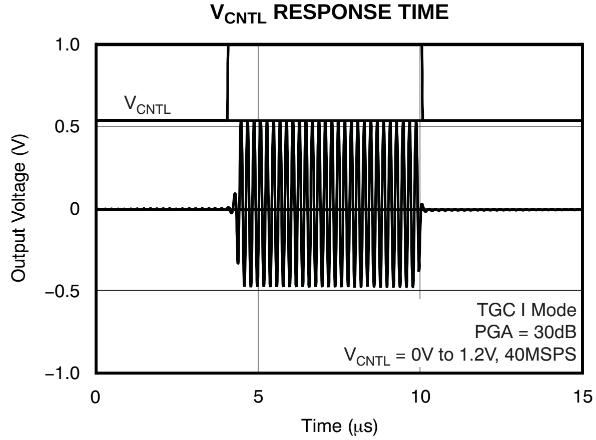


Figure 81.

PARTIAL POWER-DOWN/POWER-UP RESPONSE TIME

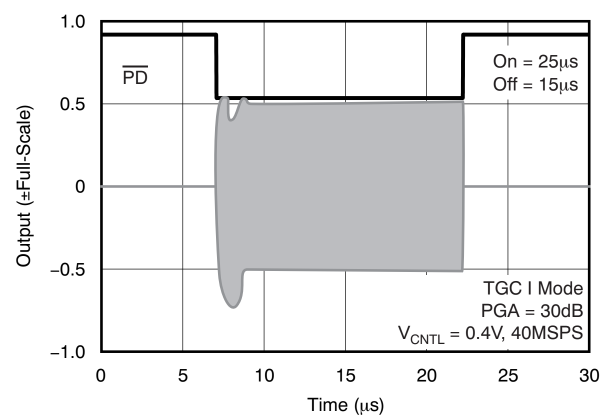


Figure 82.

SNR AND SNRD vs V_{CNTL}

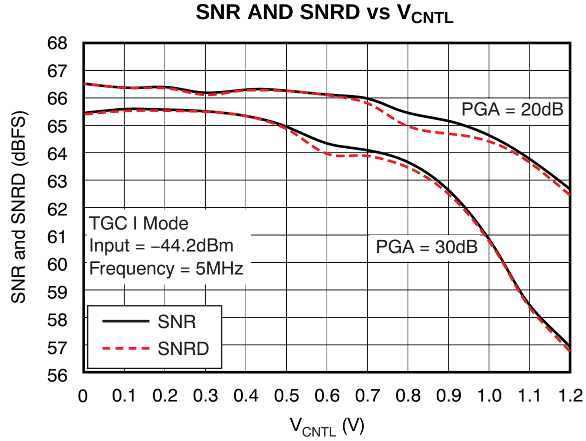


Figure 83.

MAGNITUDE AND PHASE vs FREQUENCY

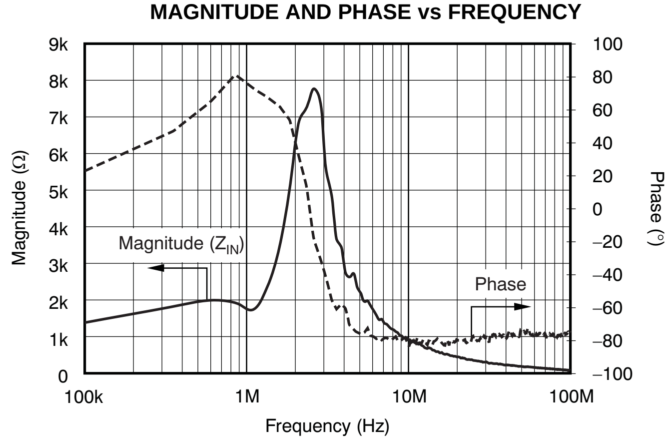


Figure 84.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

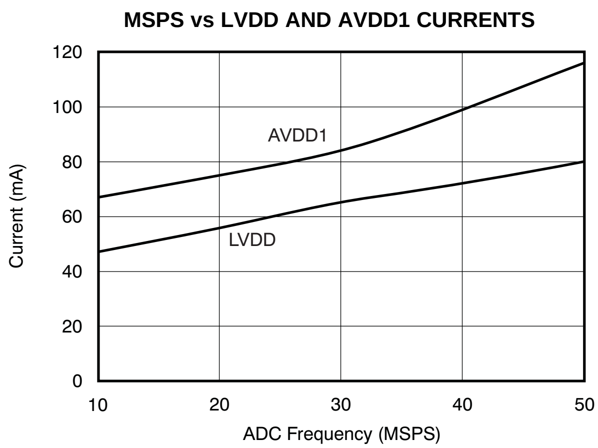


Figure 85.

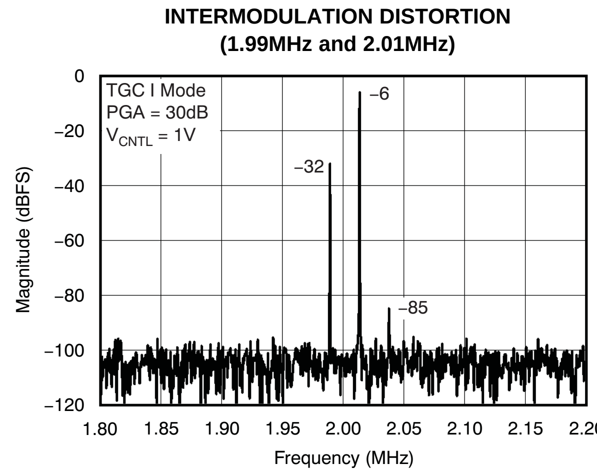


Figure 86.

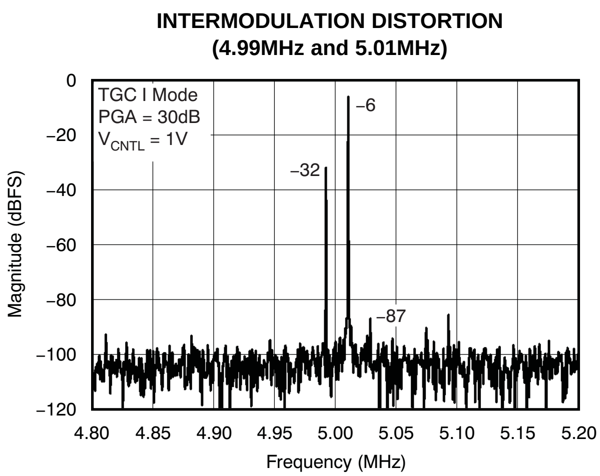


Figure 87.

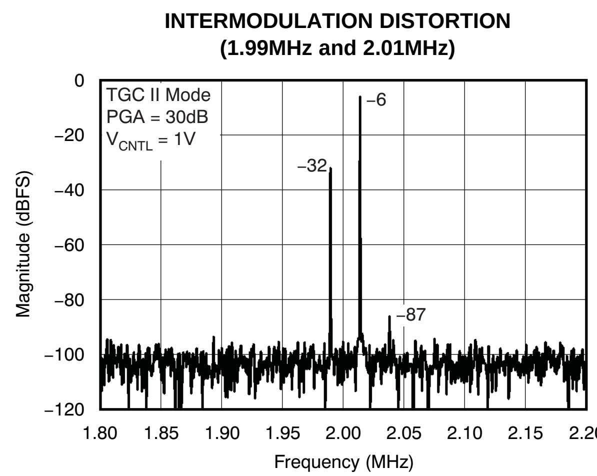


Figure 88.

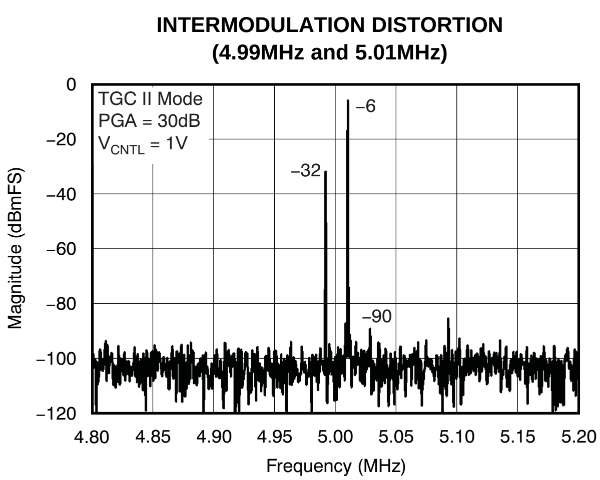


Figure 89.

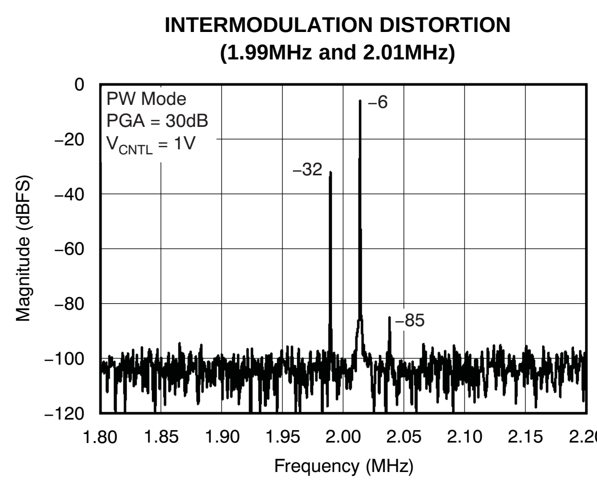


Figure 90.

TYPICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0μF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, internal reference mode, ISET = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

INTERMODULATION DISTORTION (4.99MHz and 5.01MHz)

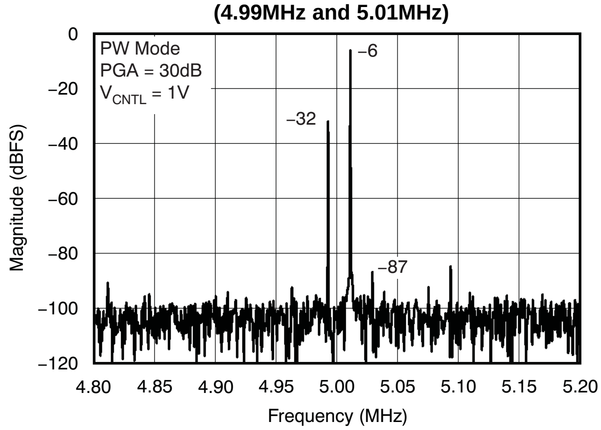


Figure 91.

SERIAL INTERFACE

The AFE5804 has a set of internal registers that can be accessed through the serial interface formed by pins $\overline{CS}$ (chip select, active low), SCLK (serial interface clock), and SDATA (serial interface data). When $\overline{CS}$ is low, the following actions occur:

- Serial shift of bits into the device is enabled
- SDATA (serial data) is latched at every rising edge of SCLK
- SDATA is loaded into the register at every 24th SCLK rising edge

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers ***must*** be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a low-going pulse on the ADS_$\overline{RESET}$ pin; or
2. Through a software reset; using the serial interface, set the S_RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the ADS_$\overline{RESET}$ pin stays high (inactive).
3. The registers in Table 2 must be programmed after the initialization stage. The power-supply ripple and clock jitter effects can be minimized.

Table 2. Register Data

ADDRESS	DATA
01	0010h
D1	0140h
DA	0001h
E1	0020h
02	0080h
01	0000h

Serial Port Interface (SPI) Information

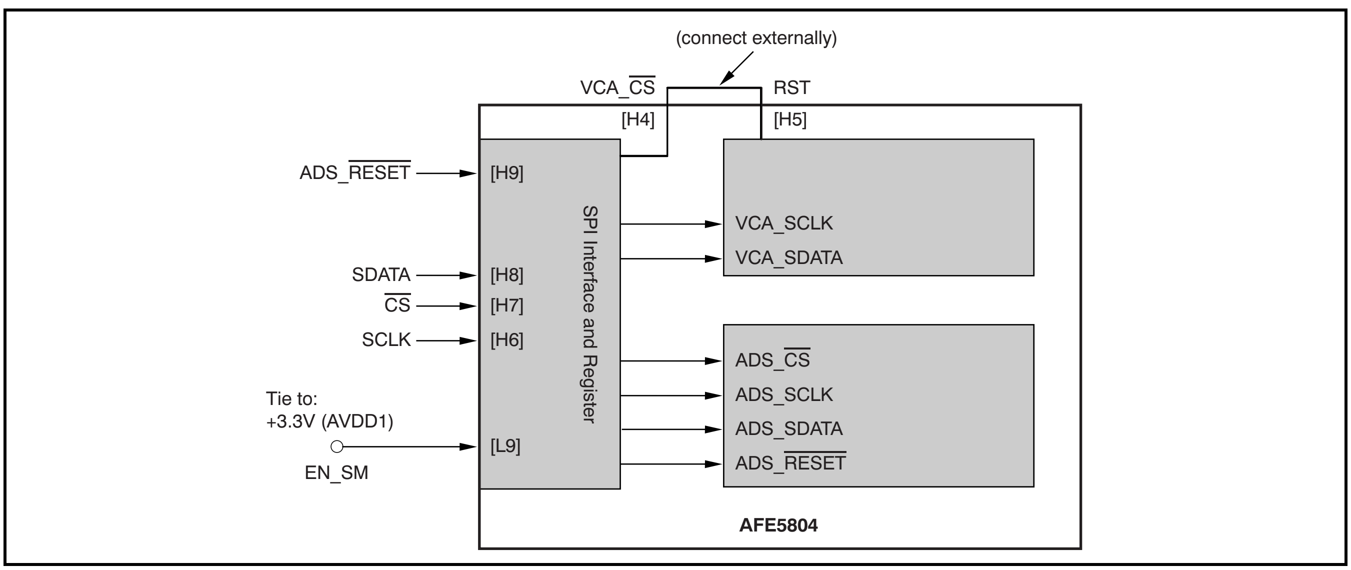
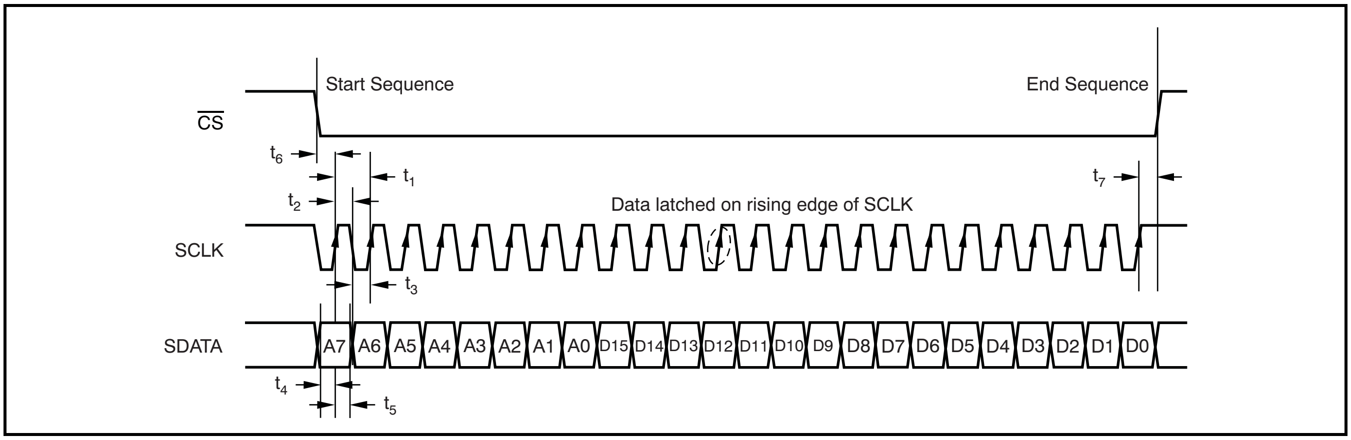


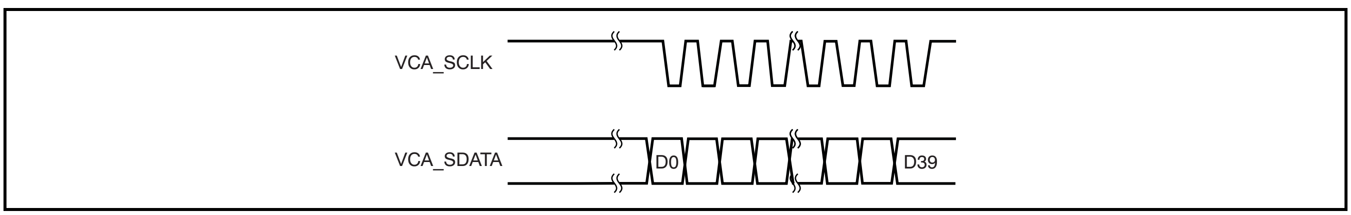
Figure 92. Typical Connection Diagram for the SPI Control Lines

SERIAL INTERFACE TIMING



PARAMETER	DESCRIPTION	AFE5804 MIN	AFE5804 TYP	AFE5804 MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{CS}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{CS}$ rising edge	8			ns

Internally-Generated VCA Control Signals



VCA_SCLK and VCA_SDATA signals are generated if:

- Registers with address 16, 17, or 18 (hex) are written to, and
- EN_SM pin is HIGH

SERIAL REGISTER MAP

Table 3. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE(1) (2) (3) (4)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
00																X	S_RST	Self-clearing software RESET.	Inactive
03	0	0	0	0	0	0	0	0	0	0	RES_ VCA	0	0	0	0	0			
16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	VCA_SDATA <0:15>	See Table 5 information	D5 = 1 (TGC mode)
17	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VCA_SDATA <16:31>	See Table 5 information	
18									X	X	X	X	X	X	X	X	VCA_DATA <32:39>	See Table 5 information	
0F													X	X	X	X	PDN_CH<1:4>	Channel-specific ADC power-down mode.	Inactive
									X	X	X	X					PDN_CH<8:5>	Channel-specific ADC power-down mode.	Inactive
								X									PDN_PARTIAL	Partial power-down mode (fast recovery from power-down).	Inactive
						0	X										PDN_COMPLETE	Register mode for complete power-down (slower recovery).	Inactive
						X	0										PDN_PIN_CFG	Configures the PD pin for partial power-down mode.	Complete power-down
11														X	X	X	ILVDS_LCLK<2:0>	LVDS current drive programmability for LCLKM and LCLKP pins.	3.5mA drive
										X	X	X					ILVDS_FRAME <2:0>	LVDS current drive programmability for FCLKM and FCLKP pins.	3.5mA drive
						X	X	X									ILVDS_DAT<2:0>	LVDS current drive programmability for OUTM and OUTP pins.	3.5mA drive
12		X															EN_LVDS_TERM	Enables internal termination for LVDS buffers.	Termination disabled
		1												X	X	X	TERM_LCLK<2:0>	Programmable termination for LCLKM and LCLKP buffers.	Termination disabled
		1								X	X	X					TERM_FRAME <2:0>	Programmable termination for FCLKM and FCLKP buffers.	Termination disabled
		1				X	X	X									TERM_DAT<2:0>	Programmable termination for OUTM and OUTP buffers.	Termination disabled
14													X	X	X	X	LFNS_CH<1:4>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
									X	X	X	X					LFNS_CH<8:5>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
25										X	0	0					EN_RAMP	Enables a repeating full-scale ramp pattern on the outputs.	Inactive
										0	X	0					DUALCUSTOM_ PAT	Enables the mode wherein the output toggles between two defined codes.	Inactive
										0	0	X					SINGLE_CUSTOM _PAT	Enables the mode wherein the output is a constant specified code.	Inactive
															X	X	BITS_CUSTOM1 <11:10>	2MSBs for a single custom pattern (and for the first code of the dual custom pattern). <11> is the MSB.	Inactive
													X	X			BITS_CUSTOM2 <11:10>	2MSBs for the second code of the dual custom pattern.	Inactive
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1 <9:0>	10 lower bits for the single custom pattern (and for the first code of the dual custom pattern). <0> is the LSB.	Inactive
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2 <9:0>	10 lower bits for the second code of the dual custom pattern.	Inactive

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
(2) X = Register bit referenced by the corresponding name and description (default setting is listed in table).
(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
(4) Multiple functions in a register should be programmed in a single write operation.

Table 3. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE(1) (2) (3) (4) (continued)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
2A													X	X	X	X	GAIN_CH4<3:0>	Programmable gain channel 4.	0dB gain
									X	X	X	X					GAIN_CH3<3:0>	Programmable gain channel 3.	0dB gain
					X	X	X	X									GAIN_CH2<3:0>	Programmable gain channel 2.	0dB gain
	X	X	X	X													GAIN_CH1<3:0>	Programmable gain channel 1.	0dB gain
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain channel 5.	0dB gain
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain channel 6.	0dB gain
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain channel 7.	0dB gain
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain channel 8.	0dB gain
42	1								1							X	DIFF_CLK	Differential clock mode.	Single-ended clock
	1								1					X			EN_DCC	Enables the duty-cycle correction circuit.	Disabled
	1								1				X				EXT_REF_VCM	Drives the external reference mode through the VCM pin.	External reference drives REFT and REFB
	1								1	X	X						PHASE_DDR<1:0>	Controls the phase of LCLK output relative to data.	90 degrees
45															0	X	PAT_DESKEW	Enables deskew pattern mode.	Inactive
															X	0	PAT_SYNC	Enables sync pattern mode.	Inactive
46	1						1							X			BTC_MODE	Binary twos complement format for ADC output.	Straight offset binary
	1						1						X				MSB_FIRST	Serialized ADC output comes out MSB-first.	LSB-first output
	1						1					X					EN_SDR	Enables SDR output mode (LCLK becomes a 12x input clock).	DDR output mode
	1		1				1					1					FALL_SDR	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode.	Rising edge of LCLK in middle of data window

SUMMARY OF FEATURES

FEATURES	DEFAULT	SELECTION	POWER IMPACT (Relative to Default) AT f_S = 50MSPS
ANALOG FEATURES			
Internal or external reference (driven on the REFT and REFB pins)	N/A	Pin	Internal reference mode takes approximately 20mW more power on AVDD1
External reference driven on the CM pin	Off	Register 42	Approximately 8mW less power on AVDD1
Duty cycle correction circuit	Off	Register 42	Approximately 7mW more power on AVDD1
Low-frequency noise suppression	Off	Register 14	With zero input to the ADC, low-frequency noise suppression causes digital switching at f_S/2, thereby increasing LVDD power by approximately 5.5mW/channel
Single-ended or differential clock	Single-ended	Register 42	Differential clock mode takes approximately 7mW more power on AVDD1
Power-down mode	Off	Pin and register 0F	Refer to the *Power-Down Modes* section in the Electrical Characteristics table
DIGITAL FEATURES			
Programmable digital gain (0dB to 12dB)	0dB	Registers 2A and 2B	No difference
Straight offset or BTC output	Straight offset	Register 46	No difference
Swap polarity of analog input pins	Off	Register 24	No difference
LVDS OUTPUT PHYSICAL LAYER			
LVDS internal termination	Off	Register 12	Approximately 7mW more power on AVDD
LVDS current programmability	3.5mA	Register 11	As per LVDS clock and data buffer current setting
LVDS OUTPUT TIMING			
LSB- or MSB-first output	LSB-first	Register 46	No difference
DDR or SDR output	DDR	Register 46	SDR mode takes approximately 2mW more power on LVDD (at f_S = 30MSPS)
LCLK phase relative to data output	Refer to Figure 94	Register 42	No difference

DESCRIPTION OF SERIAL REGISTERS

SOFTWARE RESET

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
00																X	S_RST

Software reset is applied when the RST bit is set to '1'; setting this bit resets all internal registers and self-clears to '0'.

Table 4. VCA Register Information

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03	0	0	0	0		0	0	0	0	0	RES_VCA	0	0	0	0	0
16	VCA D15	VCA D14	VCA D13	VCA D12	VCA D11	VCA D10	VCA D9	VCA D8	VCA D7	VCA D6	VCA D5	VCA D4	VCA D3	VCA D2	1(1) D1	1(1) D0
17	VCA D31	VCA D30	VCA D29	VCA D28	VCA D27	VCA D26	VCA D25	VCA D24	VCA D23	VCA D22	VCA D21	VCA D20	VCA D19	VCA D18	VCA D17	VCA D16
18									VCA D39	VCA D38	VCA D37	VCA D36	VCA D35	VCA D34	VCA D33	VCA D32

(1) Bits D0 and D1 of register 16 are forced to '1'.

- VCA_SCLK and VCA_SDATA become active only when one of the registers 16, 17 or 18 (address in hex) of the AFE5804 are written into.
- The contents of all three registers (total 40 bits) are written on VCA_SDATA even if only one of the above registers is written to. This condition is only valid if the content of the register has changed because of the most recent write. Writing contents that are the same as existing contents does not trigger activity on VCA_SDATA.
- For example, if register 17 is written to after a RESET is applied, then the contents of register 17 as well as the default values of the bits in registers 16 and 18 are written to VCA_SDATA.
- If register 16 is then written to, then the new contents of register 16, the previously written contents of register 17, and the default contents of register 18 are written to VCA_SDATA. Note that regardless of what is written to D0 and D1 of register 16, the respective outputs on VCA_SDATA are always ‘1’.
- Alternatively, all three registers (16, 17 and 18) can also be written within one write cycle of the ADC serial interface. In that case, there would be 48 consecutive SCLK edges within the same $\overline{CS}$ active window.
- VCA_SCLK is generated using an oscillator (running at approximately 6MHz) inside the AFE5804, but the oscillator is gated so that it is active only during the write operation of the 40 VCA bits.
- The external ADC SCLK frequency can be greater than 6MHz. To ensure the SDATA transfer reliability, ≥ 1µs gap is recommended between programming two VCA registers consecutively.

VCA Reset

- VCA_$\overline{CS}$ should be permanently connected to the RST-input.
- When VCA_$\overline{CS}$ goes high (either because of an active low pulse on ADS_$\overline{RESET}$ for more than 10ns or as a result or setting bit RES_VCA), the following functions are performed inside the AFE5804:
  - Bits D0 and D1 of register 16 are forced to ‘1’
  - All other bits in registers 16, 17 and 18 are RESET to the respective default values (‘0’ for all bits except D5 of register 16 which is set to a default of ‘1’).
  - No activity on signals VCA_SCLK and VCA_SDATA.
- If bit RES_VCA has been set to ‘1’, then the state machine is in the RESET state until RES_VCA is set to ‘0’.

INPUT REGISTER BIT MAPS

Table 5. VCA Register Map

BYTE 1	BYTE 2		BYTE 3		BYTE 4		BYTE 5	
D0:D7	D8:D11	D12:D15	D16:D19	D20:D23	D24:D27	D28:D31	D32:D35	D36:D39
Control	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8

Table 6. Byte 1—Control Byte Register Map

BIT NUMBER	BIT NAME	DESCRIPTION
D0 (LSB)	1	Start bit; this bit is permanently set high = 1
D1	WR	Write bit; this bit is permanently set high = 1
D2	PWR	1= Power-down mode enabled
D3	BW	Low-pass filter bandwidth setting (see Table 11)
D4	M0	(see Table 12)
D5	M1	(see Table 12)
D6	PG0	LSB of PGA gain control (see Table 13)
D7 (MSB)	PG1	MSB of PGA gain control

Table 7. Byte 2—First Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D8 (LSB)	DB1:1	Channel 1, LSB of matrix control
D9	DB1:2	Channel 1, matrix control
D10	DB1:3	Channel 1, matrix control
D11	DB1:4	Channel 1, MSB of matrix control
D12	DB2:1	Channel 2, LSB of matrix control
D13	DB2:2	Channel 2, matrix control
D14	DB2:3	Channel 2, matrix control
D15 (MSB)	DB2:4	Channel 2, MSB of matrix control

Table 8. Byte 3—Second Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D16 (LSB)	DB3:1	Channel 3, LSB of matrix control
D17	DB3:2	Channel 3, matrix control
D18	DB3:3	Channel 3, matrix control
D19	DB3:4	Channel 3, MSB of matrix control
D20	DB4:1	Channel 4, LSB of matrix control
D21	DB4:2	Channel 4, matrix control
D22	DB4:3	Channel 4, matrix control
D23 (MSB)	DB4:4	Channel 4, MSB of matrix control

Table 9. Byte 4—Third Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D24 (LSB)	DB5:1	Channel 5, LSB of matrix control
D25	DB5:2	Channel 5, matrix control
D26	DB5:3	Channel 5, matrix control
D27	DB5:4	Channel 5, MSB of matrix control
D28	DB6:1	Channel 6, LSB of matrix control
D29	DB6:2	Channel 6, matrix control
D30	DB6:3	Channel 6, matrix control
D31 (MSB)	DB6:4	Channel 6, MSB of matrix control

Table 10. Byte 5—Fourth Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D32 (LSB)	DB7:1	Channel 7, LSB of matrix control
D33	DB7:2	Channel 7, matrix control
D34	DB7:3	Channel 7, matrix control
D35	DB7:4	Channel 7, MSB of matrix control
D36	DB8:1	Channel 8, LSB of matrix control
D37	DB8:2	Channel 8, matrix control
D38	DB8:3	Channel 8, matrix control
D39 (MSB)	DB8:4	Channel 8, MSB of matrix control

Table 11. LPF Bandwidth Setting

	SETTING	FUNCTION
BW	D3 = 0	Bandwidth set to 17MHz (default)
BW	D3 = 1	Bandwidth set to 12.5MHz

Table 12. Mode Setting

M1 [D5]	M0 [D4]	FUNCTION
0	0	CW mode
0	1	TGC mode I; high-performance mode, lowest noise
1	0	TGC mode II; lowest power mode
1	1	PW mode

Table 13. PGA Gain Setting

PG1 (D7)	PG0 (D6)	FUNCTION
0	0	Sets PGA gain to 20dB (default)
0	1	Sets PGA gain to 25dB
1	0	Sets PGA gain to 27dB
1	1	Sets PGA gain to 30dB

Table 14. CW Switch Matrix Control for Each Channel

DBn:4 (MSB)	DBn:3	DBn:2	DBn:1 (LSB)	LNA INPUT CHANNEL n DIRECTED TO
0	0	0	0	Output CW0
0	0	0	1	Output CW1
0	0	1	0	Output CW2
0	0	1	1	Output CW3
0	1	0	0	Output CW4
0	1	0	1	Output CW5
0	1	1	0	Output CW6
0	1	1	1	Output CW7
1	0	0	0	Output CW8
1	0	0	1	Output CW9
1	0	1	0	Connected to AVDD_5V
1	0	1	1	Connected to AVDD_5V
1	1	0	0	Connected to AVDD_5V
1	1	0	1	Connected to AVDD_5V
1	1	1	0	Connected to AVDD_5V
1	1	1	1	Connected to AVDD_5V

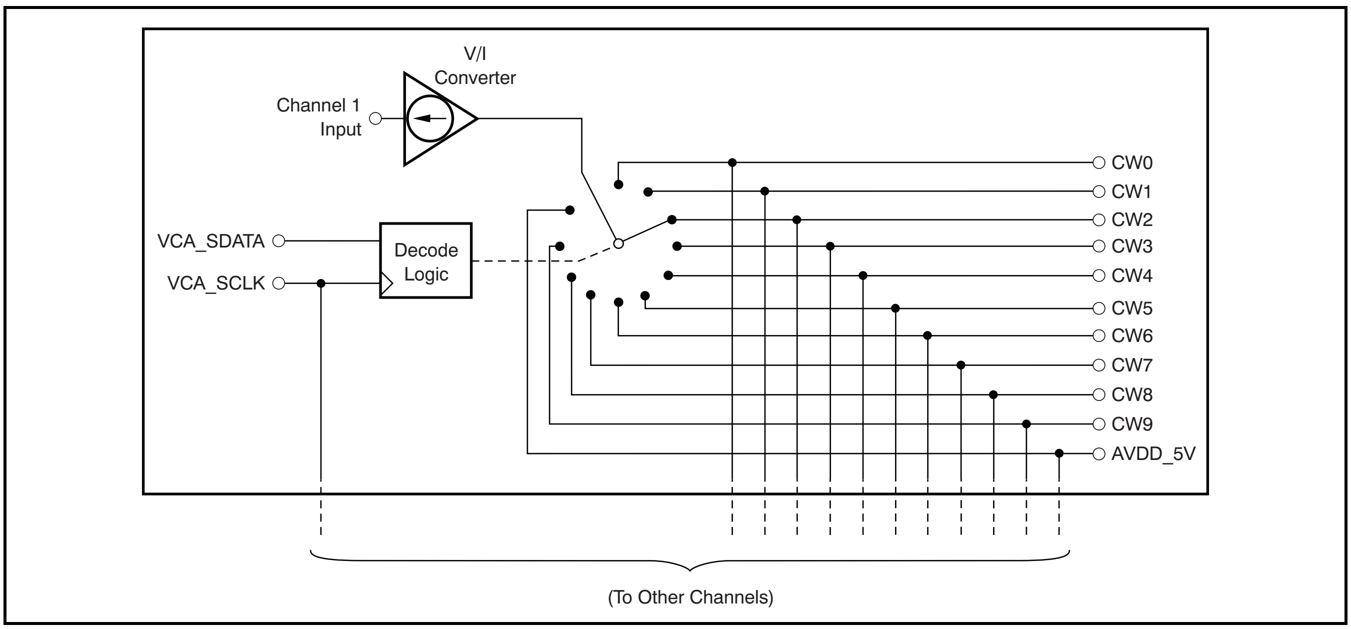


Figure 93. Basic CW Cross-Point Switch Matrix Configuration

POWER-DOWN MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F													X	X	X	X	PDN_CH<1:4>
									X	X	X	X					PDN_CH<8:5>
								X									PDN_PARTIAL
						0	X										PDN_COMPLETE
						X	0										PDN_PIN_CFG

Each of the eight ADC channels can be individually powered down. PDN_CH<N> controls the power-down mode for the ADC channel <N>.

In addition to channel-specific power-down, the AFE5804 also has two global power-down modes: partial power-down mode and complete power-down mode.

In addition to programming the device for either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits, respectively), the ADS_PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG = 0 (default), when the ADS_PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG = 1, when the ADS_PD pin is high, the device enters partial power-down mode.

The partial power-down mode function allows the AFE5804 to be rapidly placed in a low-power state. In this mode, most amplifiers in the signal path are powered down, while the internal references remain active. This configuration ensures that the external bypass capacitors retain the respective charges, minimizing the wake-up response time. The wake-up response is typically less than 50µs, provided that the clock has been running for at least 50µs before normal operating mode resumes. The power-down time is instantaneous (less than 1.0µs).

In partial power-down mode, the part typically dissipates only 95mW, representing a 76% power reduction compared to the normal operating mode. This function is controlled through the ADS_PD and VCA_PD pins, which are designed to interface with 3.3V low-voltage logic. If separate control of the two PD pins is not desired, then both can be tied together. In this case, the ADS_PD pin should be configured to operate as a partial power-down mode pin (see further information below).

For normal operation the PD pins should be tied to a logic low (0); a high (1) places the AFE5804 into partial power-down mode.

To achieve the lowest power dissipation of only 52mW, the AFE5804 can be placed in complete power-down mode. This mode is controlled through the serial interface by setting Register 16 (bit D2) and Register 0F (bit D9:D10). In complete power-down mode, all circuits (including references) within the AFE5804 are powered-down, and the bypass capacitors then discharge. Consequently, the wake-up time from complete power-down mode depends largely on the time needed to recharge the bypass capacitors. Another factor that affects the wake-up time is the elapsed time that the AFE5804 spends in shutdown mode.

LVDS DRIVE PROGRAMMABILITY

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
11														X	X	X	ILVDS_LCLK<2:0>
										X	X	X					ILVDS_FRAME<2:0>
						X	X	X									ILVDS_DAT<2:0>

The LVDS drive strength of the bit clock (LCLKP or LCLKM) and the frame clock (FCLKP or FCLKM) can be individually programmed. The LVDS drive strengths of all the data outputs OUTP and OUTM can also be programmed to the same value.

All three drive strengths (bit clock, frame clock, and data) are programmed using sets of three bits. Table 15 shows an example of how the drive strength of the bit clock is programmed (the method is similar for the frame clock and data drive strengths).

Table 15. Bit Clock Drive Strength(1)

ILVDS_LCLK<2>	ILVDS_LCLK<1>	ILVDS_LCLK<0>	LVDS DRIVE STRENGTH FOR LCLKP AND LCLKM
0	0	0	3.5mA (default)
0	0	1	2.5mA
0	1	0	1.5mA
0	1	1	0.5mA
1	0	0	7.5mA
1	0	1	6.5mA
1	1	0	5.5mA
1	1	1	4.5mA

(1) Current settings lower than 1.5mA are not recommended.

LVDS INTERNAL TERMINATION PROGRAMMING

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
12		X															EN_LVDS_TERM
		1												X	X	X	TERM_LCLK<2:0>
		1								X	X	X					TERM_FRAME<2:0>
		1				X	X	X									TERM_DAT<2:0>

The LVDS buffers have high-impedance current sources that drive the outputs. When driving traces with characteristic impedances that are not perfectly matched with the termination impedance on the receiver side, there may be reflections back to the LVDS output pins of the AFE5804 that cause degraded signal integrity. By enabling an internal termination (between the positive and negative outputs) for the LVDS buffers, the signal integrity can be significantly improved in such scenarios. To set the internal termination mode, the EN_LVDS_TERM bit should be set to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 16 shows an example of how the internal termination of the LVDS buffer driving the bit clock is programmed (the method is similar for the frame clock and data drive strengths). These termination values are only typical values and can vary by several percentages across temperature and from device to device.

Table 16. Bit Clock Internal Termination

TERM_LCLK<2>	TERM_LCLK<1>	TERM_LCLK<0>	INTERNAL TERMINATION BETWEEN LCLKP AND LCLKM (Ω)
0	0	0	None
0	0	1	260
0	1	0	150
0	1	1	94
1	0	0	125
1	0	1	80
1	1	0	66
1	1	1	55

LOW-FREQUENCY NOISE SUPPRESSION MODE

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14													X	X	X	X	LFNS_CH<1:4>
									X	X	X	X					LFNS_CH<8:5>

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5804 to approximately $f_S/2$, thereby moving the noise floor around dc to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel.

LVDS TEST PATTERNS

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<11:10>
													X	X			BITS_CUSTOM2<11:10>
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1<9:0>
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2<9:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The AFE5804 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. Setting EN_RAMP to '1' causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.

The device can also be programmed to output a constant code by setting SINGLE_CUSTOM_PAT to '1', and programming the desired code in BITS_CUSTOM1<11:0>. In this mode, BITS_CUSTOM<11:0> take the place of the 12-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to toggle between two consecutive codes by programming DUAL_CUSTOM_PAT to '1'. The two codes are represented by the contents of BITS_CUSTOM1<11:0> and BITS_CUSTOM2<11:0>.

In addition to custom patterns, the device may also be made to output two preset patterns:

1. **Deskew patten:** Set using PAT_DESKEW, this mode replaces the 12-bit ADC output D<11:0> with the *010101010101* word.
2. **Sync pattern:** Set using PAT_SYNC, the normal ADC word is replaced by a fixed *111111000000* word.

Note that only one of the above patterns should be active at any given instant.

PROGRAMMABLE GAIN

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH4<3:0>
									X	X	X	X					GAIN_CH3<3:0>
					X	X	X	X									GAIN_CH2<3:0>
	X	X	X	X													GAIN_CH1<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

The AFE5804, through its registers, allows for a digital gain to be programmed for each channel. This programmable gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain not only fills the output code range of the ADC, but also enhances the SNR of the device by using quantization information from some extra internal bits. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0dB to 12dB, as shown in Table 17.

Table 17. Gain Setting for Channel 1

GAIN_CH1<3>	GAIN_CH1<2>	GAIN_CH1<1>	GAIN_CH1<0>	CHANNEL 1 GAIN SETTING
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
0	0	1	1	3dB
0	1	0	0	4dB
0	1	0	1	5dB
0	1	1	0	6dB
0	1	1	1	7dB
1	0	0	0	8dB
1	0	0	1	9dB
1	0	1	0	10dB
1	0	1	1	11dB
1	1	0	0	12dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

CLOCK, REFERENCE, AND DATA OUTPUT MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42	1								1							X	DIFF_CLK
	1								1					X			EN_DCC
	1								1				X				EXT_REF_VCM
	1								1	X	X						PHASE_DDR<1:0>
46	1						1							X			BTC_MODE
	1						1						X				MSB_FIRST
	1						1					X					EN_SDR
	1		1				1					1					FALL_SDR

INPUT CLOCK

The AFE5804 is configured by default to operate with a single-ended input clock; CLKP is driven by a CMOS clock and CLKM is tied to '0'. However, by programming DIFF_CLK to '1', the device can be made to work with a differential input clock on CLKP and CLKM. Operating with a low-jitter differential clock generally provides better SNR performance, especially at input frequencies greater than 30MHz.

In cases where the duty cycle of the input clock falls outside the 45% to 55% range, it is recommended to enable an internal duty cycle correction circuit. Enable this circuit by setting the EN_DCC bit to '1'.

EXTERNAL REFERENCE

The AFE5804 can be made to operate in external reference mode by pulling the INT/$\overline{\text{EXT}}$ pin to '0'. In this mode, the REFT and REFB pins should be driven with voltage levels of 2.5V and 0.5V, respectively, and must have enough drive strength to drive the switched capacitance loading of the reference voltages by each ADC. The advantage of using the external reference mode is that multiple AFE5804 units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices. However, in applications that do not have an available high drive, differential external reference, the AFE5804 can still be driven with a single external reference voltage on the CM pin. When EXT_REF_VCM is set as '1' (and the INT/$\overline{\text{EXT}}$ pin is set to '0'), the CM pin is configured as an input pin, and the voltages on REFT and REFB are generated as shown in Equation 1 and Equation 2.

$$VREFT = 1.5V + \frac{V_{CM}}{1.5V} \quad (1)$$

$$VREFB = 1.5V - \frac{V_{CM}}{1.5V} \quad (2)$$

BIT CLOCK PROGRAMMABILITY

The output interface of the AFE5804 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. Figure 94 shows this default phase.

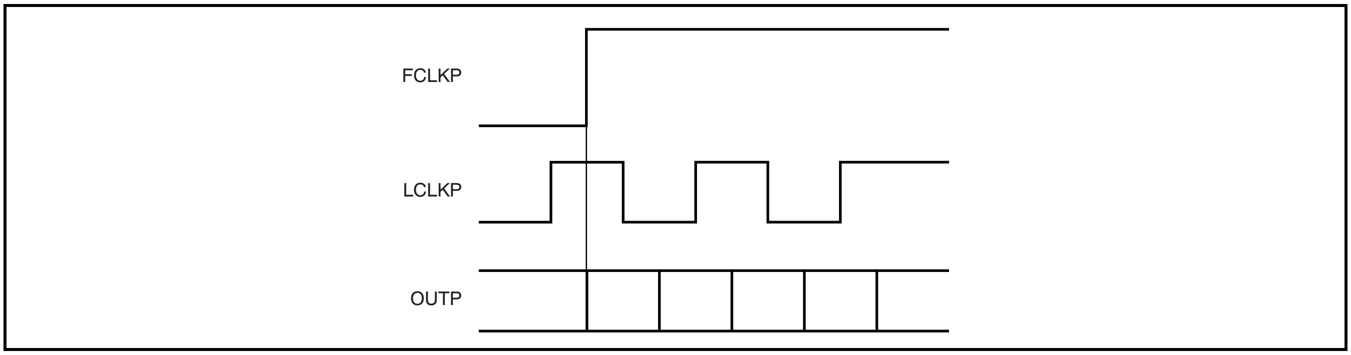


Figure 94. LCLK Default Phase

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. Figure 95 shows the LCLK phase modes.

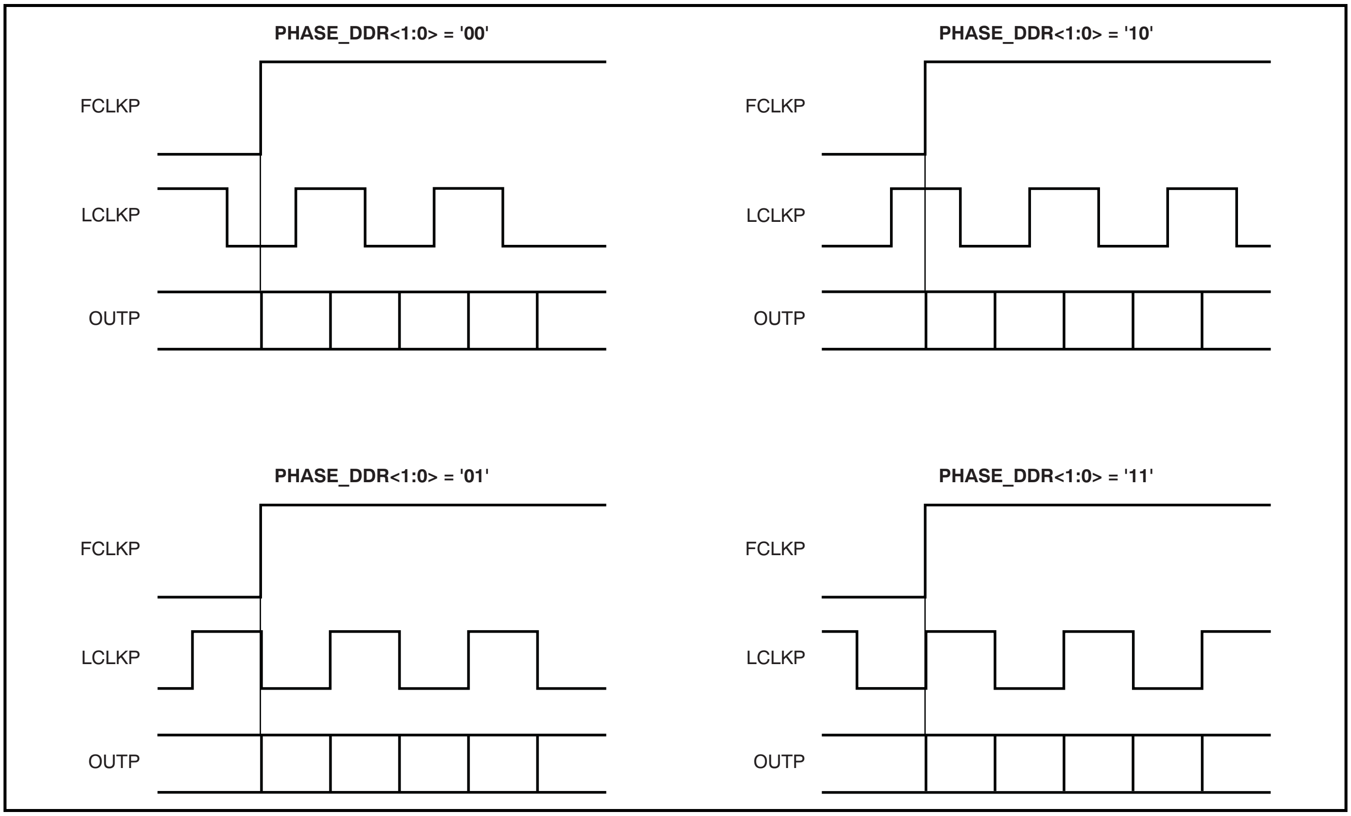


Figure 95. LCLK Phase Programmability Modes

In addition to programming the phase of LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting the EN_SDR bit to '1'. In this mode, the bit clock (LCLK) is output at 12 times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, LCLK may be output in either of the two manners shown in Figure 96. As Figure 96 illustrates, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode.

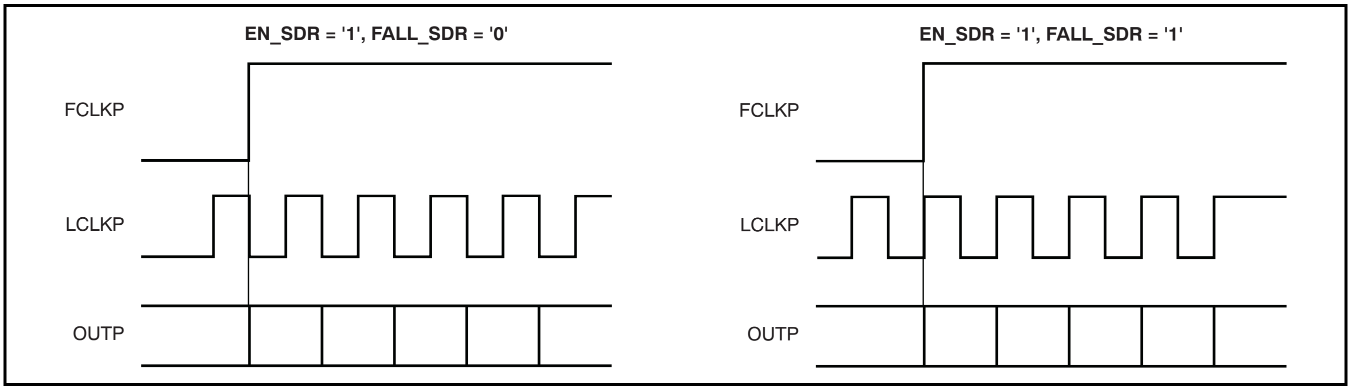


Figure 96. SDR Interface Modes

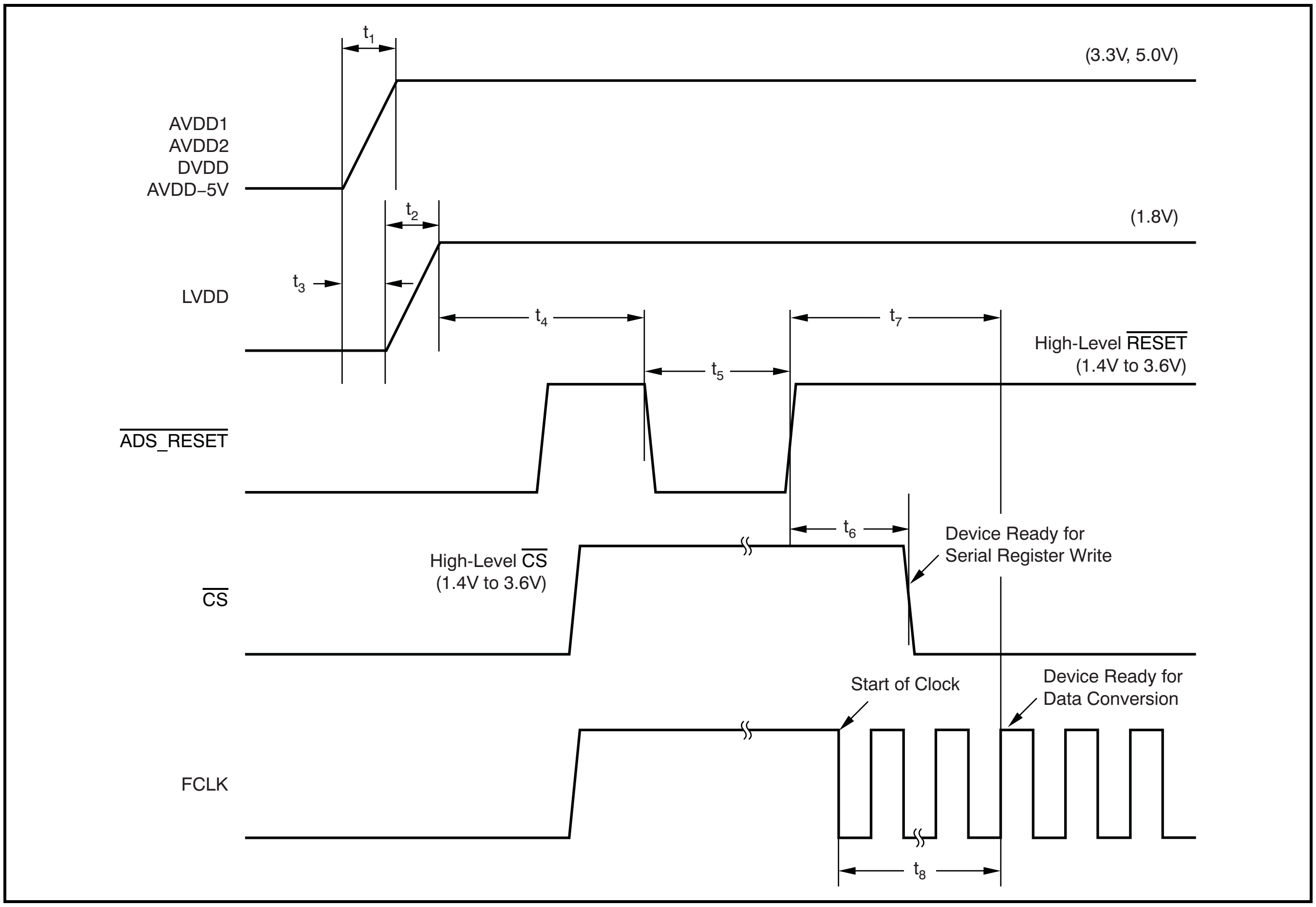
The SDR mode does not work well beyond 40MSPS because the LCLK frequency becomes very high.

DATA OUTPUT FORMAT MODES

The ADC output, by default, is in straight offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes binary twos complement mode.

Also by default, the first bit of the frame (following the rising edge of FCLKP) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following the FCLKP rising edge.

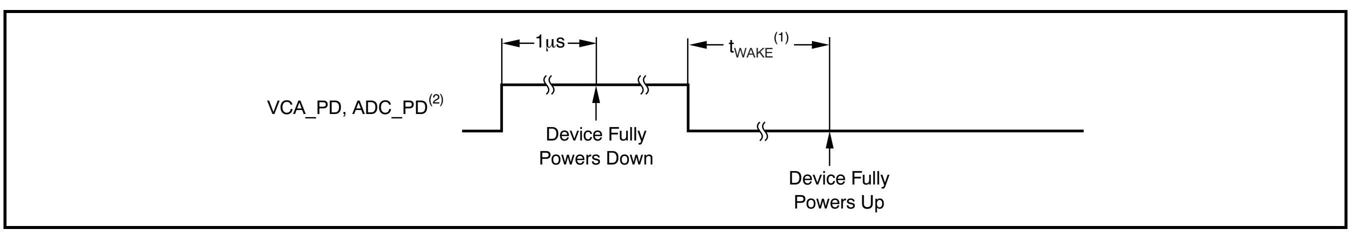
RECOMMENDED POWER-UP SEQUENCING AND RESET TIMING



10μs < t_1 < 50ms, 10μs < t_2 < 50ms, –10ms < t_3 < 10ms, t_4 > 10ms, t_5 > 100ns, t_6 > 100ns, t_7 > 10ms, and t_8 > 100μs.

(1) The AVDDx and LVDD power-on sequence does not matter as long as –10ms < t_3 < 10ms. Similar considerations apply while shutting down the device.

POWER-DOWN TIMING



Power-up time shown is based on 1μF bypass capacitors on the reference pins. t_{WAKE} is the time it takes for the device to wake up completely from power-down mode. The AFE5804 has two power-down modes: complete power-down mode and partial power-down mode.

(2) t_{WAKE} ≤ 50μs for complete power-down mode. t_{WAKE} ≤ 2μs for partial power-down mode (provided the clock is not shut off during power-down).

(3) The ADS_PD pins can be configured for partial power-down mode through a register setting.

THEORY OF OPERATION

The AFE5804 is an eight-channel, fully integrated analog front-end device. Its integrated LNA, attenuator, PGA, LPF, and ADC implement a number of proprietary circuit design techniques to specifically address the performance demands of medical ultrasound systems. It offers unparalleled low-noise and low-power performance at a high level of integration. For the TGC signal path, each channel consists of a 20dB fixed-gain low-noise amplifier (LNA), a linear-in-dB voltage-controlled attenuator (VCA), and a programmable gain amplifier (PGA), as well as a clamping and low-pass filter stage. Digitally-controlled through the logic interface, the PGA gain can be set to four different settings: 20dB, 25dB, 27dB, and 30dB. At its highest setting, the total available gain of the AFE5804 is therefore 50dB. To facilitate the logarithmic time-gain compensation required for ultrasound systems, the VCA is designed to provide a 46dB attenuation range. Here, all channels are simultaneously controlled by an externally-applied control voltage (V_{CNTL}) in the range of 0V to 1.2V. While the LNA is designed to be driven from a single-ended source, the internal TGC signal path is designed to be fully differential to maximize dynamic range while also optimizing for low, even-order harmonic distortion.

CW doppler signal processing is facilitated by routing the differential LNA outputs to V/I amplifier stages. The resulting signal currents of each channel then connect to an 8×10 switch matrix that is controlled through the serial interface and a corresponding register. The CW outputs are typically routed to a passive delay line that allows coherent summing (beam forming) of the active channels and additional off-chip signal processing, as shown in Figure 97.

Applications that do not utilize the CW path can simply operate the AFE5804 in TGC mode. In this mode, the CW blocks (V/I amplifiers and switch matrix) remain powered down, and the CW outputs can be left unconnected.

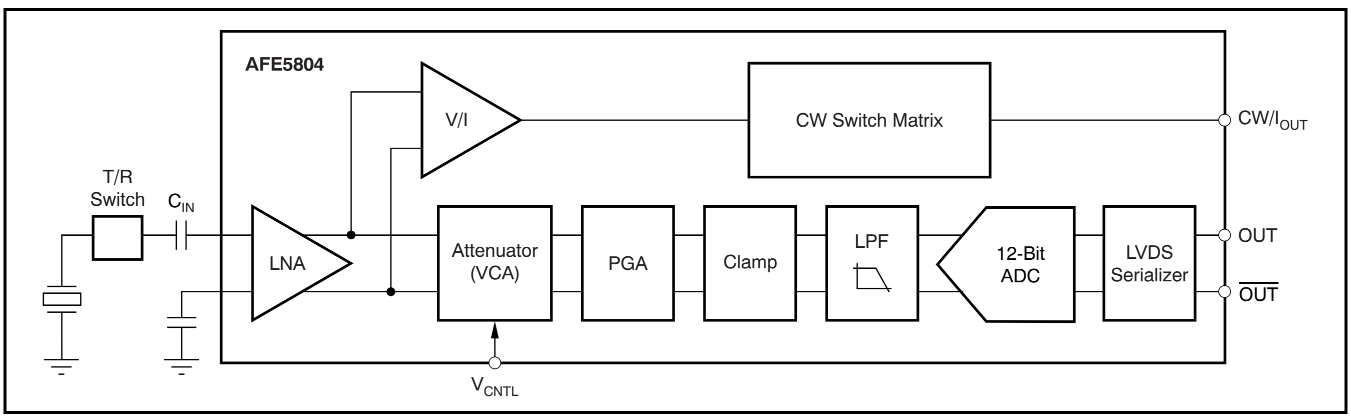


Figure 97. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

As with many high-gain systems, the front-end amplifier is critical to achieve a certain overall performance level. Using a proprietary new architecture, the LNA of the AFE5804 delivers exceptional low-noise performance, while operating on a very low quiescent current compared to CMOS-based architectures with similar noise performances.

The LNA performs a single-ended input to differential output voltage conversion and is configured for a fixed gain of 20dB (10V/V). The ultralow input-referred noise of only $0.75nV/\sqrt{Hz}$, along with the linear input range of $280mV_{PP}$, results in a wide dynamic range that supports the high demands of PW and CW ultrasound imaging modes. Larger input signals can be accepted by the LNA, but distortion performance degrades as input signals levels increase. The LNA input is internally biased to approximately 2.4V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor. Internally, the LNA directly drives the VCA, avoiding the typical drawbacks of ac-coupled architectures, such as slow overload recovery.

VOLTAGE-CONTROLLED ATTENUATOR (VCA)

The VCA is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB is constant for each equal increment of the control voltage (VCNTL). Figure 98 shows the simplified schematic of this VCA stage.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (R_S) and eight identical shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A8). Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V8 are equally spaced over the 0V to 1.2V control voltage range. As the control voltage rises through the input range of each clipping amplifier, the amplifier output rises from 0V (FET completely ON) to VCM – V_T (FET nearly OFF), where VCM is the common source voltage and V_T is the threshold voltage of the FET. As each FET approaches its off state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic.

Thus, low control voltages have most of the FETs turned on, producing maximum signal attenuation. Similarly, high control voltages turn the FETs off, leading to minimal signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network.

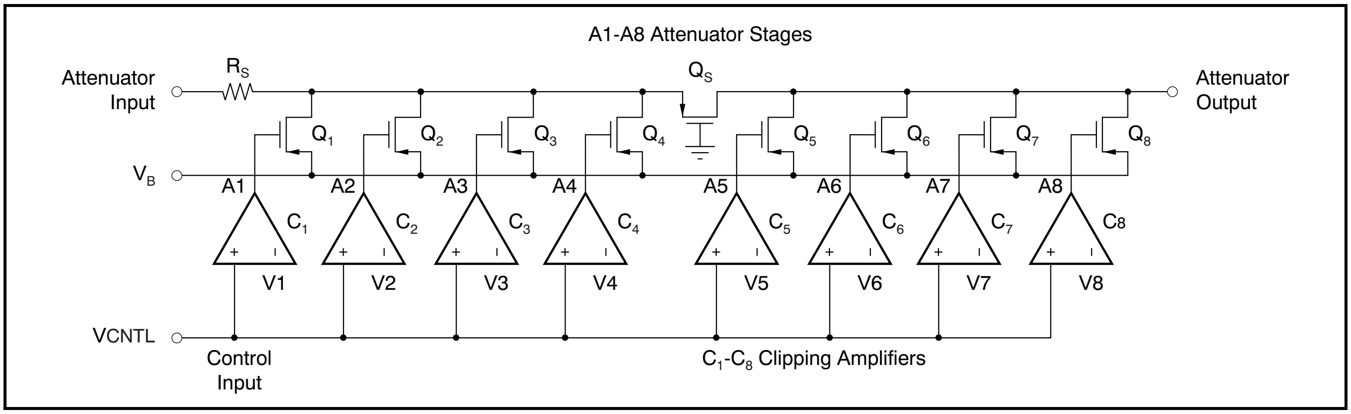


Figure 98. Voltage-Controlled Attenuator Simplified Schematic

PROGRAMMABLE POST-GAIN AMPLIFIER (PGA)

Following the VCA is a programmable post-gain amplifier (PGA). Figure 99 shows a simplified schematic of the PGA, including the clamping stage. The gain of this PGA can be configured to four different gain settings: 20dB, 25dB, 27dB, and 30dB, programmable through the serial port; see Table 11.

The PGA structure consists of a differential, programmable-gain voltage-to-current converter stage followed by transimpedance amplifiers to buffer each side of the differential output. Low input noise is also a requirement for the PGA design as a result of the large amount of signal attenuation that can be applied in the preceding VCA stage. At minimum VCA attenuation (used for small input signals), the LNA noise dominates; at maximum VCA attenuation (large input signals), the attenuator and PGA noise dominates.

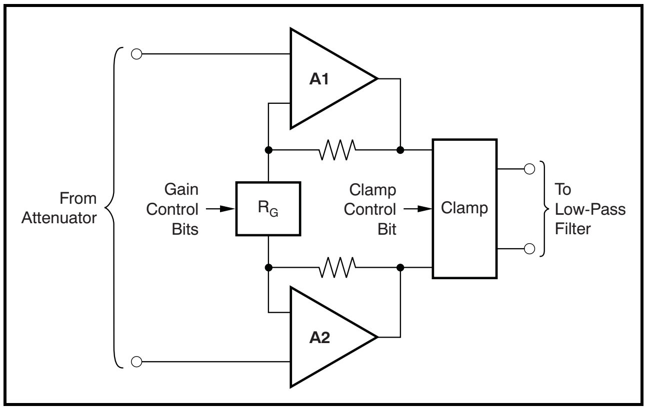


Figure 99. Post-Gain Amplifier (Simplified Schematic)

CLAMPING

To further optimize the overload recovery behavior of a complete TGC channel, the AFE5804 integrates a clamping stage, as shown in Figure 100. This clamping stage precedes the low-pass filter in order to prevent the filter circuit from being driven into overload, the result of which would be an extended recovery time. The clamping level is fixed to clamp the signal level to approximately 2.3V_{PP} differential.

LOW-PASS FILTER

The AFE5804 integrates an anti-aliasing filter in the form of a programmable low-pass filter (LPF) for each channel. The LPF is designed as a differential, active, second-order filter that approximates a Bessel characteristic, with typically 12dB per octave roll-off. Figure 100 shows the simplified schematic of half the differential active low-pass filter. Programmable through the serial interface, the –3dB frequency corner can be set to either 12.5MHz or 17MHz. The filter bandwidth is set for all channels simultaneously.

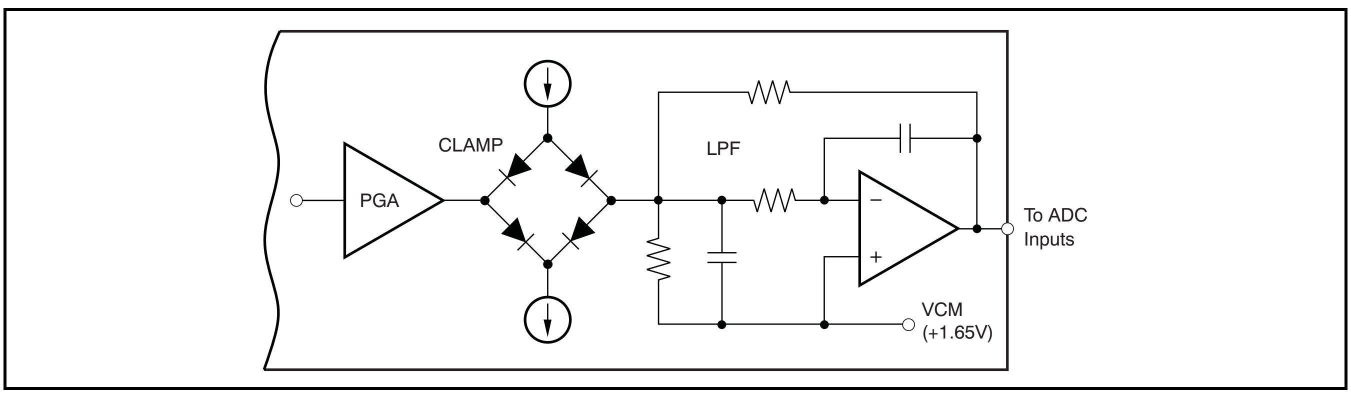


Figure 100. Clamping Stage and Low-Pass Filter (Simplified Schematic)

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital converter (ADC) of the AFE5804 employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level.

The 12 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5804 operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 12x clock required for the serializer is generated internally from CLKP/M using a phase-locked loop (PLL). A 6x and a 1x clock are also output in LVDS format, along with the data, to enable easy data capture. The AFE5804 operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices, and provide the option to operate the devices without having to externally drive and route reference lines. The nominal values of REFT and REFB are 2.5V and 0.5V, respectively. The references are internally scaled down differentially by a factor of 2. V_{CM} (the common-mode voltage of REFT and REFB) is also made available externally through a pin, and is nominally 1.5V.

The ADC output goes to a serializer that operates from a 12x clock generated by the PLL. The 12 data bits from each channel are serialized and sent LSB first. In addition to serializing the data, the serializer also generates a 1x clock and a 6x clock. These clocks are generated in the same way the serialized data are generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the AFE5804.

APPLICATION INFORMATION

ANALOG INPUT AND LNA

While the LNA is designed as a fully differential amplifier, it is optimized to perform a single-ended input to differential output conversion. A simplified schematic of an LNA channel is shown in Figure 101. A bias voltage (V_B) of +2.4V is internally applied to the LNA inputs through 8kΩ resistors. In addition, the dedicated signal input (IN pin) includes a pair of back-to-back diodes that provide a coarse input clamping function in case the input signal rises to very large levels, exceeding $0.6V_{PP}$. This configuration prevents the LNA from being driven into a severe overload state, which may otherwise cause an extended overload recovery time. The integrated diodes are designed to handle a dc current of up to approximately 5mA. Depending on the application requirements, the system overload characteristics may be improved by adding external Schottky diodes at the LNA input, as shown in Figure 101.

As Figure 101 also shows, the complementary LNA input (V_{BL} pin) is internally decoupled by a small capacitor. Furthermore, for each input channel, a separate V_{BL} pin is brought out for external bypassing. This bypassing should be done with a small, 0.1µF (typical) ceramic capacitor placed in close proximity to each V_{BL} pin. Attention should be given to provide a low-noise analog ground for this bypass capacitor. A noisy ground potential may cause noise to be picked up and injected into the signal path, leading to higher noise levels.

The LNA closed-loop architecture is internally compensated for maximum stability without the need for external compensation components (inductors or capacitors). At the same time, the total input capacitance is kept to a minimum with only 16pF. This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. Moreover, the closed-loop design yields very low offsets and offset drift; this consideration is important because the LNA directly drives the subsequent voltage-controlled attenuator.

The LNA of the AFE5804 uses the benefits of a bipolar process technology to achieve an exceptionally low noise voltage of $0.75nV/\sqrt{Hz}$, and a low current noise of only $3pA/\sqrt{Hz}$ (in TGC mode 1). With these input-referred noise specifications, the AFE5804 achieves very low noise figure numbers over a wide range of source resistances and frequencies (see the graph, *Noise Figure vs Frequency Over R_S* in the Typical Characteristics). The optimal noise power matching is achieved for source impedances of around 200Ω. Further details of the AFE5804 input noise performance are shown in the Typical Characteristic graphs.

Table 18. Noise Figure versus Source Resistance (R_S) at 2MHz

R_S (Ω)	NOISE FIGURE (dB)
50	2.1
200	1.1
400	1.2
1000	1.9

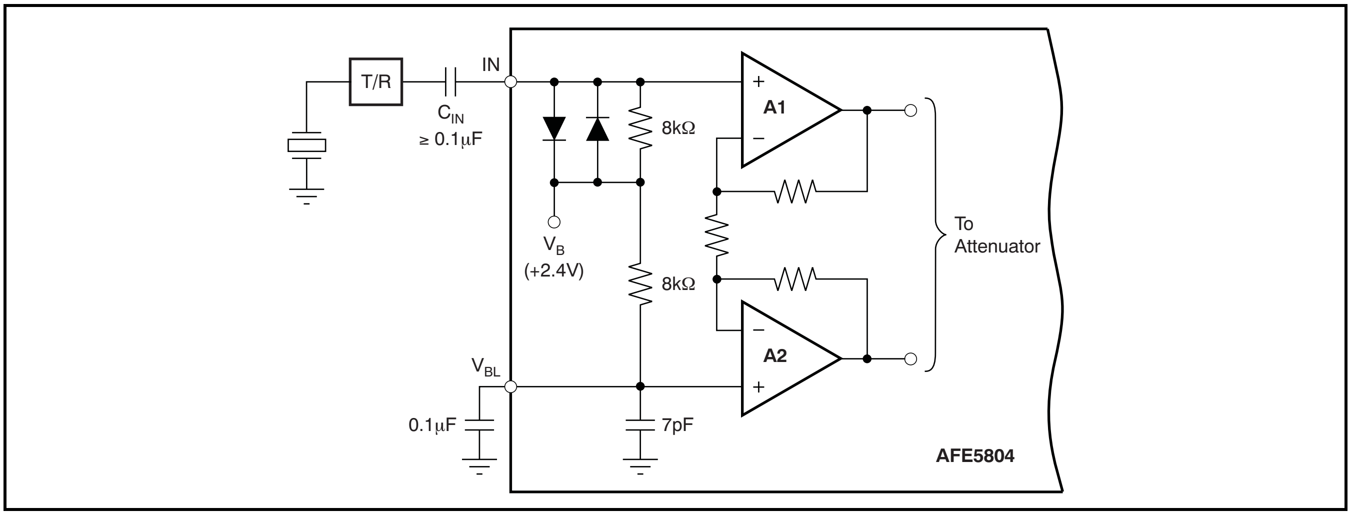


Figure 101. LNA Channel (Simplified Schematic)

OVERLOAD RECOVERY

The AFE5804 is designed in particular for ultrasound applications where the front-end device is required to recover very quickly from an overload condition. Such an overload can either be the result of a transmit pulse feedthrough or a strong echo, which can cause overload of the LNA, PGA, and ADC. As discussed earlier, the LNA inputs are internally protected by a pair of back-to-back diodes to prevent severe overload of the LNA. Figure 102 illustrates an ultrasound receive channel front-end that includes typical external overload protection elements. Here, four high-voltage switching diodes are configured in a bridge configuration and form the transmit/receive (T/R) switch. During the transmit period, high voltage pulses from the pulser are applied to the transducer elements and the T/R switch isolates the sensitive LNA input from being damaged by the high voltage signal. However, it is common that fast transients up to several volts leak through the T/R switch and potentially overload the receiver. Therefore, an additional pair of clamping diodes is placed between the T/R switch and the LNA input. In order to clamp the over-voltage to small levels, Schottky diodes (such as the BAS40 series by Infineon®) are commonly used. For example, clamping to levels of ±0.3V can significantly reduce the overall overload recovery performance. The T/R switch characteristics are largely determined by the biasing current of the diodes, which can be set by adjusting the 3kΩ resistor values; for example, setting a higher current level may lead to an improved switching characteristic and reduced noise contribution. A typical front-end protection circuitry may add in the order of $2nV/\sqrt{Hz}$ of noise to the signal path. The increase in noise also depends on the value of the termination resistor (R_T).

As Figure 102 shows, the front-end circuitry should be capacitively coupled to the LNA signal input (IN). This coupling ensures that the LNA input bias voltage of +2.4V is maintained and decoupled from any other biasing voltage before the LNA.

Within the AFE5804, overload can occur in either the LNA or the PGA. LNA overload can occur as the result of T/R switch feedthrough; and the PGA can be driven into an overload condition by a strong echo in the near-field while the signal gain is high. In any case, the AFE5804 is optimized for very short recovery times, as shown in Figure 102.

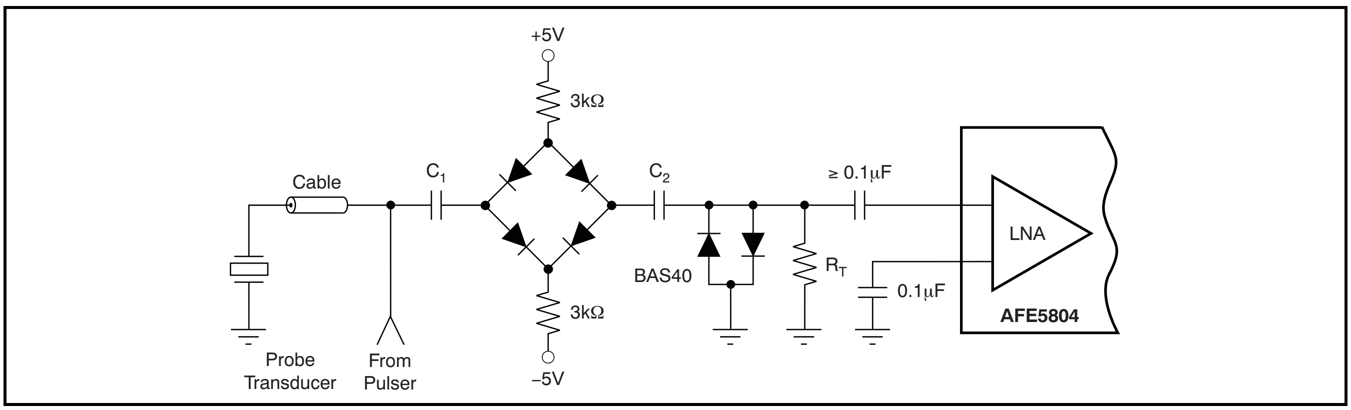


Figure 102. Typical Input Overload Protection Circuit of an Ultrasound System

VCA—GAIN CONTROL

The attenuator (VCA) for each of the eight channels of the AFE5804 is controlled by a single-ended control signal input, the V_{CNTL} pin. The control voltage range spans from 0V to 1.2V, referenced to ground. This control voltage varies the attenuation of the VCA based on its linear-in-dB characteristic with its maximum attenuation (minimum gain) at V_{CNTL} = 0V, and minimum attenuation (maximum gain) at V_{CNTL} = 1.2V. Table 19 shows the nominal gains for each of the four PGA gain settings. The total gain range is typically 46dB and remains constant independent of the PGA selected; the *Max Gain* column reflects the absolute gain of the full signal path comprised of the fixed LNA gain of 20dB and the programmable PGA gain.

Table 19. Nominal Gain Control Ranges for Each of the Four PGA Gain Settings

PGA GAIN	MIN GAIN AT V_{CNTL} = 0V	MAX GAIN AT V_{CNTL} = 1.2V
20dB	–5.5dB	40.5dB
25dB	–1.0dB	45.0dB
27dB	1.0dB	47.0dB
30dB	3.0dB	49.0dB

As previously discussed, the VCA architecture uses eight attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; gain ripple is typically less than ±0.5dB.

The AFE5804 gain-control input has a –3dB bandwidth of approximately 1.5MHz. This wide bandwidth, although useful in many applications, can allow high-frequency noise to modulate the gain control input. In practice, this modulation can easily be avoided by additional external filtering (R_F and C_F) of the control input, as Figure 103 shows. Stepping the control voltage from 0V to 1.2V, the gain control response time is typically less than 500ns to settle within 10% of the final signal level of a $1V_{PP}$ (–6dBFS) output.

The control voltage input (VCNTL pin) represents a high-impedance input. Multiple AFE5804 devices can be connected in parallel with no significant loading effects using the VCNTL pin of each device. Note that when the V_{CNTL} pin is left unconnected, it floats up to a potential of about +3.7V. For any voltage level above 1.2V and up to 5.0V, the VCA continues to operate at its minimum attenuation level; however, it is recommended to limit the voltage to approximately 1.5V or less.

When the AFE5804 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, it is recommended to set the V_{CNTL} voltage to +1.2V in order to minimize the internal loading of the LNA outputs. Small improvements in reduced power dissipation and improved distortion performance may also be realized.

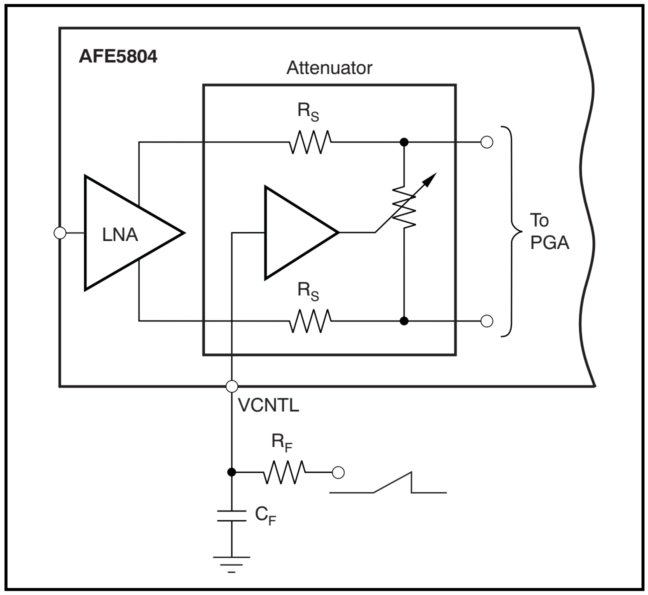


Figure 103. External Filtering of the V_{CNTL} Input

CW DOPPLER PROCESSING

The AFE5804 integrates many of the elements necessary to allow for the implementation of a CW doppler processing circuit, such as a V/I converter for each channel and a cross-point switch matrix with an 8-input into 10-output (8×10) configuration.

In order to switch the AFE5804 from the default TGC mode operation into CW mode, bit D5 of the control register must be updated to low ('0'). This setting also enables access to all other registers that determine the switch matrix configuration (see the Input Register Bit Map tables). In order to process CW signals, the LNA internally feeds into a differential V/I amplifier stage. The transconductance of the V/I amplifier is typically 13.5mA/V with a $100mV_{PP}$ input signal. For proper operation, the CW outputs must be connected to an external bias voltage of +2.5V. Each CW output is designed to sink a small dc current of 0.9mA, and can deliver a signal current up to $2.9mA_{PP}$.

The resulting signal current then passes through the 8×10 switch matrix. Depending on the programmed configuration of the switch matrix, any V/I amplifier current output can be connected to any of 10 CW outputs. This design is a simple current-summing circuit such that each CW output can represent the sum of any or all of the channel currents. The CW outputs are typically routed to a passive LC delay line, allowing coherent summing of the signals.

After summing, the CW signal path further consists of a high dynamic range mixer for down-conversion to I/Q base-band signals. The I/Q signals are then band-limited (that is, low-frequency contents are removed) in a filter stage that precedes a pair of high-resolution, low sample rate ADCs.

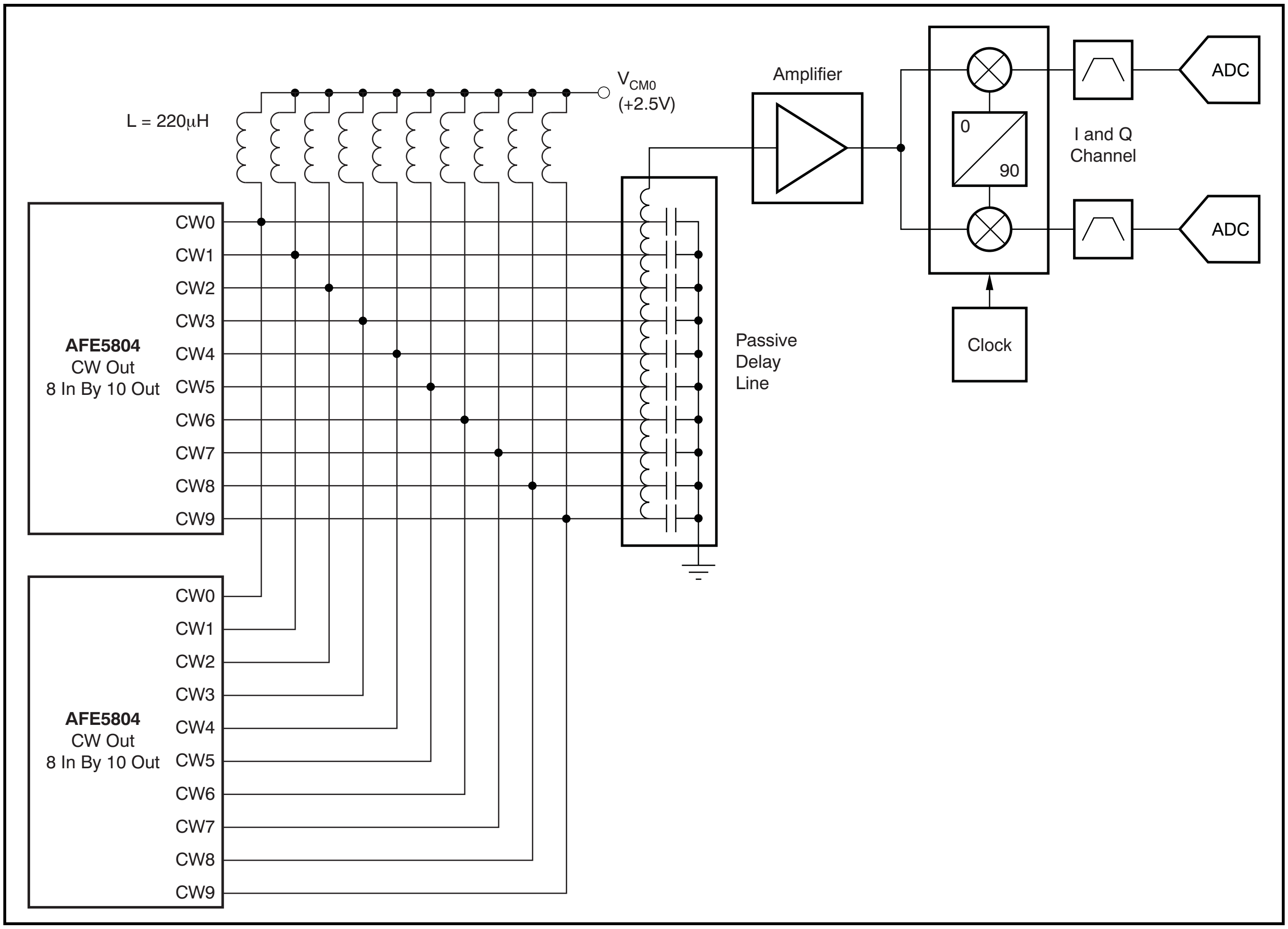


Figure 104. Conceptual CW Doppler Signal Path Using Current Summing and a Passive Delay Line for Beam-Forming

CLOCK INPUT

The eight channels on the device operate from a single clock input. To ensure that the aperture delay and jitter are the same for all channels, the AFE5804 uses a clock tree network to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point to the sampling circuit. This architecture ensures that the performance and timing for all channels are identical. The use of the clock tree for matching introduces an aperture delay that is defined as the delay between the rising edge of FCLK and the actual instant of sampling. The aperture delays for all the channels are matched to the best possible extent. A mismatch of ±20ps (±3σ) could exist between the aperture instants of the eight ADCs within the same chip. However, the aperture delays of ADCs across two different chips can be several hundred picoseconds apart.

The AFE5804 can operate either in CMOS single-ended clock mode (default is DIFF_CLK = 0) or differential clock mode (SINE, LVPECL, or LVDS). In the single-ended clock mode, CLKM must be forced to $0V_{DC}$, and the single-ended CMOS applied on the CLKP pin. Figure 105 shows this operation.

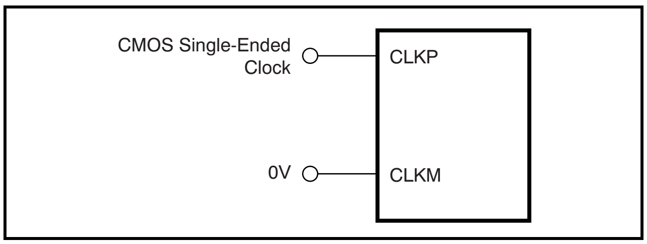


Figure 105. Single-Ended Clock Driving Circuit (DIFF_CLK = 0)

When configured for the differential clock mode (register bit DIFF_CLK = 1) the AFE5804 clock inputs can be driven differentially (SINE, LVPECL, or LVDS) with little or no difference in performance between them, or with a single-ended (LVCMOS). The common-mode voltage of the clock inputs is set to V_{CM} using internal 5kΩ resistors, as shown in Figure 106. This method allows using transformer-coupled drive circuits for a sine wave clock or ac-coupling for LVPECL and LVDS clock sources, as shown in Figure 107 and Figure 108. When operating in the differential clock mode, the single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1μF capacitor, as Figure 108 shows.

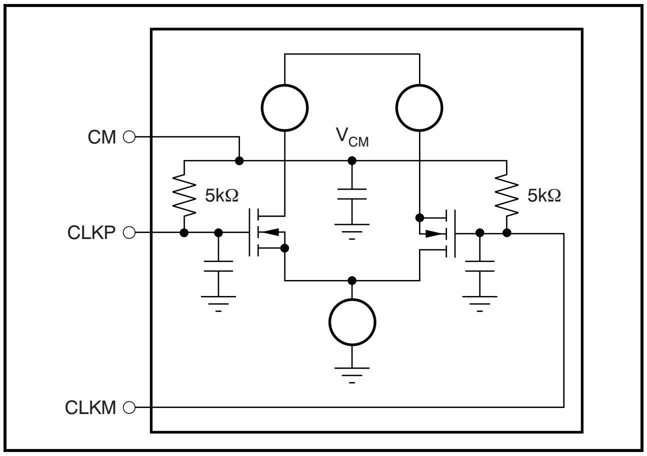


Figure 106. Internal Clock Buffer

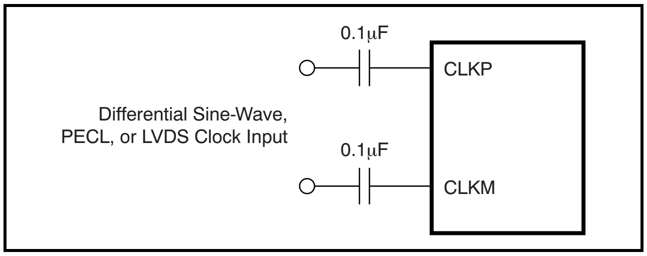


Figure 107. Differential Clock Driving Circuit (DIFF_CLK = 1)

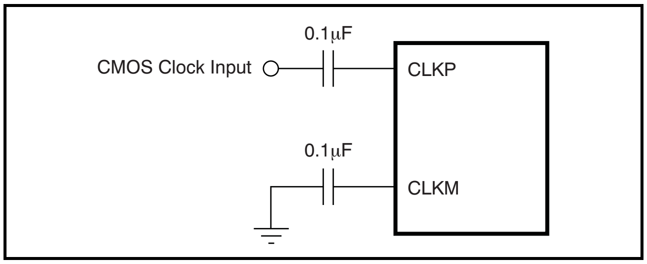


Figure 108. Single-Ended Clock Driving Circuit When DIFF_CLK = 1

For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. If the duty cycle deviates from 50% by more than 2% or 3%, it is recommended to enable the DCC through register bit EN_DCC.

REFERENCE CIRCUIT

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system has approximately 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at the ISET pin. Using a 56kΩ resistor on ISET generates an internal reference current of 20µA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external resistor at ISET reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56kΩ so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates the common-mode voltage V_{CM}, which is set to the midlevel of REFT and REFB. It is meant as a reference voltage to derive the input common-mode if the input is directly coupled. It can also be used to derive the reference common-mode voltage in the external reference mode. Figure 109 shows the suggested decoupling for the reference pins.

The device also supports the use of external reference voltages. There are two methods to force the references externally. The first method involves pulling INT/$\overline{\text{EXT}}$ low and forcing externally REFT and REFB to 2.5V and 0.5V nominally, respectively. In this mode, the internal reference buffer goes to a 3-state output. The external reference driving circuit should be designed to provide the required switching current for the eight ADCs inside the AFE5804. It should be noted that in this mode, CM and ISET continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM}.

The second method of forcing the reference voltages externally can be accessed by pulling INT/$\overline{\text{EXT}}$ low, and programming the serial interface to drive the external reference mode through the CM pin (register bit called EXT_REF_VCM). In this mode, CM becomes configured as an input pin that can be driven from external circuitry. The internal reference buffers driving REFT and REFB are active in this mode. Forcing 1.5V on the CM pin in the mode results in REFT and REFB coming to 2.5V and 0.5V, respectively. In general, the voltages on REFT and REFB in this mode are given by Equation 3 and Equation 4:

$$VREFT = 1.5V + \frac{V_{CM}}{1.5V} \tag{3}$$

$$VREFB = 1.5V - \frac{V_{CM}}{1.5V} \tag{4}$$

The state of the reference voltage internal buffers during various combinations of the PD, INT/$\overline{\text{EXT}}$, and EXT_REF_VCM register bits is described in Table 20.

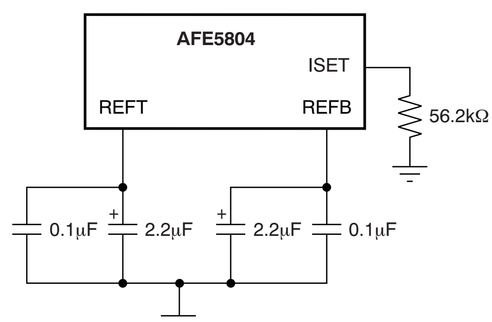


Figure 109. Suggested Decoupling on the Reference Pins

Table 20. State of Reference Voltages for Various Combinations of PD and INT/$\overline{EXT}$

REGISTER BIT	INTERNAL BUFFER STATE							
PD	0	0	1	1	0	0	1	1
INT/$\overline{EXT}$	0	1	0	1	0	1	0	1
EXT_REF_VCM	0	0	0	0	1	1	1	1
REFT buffer	3-state	2.5V	3-state	2.5V(1)	1.5V + V_{CM}/1.5V	Do not use	2.5V(1)	Do not use
REFB buffer	3-state	0.5V	3-state	0.5V(1)	1.5V – V_{CM}/1.5V	Do not use	0.5V(1)	Do not use
CM pin	1.5V	1.5V	1.5V	1.5V	Force	Do not use	Force	Do not use

(1) Weakly forced with reduced strength.

POWER SUPPLIES

The AFE5804 operates on three supply rails: a digital 1.8V supply, and the 3.3V and 5V analog supplies. At initial power-up, the part is operational in TGC mode, with the registers in the respective default configurations (see Table 3).

In TGC mode, only the VCA (attenuator) draws a low current (typically 7mA) from the 5V supply. Switching into the CW mode, the internal V/I-amplifiers are then powered from the 5V rail as well, raising the operating current on the 5V rail. At the same time, the post-gain amplifiers (PGA) are being powered down, thereby reducing the current consumption on the 3.3V rail (refer to the Electrical Characteristics table for details on TGC mode and CW mode current consumption).

All analog supply rails for the AFE5804 should be low noise, including the 3.3V digital supply DVDD that connects to the internal logic blocks of the VCA within the AFE5804. It is recommended to tie the DVDD pins to the same 3.3V analog supply as the AVDD1/2 pins, rather than a different 3.3V rail that may also provide power to other logic device in the system. Transients and noise generated by those devices can couple into the AFE5804 and degrade overall device performance.

CLOCK JITTER, POWER NOISE, SNR, AND LVDS TIMING

As explained in Application Note SLYT075, ADC clock jitter can degrade ADC performance. Therefore, it is always preferred to use a low jitter clock to drive the AFE5804. To ensure the performance of the AFE5804, a clock with a jitter of 1ps RMS or better is expected. However, it might not always be possible to achieve this for practical reasons. With a higher clock jitter, the SNR of the AFE5804 may be degraded as well as the LVDS timing stability. In addition, clean and stable power supplies are always preferred to maximize the AFE5804 SNR and ensure LVDS timing stability.

Poor RMS jitter (greater than 100ps), combined with inadequate power-supply design (for example, supply voltage drops and ripple increases), can affect LVDS timing. As a result, occasional glitches might be observed on the AFE5804 outputs. If this phenomenon is observed, or if the clock jitter and LVDD noise are concerns in the system, the registers in Table 21 can be written as part of the initialization sequence in order to stabilize LVDS clock timing and SNR performance.

Table 21. Address and Data in Hexadecimal

ADDRESS	DATA
01	0010h
D1	0140h
DA	0001h
E1	0020h
02	0080h
01	0000h

Writing to these registers has the following additional effects:

a. Total chip power increases approximately 8mW—this amount includes a current increase of about 1.9mA on AVDD1 and about 1.1mA on LVDD.
b. With reference to the LVDS Timing Diagram and Definition of Setup and Hold Times, LCLKP/LCLKM shift by about 100ps to the left relative to CLK and OUTP/OUTM. This shift causes the data setup time to reduce by 100ps and the data hold time to increase by 100ps.
c. The clock propagation delay (t_{PROP}) is reduced by roughly 2ns. The typical and minimum values for this specification are reduced by 2ns, and the maximum value for this spec is reduced by 1.5ns.

Power-supply noise can usually be minimized if grounding, bypassing, and PCB layout are well managed. Some guidelines can be found in the *Grounding and Bypassing* and *Board Layout* sections.

GROUNDING AND BYPASSING

The AFE5804 distinguishes between three different grounds: AVSS1 and AVSS2 (analog grounds), and LVSS (digital ground). In most cases, it should be adequate to lay out the printed circuit board (PCB) to use a single ground plane for the AFE5804. Care should be taken that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital (LVDS) supply set consisting of the LVDD and LVSS pins can be placed on separate power and ground planes. For this configuration, the AVSS and LVSS grounds should be tied together at the power connector in a star layout.

All bypassing and power supplies for the AFE5804 should be referenced to this analog ground plane. All supply pins should be bypassed with 0.1μF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2μF to 10μF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (less than 0.5in or 12,7mm) to the AFE5804 itself.

The AFE5804 internally generates a number of reference voltages, such as the bias voltages (VB1 through VB6). Note that in order to achieve optimal low-noise performance, the VB1 pin must be bypassed with a capacitor value of at least 1μF; the recommended value for this bypass capacitor is 2.2μF. All other designed reference pins can be bypassed with smaller capacitor values, typically 0.1μF. For best results choose low-inductance ceramic chip capacitors (size 402) and place them as close as possible to the device pins as possible.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the AFE5804, care has been taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. It is important to maintain low inductance properties throughout the design of the PCB layout by use of proper planes and layer thickness.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5804 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement.

In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design (for example, 100Ω differential). In addition, all LVDS trace lengths should be equal and symmetrical; it is recommended to keep trace length variations less than 150mil (0.150in or 3,81mm).

Additional details on PCB layout techniques can be found in the Texas Instruments Application Report *MicroStar BGA Packaging Reference Guide* (SSYZ015B), which can be downloaded from the TI web site (www.ti.com).

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2008) to Revision C **Page**

Changes from Revision A (September 2008) to Revision B **Page**

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE5804ZCF	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	AFE5804
AFE5804ZCF.A	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	AFE5804
AFE5804ZCF.B	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (10+1)	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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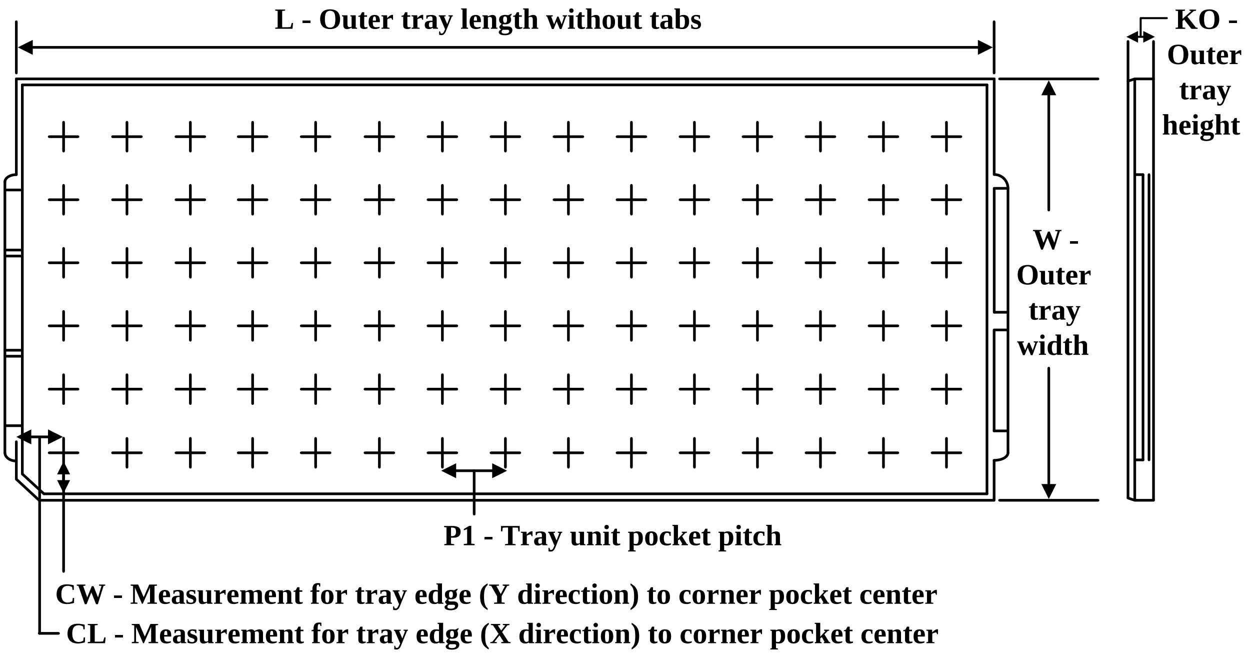
TRAY

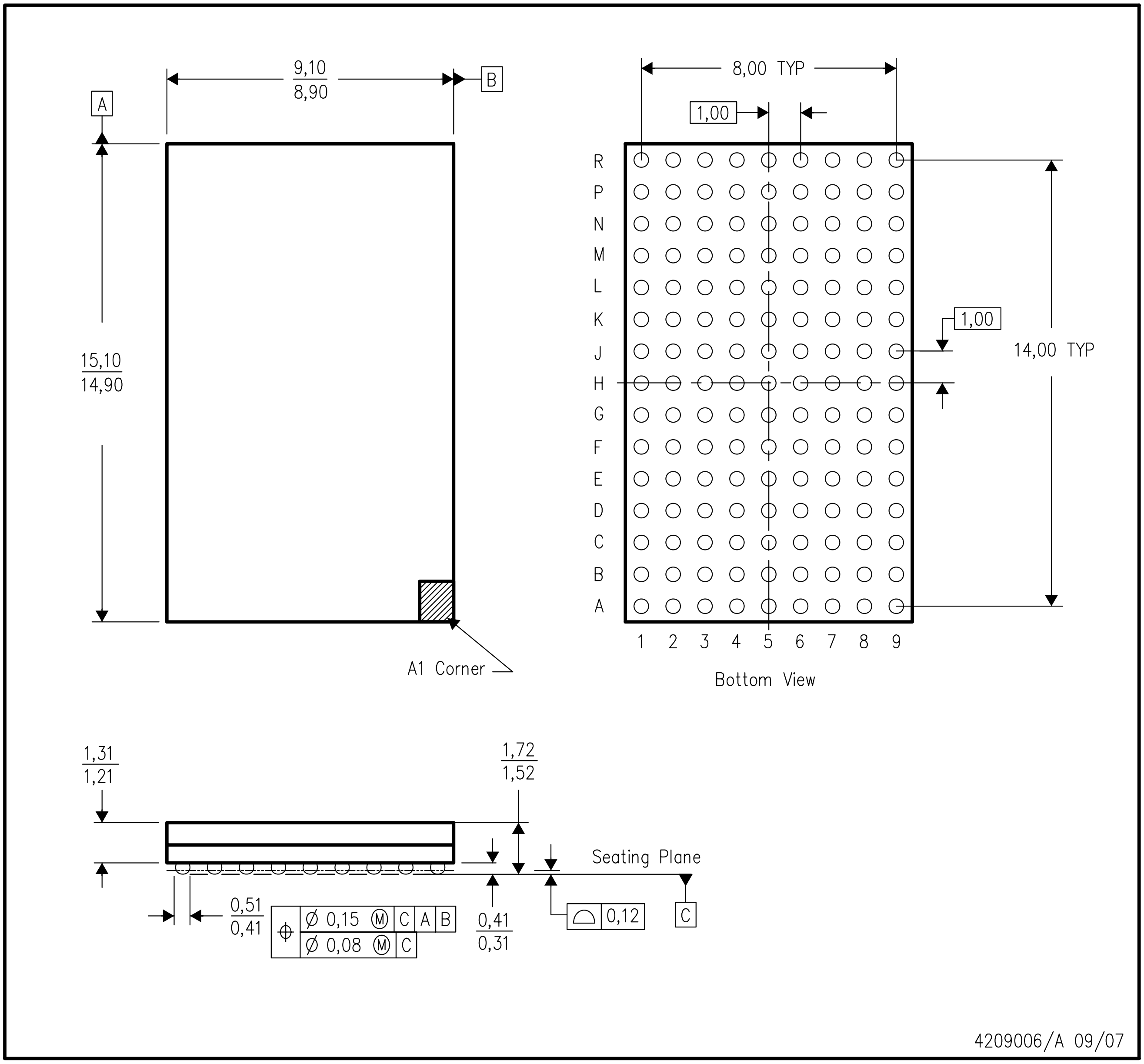


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE5804ZCF	ZCF	NFBGA	135	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35
AFE5804ZCF.A	ZCF	NFBGA	135	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35

ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.