

8-BIT MICROCONTROLLER***Table of Contents-***

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1. GENERAL DESCRIPTION

The W78L812 is an 8-bit microcontroller which can accommodate a wide range of supply voltages with low power consumption. The instruction set for the W78L812 is fully compatible with the standard 8051. The W78L812 contains an 8K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 5-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by a fourteen sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L812 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78L812 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

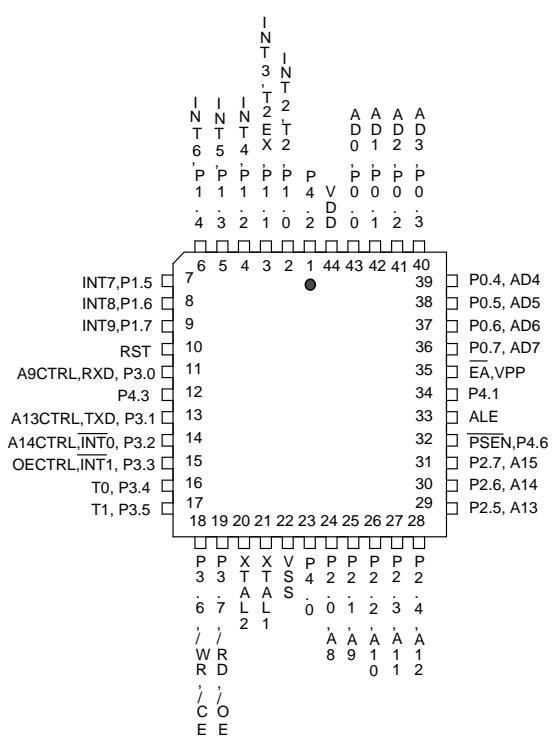
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 8 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- Three 16-bit timer/counters
- Timer 2 Clock-out
- One full duplex serial port (UART)
- Watchdog Timer
- Direct LED drive outputs
- Fourteen sources, two-level interrupt capability
- Wake-up via external interrupts at Port 1
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
 - Lead Free (RoHS) DIP 40: W78L812A24DL
 - Lead Free (RoHS) PLCC 44: W78L812A24PL
 - Lead Free (RoHS) PQFP 44: W78L812A24FL
 - Lead Free (RoHS) LQFP 48: W78L812A24LL

3. PIN CONFIGURATIONS

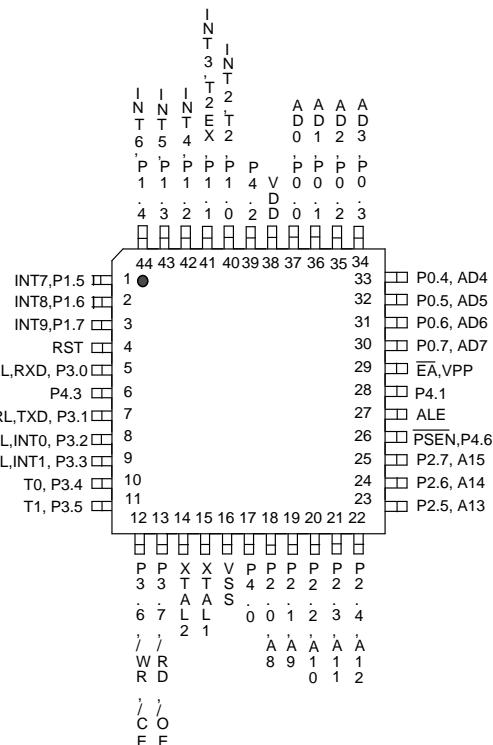
40-Pin DIP

| | | | | | |
|--------------------|--------------------------|----|----|--------------------------|-----------|
| INT2,,T2, P1.0 | <input type="checkbox"/> | 1 | 40 | <input type="checkbox"/> | VDD |
| INT3,T2EX, P1.1 | <input type="checkbox"/> | 2 | 39 | <input type="checkbox"/> | P0.0, AD0 |
| INT4,P1.2 | <input type="checkbox"/> | 3 | 38 | <input type="checkbox"/> | P0.1, AD1 |
| INT5,P1.3 | <input type="checkbox"/> | 4 | 37 | <input type="checkbox"/> | P0.2, AD2 |
| INT6,P1.4 | <input type="checkbox"/> | 5 | 36 | <input type="checkbox"/> | P0.3, AD3 |
| INT7,P1.5 | <input type="checkbox"/> | 6 | 35 | <input type="checkbox"/> | P0.4, AD4 |
| INT8,P1.6 | <input type="checkbox"/> | 7 | 34 | <input type="checkbox"/> | P0.5, AD5 |
| INT9,P1.7 | <input type="checkbox"/> | 8 | 33 | <input type="checkbox"/> | P0.6, AD6 |
| RST | <input type="checkbox"/> | 9 | 32 | <input type="checkbox"/> | P0.7, AD7 |
| A9CTRL,RXD, P3.0 | <input type="checkbox"/> | 10 | 31 | <input type="checkbox"/> | EA,VPP |
| A13CTR,LTXD, P3.1 | <input type="checkbox"/> | 11 | 30 | <input type="checkbox"/> | ALE |
| A14CTRL,INT0, P3.2 | <input type="checkbox"/> | 12 | 29 | <input type="checkbox"/> | PSEN,P4.6 |
| OECTRL,INT1, P3.3 | <input type="checkbox"/> | 13 | 28 | <input type="checkbox"/> | P2.7, A15 |
| T0, P3.4 | <input type="checkbox"/> | 14 | 27 | <input type="checkbox"/> | P2.6, A14 |
| T1, P3.5 | <input type="checkbox"/> | 15 | 26 | <input type="checkbox"/> | P2.5, A13 |
| <u>CE,WR, P3.6</u> | <input type="checkbox"/> | 16 | 25 | <input type="checkbox"/> | P2.4, A12 |
| <u>OE,RD, P3.7</u> | <input type="checkbox"/> | 17 | 24 | <input type="checkbox"/> | P2.3, A11 |
| XTAL2 | <input type="checkbox"/> | 18 | 23 | <input type="checkbox"/> | P2.2, A10 |
| XTAL1 | <input type="checkbox"/> | 19 | 22 | <input type="checkbox"/> | P2.1, A9 |
| VSS | <input type="checkbox"/> | 20 | 21 | <input type="checkbox"/> | P2.0, A8 |

44-Pin PLCC

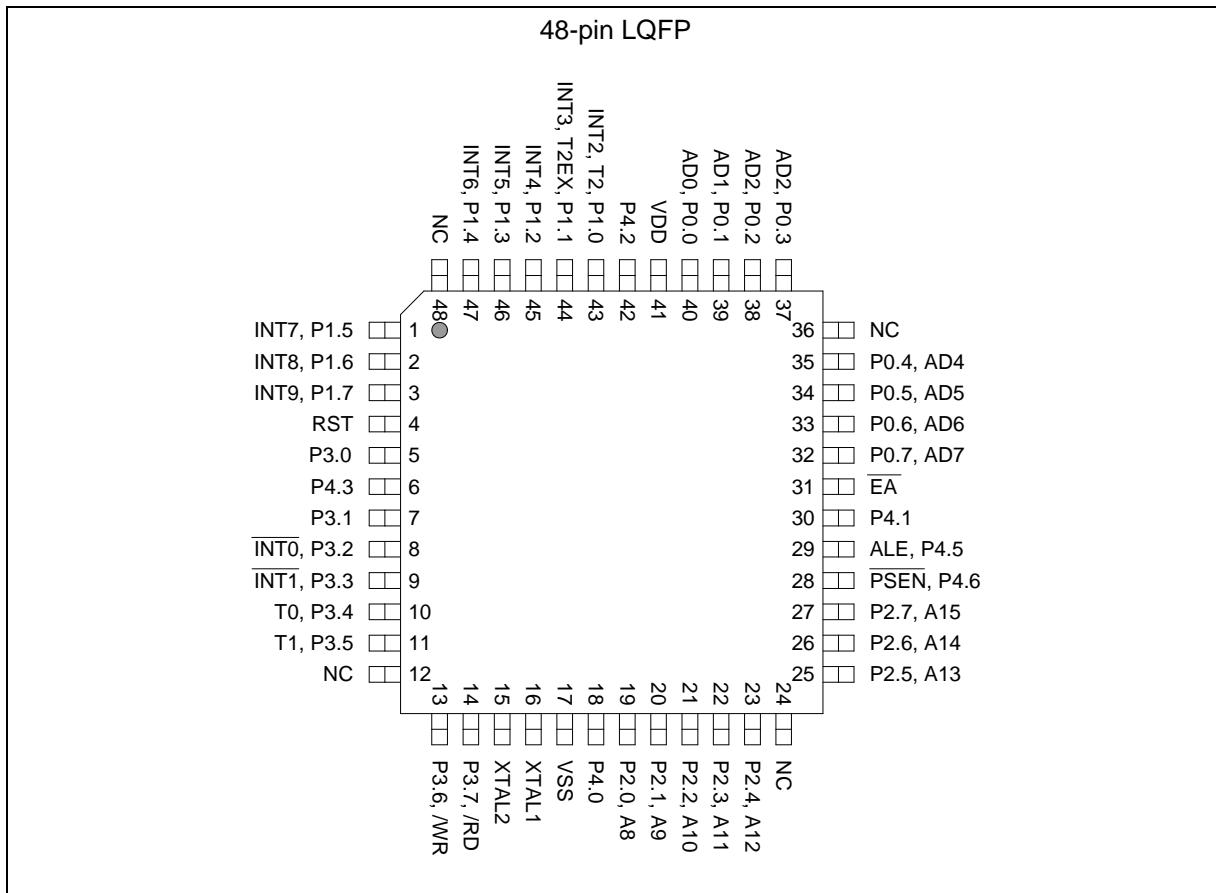


44-Pin PQFP



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4. PIN DESCRIPTION

| SYMBOL | DESCRIPTIONS |
|-------------|---|
| EA | EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if EA pin is high and the program counter is within on-chip ROM area. Otherwise they will be present on the bus. |
| PSEN | PROGRAM STORE ENABLE: PSEN enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no PSEN strobe signal outputs from this pin. This pin also serves the alternative function P4.6. |
| ALE | ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. |
| RST | RESET: A high on this pin for two machine cycles while the oscillator is running resets the device. |
| XTAL1 | CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock. |
| XTAL2 | CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. |
| VSS | GROUND: Ground potential |
| VDD | POWER SUPPLY: Supply voltage for operation. |
| P0.0 – P0.7 | PORT 0: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The pins of Port 0 can be individually configured to open-drain or standard port with internal pull-ups. |
| P1.0 – P1.7 | PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control INT2 – INT9 (P1.0 – P1.7): External interrupt 2 to 9 |
| P2.0 – P2.7 | PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. |
| P3.0 – P3.7 | PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. The pins P3.4 to P3.7 can be configured with high sink current which can drive LED displays directly. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port receiver input TXD(P3.1): Serial Port transmitter output INT0 (P3.2): External Interrupt 0 INT1(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input WR (P3.6): External Data Memory Write Strobe RD (P3.7): External Data Memory Read Strobe |
| P4.0 – P4.6 | PORT 4: A 5-bit bi-directional I/O port which is bit-addressable. Pins P4.0 to P4.3 are available on 44-pin PLCC/QFP package. P4.6 is the alternative function corresponding to PSEN. |

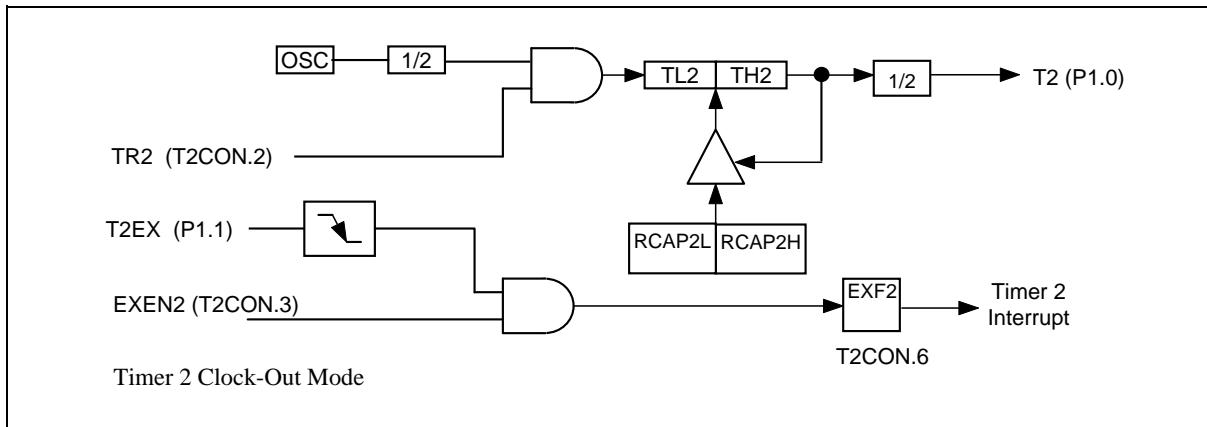
5. FUNCTIONAL DESCRIPTION

The W78L812 architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

5.1 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78L812: it is a 16-bit up/down counter that is configured and controlled by the T2CON and T2MOD registers. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1. In the auto-reload mode, Timer 2 performs a up counter which is similar with standard 8052. When counting up, an overflow in Timer 2 will cause a reload from RCAP2H and RCAP2L registers. The Timer 2 also provides a programmable clock-out mode as a clock generator. To enable this mode, timer 2 has to be configured with a 16-bit auto-reload timer (C/T2 = 0, CP/RL2 = 0) and bit T2OE (T2MOD.1) must be set to 1. This mode produces a 50% duty cycle clock output and timer 2 roll-overs will not generate an interrupt. The clock-out frequency depends on the oscillator frequency and the reload value of registers RCAP2H and RCAP2L. The clock-out frequency is determined by following equation:

$$\text{Clock-out Frequency} = \text{Oscillator Frequency} / [4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})]$$



5.2 Timer 2 Mode Control

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------|---|
| | - | - | - | - | - | - | T2OE | - |

Mnemonic: T2MOD Address: C9h

T2OE: Timer 2 Output Enable. This bit enables/disables the Timer 2 clock-out function.

5.3 I/O Port Options

The Port 0 and Port 3 of W78L812 may be configured with different types by setting the bits of the Port Options Register POR that is located at 86H. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the PUP bit in the POR register is set, the pins of Port 0 will perform a quasi-bi-directional I/O port with internal pull-up that is structurally the same as Port 2. The high nibble of Port 3 (P3.4 to P3.7) can be selected to serve the direct LED displays drive outputs by setting the HDx bit in the PO register. When the HDx bit is set, the corresponding pin P3.x can sink about 20mA current for driving LED display directly. After reset, the POR register is cleared and the pins of Ports 0 and 3 are the same as those of the standard 80C31. The POR register is shown below.

5.3.1 Port Options Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|---|---|-----|-----|-----|-----|-----|
| | EP6 | - | - | HD7 | HD6 | HD5 | HD4 | PUP |

Mnemonic: POR Address: 86H

PUP : Enable Port 0 weak pull-up.

HD4 – 7: Enable pins P3.4 to P3.7 individually with High Drive outputs.

EP6 : Enable P4.6. To set this bit shifts PSEN pin to the alternate function P4.6

5.4 Port 4

The W78L812 has one additional bit-addressable I/O port P4 in which the port address is D8H. The Port 4 contains seven bits; P4.0 to P4.3 are only available on 44-pin PLCC/QFP package; P4.6 is the alternate function corresponding to pin PSEN. When program is running in the internal memory without any access to external memory, PSEN may be individually configured to the alternate functions P4.6 that serve as general purpose I/O pins. To enable I/O port P4.6, the bit EP6 in the POR register must be set. During reset, the, PSEN perform as in the standard 80C32. The alternate functions P4.6 must be enabled by software. Care must be taken with the ALE pins when configured as the alternate functions.

5.4.1 Port 4

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|------|---|---|--------------|------|------|------|
| | - | P4.6 | - | - | P4.3 | P4.2 | P4.1 | P4.0 |
| Mnemonic: P4 | | | | | Address: D8H | | | |

5.5 Interrupt System

The W78L812 has fourteen interrupt sources: INT0 and INT1; Timer 0,1 and 2; Serial Port; INT2 to INT9. Each interrupt vectors to a specific location in program memory for its interrupt service routine. Each of these sources can be individually enabled or disabled by setting or clearing the corresponding bit in Special Function Register IE0 and IE1. The individual interrupt priority level depends on the Interrupt Priority Register IP0 and IP1. Additional external interrupts INT2 to INT9 are level sensitive and may be used to awake the device from power down mode. The Port 1 interrupts can be initialized to either active HIGH or LOW via setting the Interrupt Polarity Register IX. The IRQ register contains the flags of Port 1 interrupts. Each flag in IRQ register will be set when a interrupt request is recognized but must be cleared by software. Note that the interrupt flags have to be cleared before the interrupt service routine is completed, or else another interrupt will be generated.

5.5.1 Interrupt Enable Register 0

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|---|-----|----|-----|-----|-----|-----|
| | EA | - | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

Mnemonic: IE Address: A8H

EA : Global enable. Enable/disable all interrupts.

ET2: Enable Timer 2 interrupt.

ES : Enable Serial Port interrupt.

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

5.5.2 Interrupt Enable Register 1

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| | EX9 | EX8 | EX7 | EX6 | EX5 | EX4 | EX3 | EX2 |

EX9: Enable external interrupt 9

Note: 0 = interrupt disabled, 1 = interrupt enabled.

EX8: Enable external interrupt 8

EX7: Enable external interrupt 7

EX6: Enable external interrupt 6

EX5: Enable external interrupt 5

EX4: Enable external interrupt 4

EX3: Enable external interrupt 3

EX2: Enable external interrupt 2

5.5.3 Interrupt Priority Register 0

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|-----|----|-----|--------------|-----|-----|
| | - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
| | Mnemonic: IP0 | | | | | Address: B8h | | |

IP.7: Unused.

IP.6: Unused.

PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.

PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.

PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.

PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.

PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.

PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

5.5.4 Interrupt Priority Register 1

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----|-----|-----|-----|--------------|-----|-----|
| | PX9 | PX8 | PX7 | PX6 | PX5 | PX4 | PX3 | PX2 |
| | Mnemonic: IP1 | | | | | Address: F8h | | |

PX9: This bit defines the External interrupt 9 priority. PX9 = 1 sets it to higher priority level.

PX8: This bit defines the External interrupt 8 priority. PX8 = 1 sets it to higher priority level.

PX7: This bit defines the External interrupt 7 priority. PX7 = 1 sets it to higher priority level.

PX6: This bit defines the External interrupt 6 priority. PX6 = 1 sets it to higher priority level.

PX5: This bit defines the External interrupt 5 priority. PX5 = 1 sets it to higher priority level.

PX4: This bit defines the External interrupt 4 priority. PX4 = 1 sets it to higher priority level.

PX3: This bit defines the External interrupt 3 priority. PX3 = 1 sets it to higher priority level.

PX2: This bit defines the External interrupt 2 priority. PX2 = 1 sets it to higher priority level.

5.5.5 Interrupt Polarity Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|-----|-----|-----|-----|--------------|-----|-----|
| | IL9 | IL8 | IL7 | IL6 | IL5 | IL4 | IL3 | IL2 |
| | Mnemonic: IX | | | | | Address: E9H | | |

IL9: External interrupt 9 polarity level.

IL8: External interrupt 8 polarity level.

IL7: External interrupt 7 polarity level.

IL6: External interrupt 6 polarity level.

IL5: External interrupt 5 polarity level.

IL4: External interrupt 4 polarity level.

IL3: External interrupt 3 polarity level.

IL2: External interrupt 2 polarity level.

Note: 0 = active LOW, 1 = active HIGH.

5.5.6 Interrupt Request Flag Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| | IQ9 | IQ8 | IQ7 | IQ6 | IQ5 | IQ4 | IQ3 | IQ2 |

Mnemonic: IRQ

Address: C0H

IQ9: External interrupt 9 request flag.

IQ8: External interrupt 8 request flag.

IQ7: External interrupt 7 request flag.

IQ6: External interrupt 6 request flag.

IQ5: External interrupt 5 request flag.

IQ4: External interrupt 4 request flag.

IQ3: External interrupt 3 request flag.

IQ2: External interrupt 2 request flag.

Table.1 Priority level for simultaneous requests of the same priority interrupt sources

| SOURCE | FLAG | PRIORITY LEVEL | VECTOR ADDRESS |
|----------------------|------------|----------------|----------------|
| External Interrupt 0 | IE0 | (Highest) | 0003H |
| Serial Port | RI + TI | | 0023H |
| External Interrupt 5 | IQ5 | | 0053H |
| Timer 0 Overflow | TF0 | | 000BH |
| External Interrupt 6 | IQ6 | | 005BH |
| External Interrupt 1 | IE1 | | 0013H |
| External Interrupt 2 | IQ2 | | 003BH |
| External Interrupt 7 | IQ7 | | 0063H |
| Timer 1 Overflow | TF1 | | 001BH |
| Timer 2 Overflow | TF2 + EXF2 | | 002BH |
| External Interrupt 3 | IQ3 | | 0043H |
| External Interrupt 8 | IQ8 | | 006BH |
| External Interrupt 4 | IQ4 | | 004BH |
| External Interrupt 9 | IQ9 | (Lowest) | 0073H |

5.6 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will be disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

5.6.1 Watchdog Timer Control Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|------|------|---|---|-----|-----|-----|
| | ENW | CLRW | WIDL | - | - | PS2 | PS1 | PS0 |

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

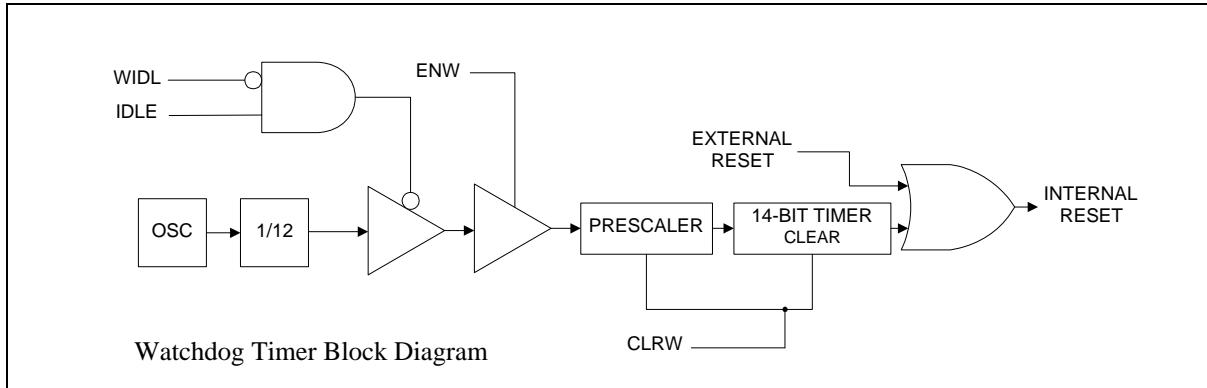
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2 – 0 as follows:

| PS2 | PS1 | PS0 | PRESCALER SELECT |
|-----|-----|-----|------------------|
| 0 | 0 | 0 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 0 | 1 | 8 |
| 0 | 1 | 1 | 16 |
| 1 | 0 | 0 | 32 |
| 1 | 0 | 1 | 64 |
| 1 | 1 | 0 | 128 |
| 1 | 1 | 1 | 256 |

The time-out period is obtained using the following equation:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Typical Watch-Dog time-out period when OSC = 20 MHz

| PS2 PS1 PS0 | WATCHDOG TIME-OUT PERIOD |
|-------------|--------------------------|
| 0 0 0 | 19.66 mS |
| 0 1 0 | 39.32 mS |
| 0 0 1 | 78.64 mS |
| 0 1 1 | 157.28 mS |
| 1 0 0 | 314.57 mS |
| 1 0 1 | 629.14 mS |
| 1 1 0 | 1.25 S |
| 1 1 1 | 2.50 S |

5.7 Clock

The W78L812 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L812 relatively insensitive to duty cycle variations in the clock. The W78L812 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

5.8 Power Management

5.8.1 Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

5.8.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator.

5.9 AUXR - Auxiliary Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|----|
| | - | - | - | - | - | - | - | AO |

Mnemonic: AUXR Address: 8Eh

AO: Turn off ALE signal.

5.10 Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

5.11 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L812 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6. ON-CHIP ROM CHARACTERISTICS

The W78L812 has several modes to program the on-chip ROM. All these operations are configured by the pins RST, ALE, PSEN, A9CTRL (P3.0), A13CTRL (P3.1), A14CTRL (P3.2), OECTRL (P3.3), \overline{CE} (P3.6), \overline{OE} (P3.7), A0 (P1.0) and VPP (\overline{EA}). Moreover, the A15 – A0 (P2.7 – P2.0, P1.7 – P1.0) and the D7 – D0 (P0.7 – P0.0) serve as the address and data bus respectively for these operations.

6.1 Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

6.2 Output Disable Condition

When the \overline{OE} is set to high, no data output appears on the D7... D0.

6.3 Program Operation

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the VPP is reach to VCP (12.5V) level, \overline{CE} set to low, and \overline{OE} set to high.

6.4 Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

6.5 Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the VPP is reach to VEP level, \overline{CE} set to low, and \overline{OE} set to high.

6.6 Erase Verify Operation

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if VPP = VEP (14.5V), \overline{CE} is high and \overline{OE} is low.

6.7 Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When P3.6 (\overline{CE}) = VIH, P3.7 (\overline{OE}) = VIH, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

| OPERATIONS | P3.0 (A9 CTRL) | P3.1 (A13 CTRL) | P3.2 (A14 CTRL) | P3.3 (OE CTRL) | P3.6 (\overline{CE}) | P3.7 (\overline{OE}) | \overline{EA} (VPP) | P2, P1 (A15... A0) | P0 (D7... D0) | NOTES |
|---------------------------|----------------------|-----------------------|-----------------------|----------------------|-----------------------------|-----------------------------|--------------------------|-----------------------|------------------|-------|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address | Data Out | |
| Output Disable | 0 | 0 | 0 | 0 | 0 | 1 | 1 | X | Hi-Z | |
| Program | 0 | 0 | 0 | 0 | 0 | 1 | VCP | Address | Data In | |
| Program Verify | 0 | 0 | 0 | 0 | 1 | 0 | VCP | Address | Data Out | @3 |
| Erase | 1 | 0 | 0 | 0 | 0 | 1 | VEP | A0:0, others: X | Data In 0FFH | @4 |
| Erase Verify | 1 | 0 | 0 | 0 | 1 | 0 | VEP | Address | Data Out | @5 |
| Program/ Erase Inhibit | X | 0 | 0 | 0 | 1 | 1 | VCP/ VEP | X | X | |

Notes:

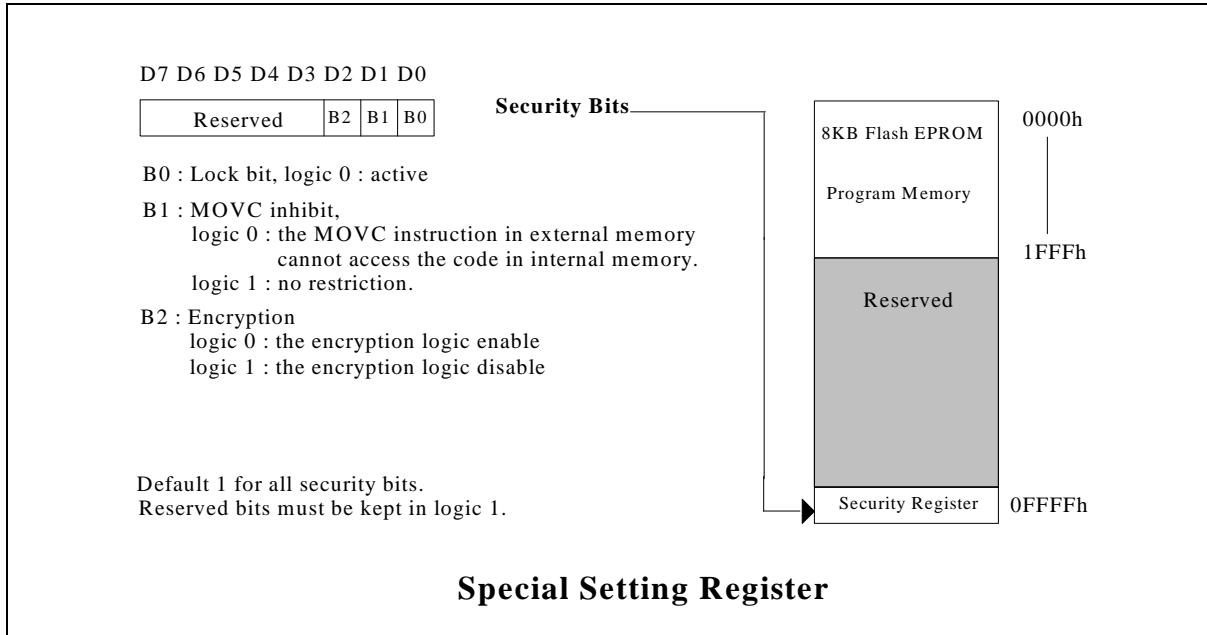
1. All these operations happen in RST = VIH, ALE = VIL and \overline{PSEN} = VIH.
2. VCP = 12.5V, VEP = 14.5V, VIH = VDD, VIL = VSS.
3. The program verify operation follows behind the program operation.
4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
5. The erase verify operation follows behind the erase operation.

6.8 Security Bits

During the programmer operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78L812 has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The register can only be accessed from the on-chip ROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation.

The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



6.8.1 Lock Bit

This bit is used to protect the customer's program code in the W78L812. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the on-chip ROM data and Special Setting Registers can not be accessed again.

6.8.2 MOVC Inhibit

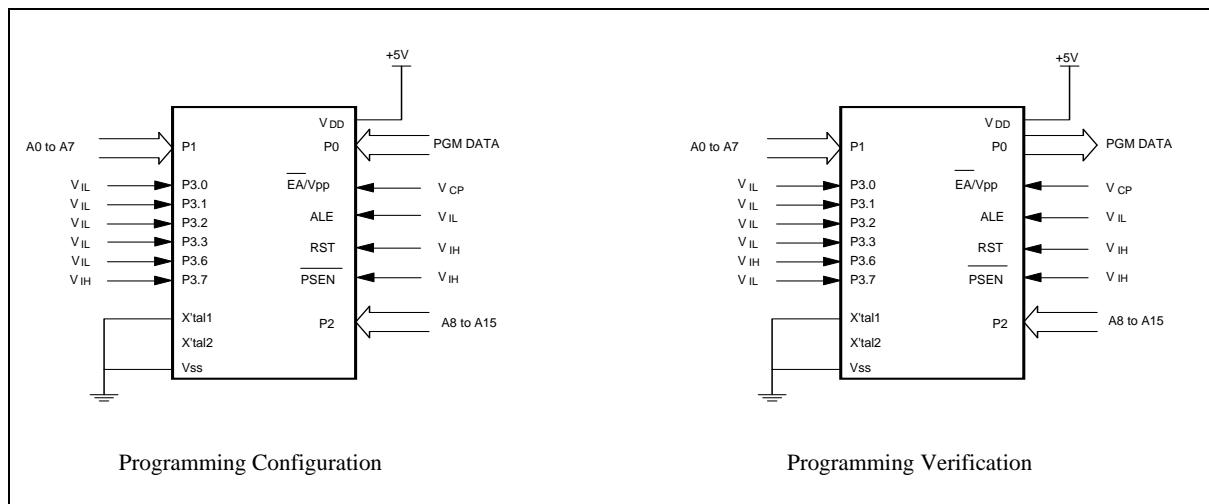
This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

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6.8.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



7. ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|-----------------------|-----------------|----------|----------|------|
| DC Power Supply | VDD – Vss | -0.3 | +7.0 | V |
| Input Voltage | VIN | Vss -0.3 | VDD +0.3 | V |
| Operating Temperature | T _a | 0 | 70 | °C |
| Storage Temperature | T _{ST} | -55 | +150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. DC CHARACTERISTICS

VSS = 0V, TA = 25° C, unless otherwise specified.

| PARAMETER | SYM. | SPECIFICATION | | | TEST CONDITIONS |
|--|-------------------|---------------|----------|------|--------------------------------------|
| | | MIN. | MAX. | UNIT | |
| Operating Voltage | VDD | 2.4 | 5.5 | V | |
| Operating Current | IDD | - | 20 | mA | VDD = 5.5V, 20 MHz, no load, RST = 1 |
| | | - | 3 | mA | VDD = 2.4V, 12 MHz, no load, RST = 1 |
| Idle Current | I _{IDLE} | - | 7 | mA | VDD = 5.5V, 20 MHz, no load |
| | | - | 1.5 | mA | VDD = 2.4V, 12 MHz, no load |
| Power Down Current | I _{PWDN} | - | 50 | μA | VDD = 5.5V, no load |
| | | - | 30 | μA | VDD = 2.4V, no load |
| Input | | | | | |
| Input Current P1, P2, P3, P4 | I _{IN} | -50 | +10 | μA | VDD = 5.5V VIN = 0V or VDD |
| Input Leakage Current P0, \overline{EA} | I _{ILK} | -10 | +10 | μA | VDD = 5.5V VSS < VIN < VDD |
| Input Current RST | I _{IN2} | -10 | +0 | μA | VDD = 5.5V 0 < VIN < VDD |
| Input Leakage Current P0, \overline{EA} | I _{ILK1} | -60 | +300 | μA | VDD = 5.5V 0V < VIN < VDD |
| Logic 1-to-0 Transition Current P1, P2, P3, P4 | | -500 | - | μA | VDD = 5.5V VIN = 2V |
| Input Low Voltage P1, P2, P3, P4 | | 0 | 0.8 | V | VDD = 5.5V |
| Input Low Voltage | | 0 | 0.5 | V | VDD = 2.4V |
| RST ^[*3] | | 0 | 0.8 | V | VDD = 5.5V |
| Input Low Voltage XTAL1 ^[*3] | V _{IL3} | 0 | 0.8 | | VDD = 5.5V |
| | | 0 | 0.6 | V | VDD = 2.4V |
| Input High Voltage P1, P2, P3, P4, \overline{EA} | V _{IH1} | 3.5 | VDD +0.2 | V | VDD = 5.5V |
| | | 1.6 | VDD +0.2 | V | VDD = 2.4V |
| Input High Voltage RST | V _{IH2} | 3.5 | VDD +0.2 | V | VDD = 5.5V |
| | | 1.7 | VDD +0.2 | V | VDD = 2.4V |
| Input High Voltage XTAL1 ^[*4] | V _{IH3} | 3.5 | VDD +0.2 | V | VDD = 5.5V |
| | | 1.6 | VDD +0.2 | V | VDD = 2.4V |

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DC Characteristics, continued

| PARAMETER | SYM. | SPECIFICATION | | | TEST CONDITIONS |
|---|------|---------------|------|------|---------------------------|
| | | MIN. | MAX. | UNIT | |
| Output | | | | | |
| Output Low Voltage P1, P2, P3, P4 | VOL1 | - | 0.45 | V | VDD = 4.5V, IOL = +2 mA |
| | | - | 0.25 | V | VDD = 2.4V, IOL = +1 mA |
| Output Low Voltage P0, ALE, <u>PSEN</u> ^[*4] | VOL2 | - | 0.45 | V | VDD = 4.5V, IOL = +4 mA |
| | | - | 0.25 | V | VDD = 2.4V, IOL = +2 mA |
| Output Low Voltage P3 ^[*6] | VOL3 | - | 0.22 | V | VDD = 4.5V, IOL = +2 mA |
| Sink current P1, P2, P3 ^[5] , P4<0:4> | ISK1 | 4 | 12 | mA | VDD = 4.5V, VOL = 0.45V |
| | | 1.8 | 5.4 | mA | VDD = 2.4V, VOL = 0.4V |
| Sink current P0, ALE, <u>PSEN</u> , P4.6 | ISK2 | 10 | 18 | mA | VDD = 4.5V, VOL = 0.45V |
| | | 4.5 | 9 | mA | VDD = 2.4V, VOL = 0.4V |
| Sink current P3.4 to P3.7 in High-Drive mode | ISK3 | 12 | 24 | mA | VDD = 4.5V, VOL = 0.45V |
| Output High Voltage P1, P2, P3, P4 | VOH1 | 2.4 | - | V | VDD = 4.5V, VOH = -100 µA |
| | | 1.4 | - | V | VDD = 2.4V, VOH = -20 µA |
| Output High Voltage P0, ALE, <u>PSEN</u> ^[*4] | VOH2 | 2.4 | - | V | VDD = 4.5V, IOH = -400 µA |
| | | 1.4 | - | V | VDD = 2.4V, IOH = -200 µA |
| Source current P1, P2, P3, P4<0:4> | ISR1 | -120 | -250 | µA | VDD = 4.5V, VOH = 2.4V |
| | | -20 | -40 | µA | VDD = 2.4V, VOH = 1.4V |
| Source current P0, ALE, <u>PSEN</u> , P4.6 | ISR2 | -10 | -14 | mA | VDD = 4.5V, VOH = 2.4V |
| | | -1.9 | -3.3 | mA | VDD = 2.4V, VOH = 1.4V |

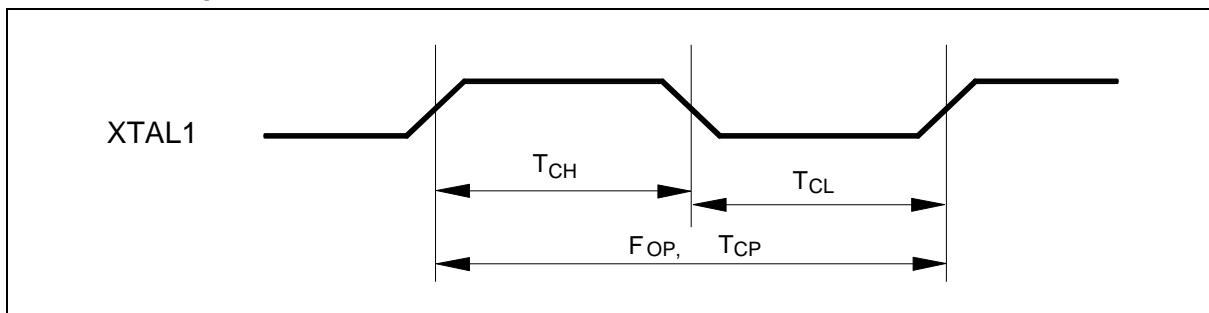
Notes:

- *1. RST pin has an internal pull-down.
- *2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.
- *3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.
- *4. P0, P2, ALE and PSEN are tested in the external access mode.
- *5. P3.4 to P3.7 are in normal mode.
- *6. P3 (P3.4 – P3.7) is used LED driver port by set SFR.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

9.1 Clock Input Waveform



| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|-----------------|--------|------|------|------|------|-------|
| Operating Speed | FOP | 0 | - | 20 | MHz | 1 |
| Clock Period | TCP | 50 | - | - | nS | 2 |
| Clock High | TCH | 25 | - | - | nS | 3 |
| Clock Low | TCL | 25 | - | - | nS | 3 |

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

9.2 Program Fetch Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|----------------------------|--------|------------------|-------|-------|------|-------|
| Address Valid to ALE Low | TAAS | 1 TCP - Δ | - | - | nS | 4 |
| Address Hold from ALE Low | TAAH | 1 TCP - Δ | - | - | nS | 1, 4 |
| ALE Low to PSEN Low | TAPL | 1 TCP - Δ | - | - | nS | 4 |
| PSEN Low to Data Valid | TPDA | - | - | 2 TCP | nS | 2 |
| Data Hold after PSEN High | TPDH | 0 | - | 1 TCP | nS | 3 |
| Data Float after PSEN High | TPDZ | 0 | - | 1 TCP | nS | |
| ALE Pulse Width | TALW | 2 TCP - Δ | 2 TCP | - | nS | 4 |
| PSEN Pulse Width | TPSW | 3 TCP - Δ | 3 TCP | - | nS | 4 |

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to PSEN going high.
4. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

9.3 Data Read Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|-------------------------|--------|------------------|-------|------------------|------|-------|
| ALE Low to RD Low | TDAR | 3 TCP - Δ | - | 3 TCP + Δ | nS | 1, 2 |
| RD Low to Data Valid | TDDA | - | - | 4 TCP | nS | 1 |
| Data Hold from RD High | TDDH | 0 | - | 2 TCP | nS | |
| Data Float from RD High | TDDZ | 0 | - | 2 TCP | nS | |
| RD Pulse Width | TDRD | 6 TCP - Δ | 6 TCP | - | nS | 2 |

Notes:

1. Data memory access time is 8 TCP.
2. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

9.4 Data Write Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|------------------------|--------|------------------|-------|------------------|------|
| ALE Low to WR Low | TDAW | 3 TCP - Δ | - | 3 TCP + Δ | nS |
| Data Valid to WR Low | TDAD | 1 TCP - Δ | - | - | nS |
| Data Hold from WR High | TDWD | 1 TCP - Δ | - | - | nS |
| WR Pulse Width | TDWR | 6 TCP - Δ | 6 TCP | - | nS |

Note: " Δ " (due to buffer driving delay and wire loading) is 20 nS.

9.5 Port Access Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|------------------------------|--------|-------|------|------|------|
| Port Input Setup to ALE Low | TPDS | 1 TCP | - | - | nS |
| Port Input Hold from ALE Low | TPDH | 0 | - | - | nS |
| Port Output to ALE | TPDA | 1 TCP | - | - | nS |

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

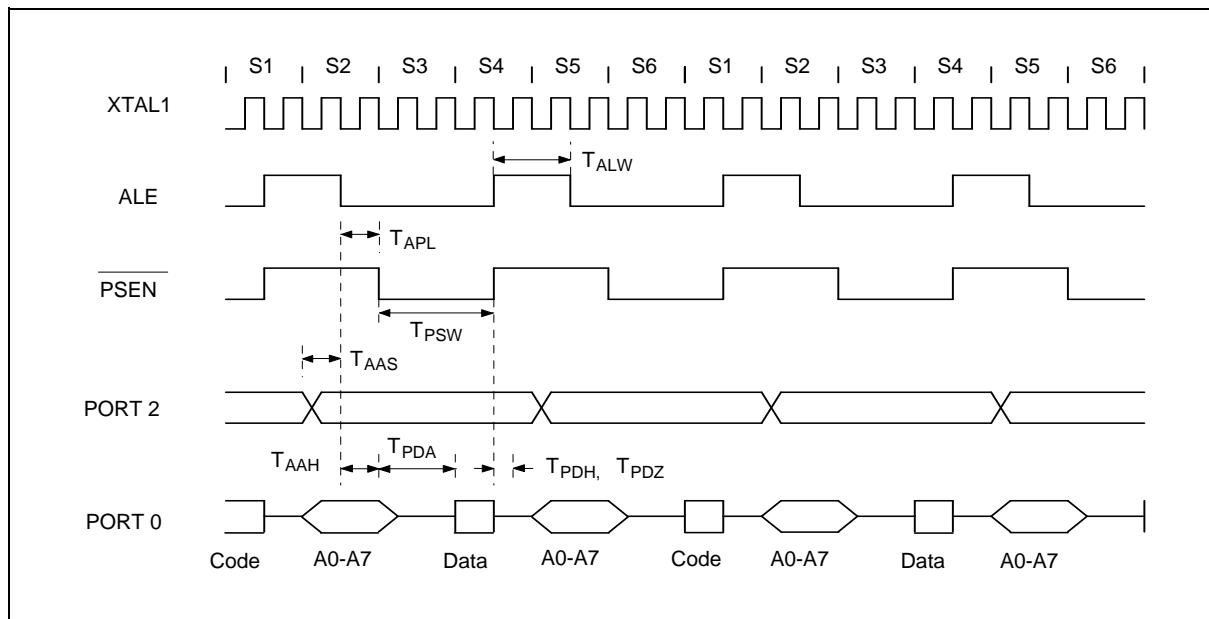
9.6 Program Operation

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|--------|------|------|------|------|
| VPP Setup Time | TVPS | 2.0 | - | - | μS |
| Data Setup Time | TDS | 2.0 | - | - | μS |
| Data Hold Time | TDH | 2.0 | - | - | μS |
| Address Setup Time | TAS | 2.0 | - | - | μS |
| Address Hold Time | TAH | 0 | - | - | μS |
| CE Program Pulse Width for Program Operation | TPWP | 290 | 300 | 310 | μS |
| OECTRL Setup Time | TOCS | 2.0 | - | - | μS |
| OECTRL Hold Time | TOCH | 2.0 | - | - | μS |
| OE Setup Time | TOES | 2.0 | - | - | μS |
| OE High to Output Float | TDFP | 0 | - | 130 | nS |
| Data Valid from OE | TOEV | - | - | 150 | nS |

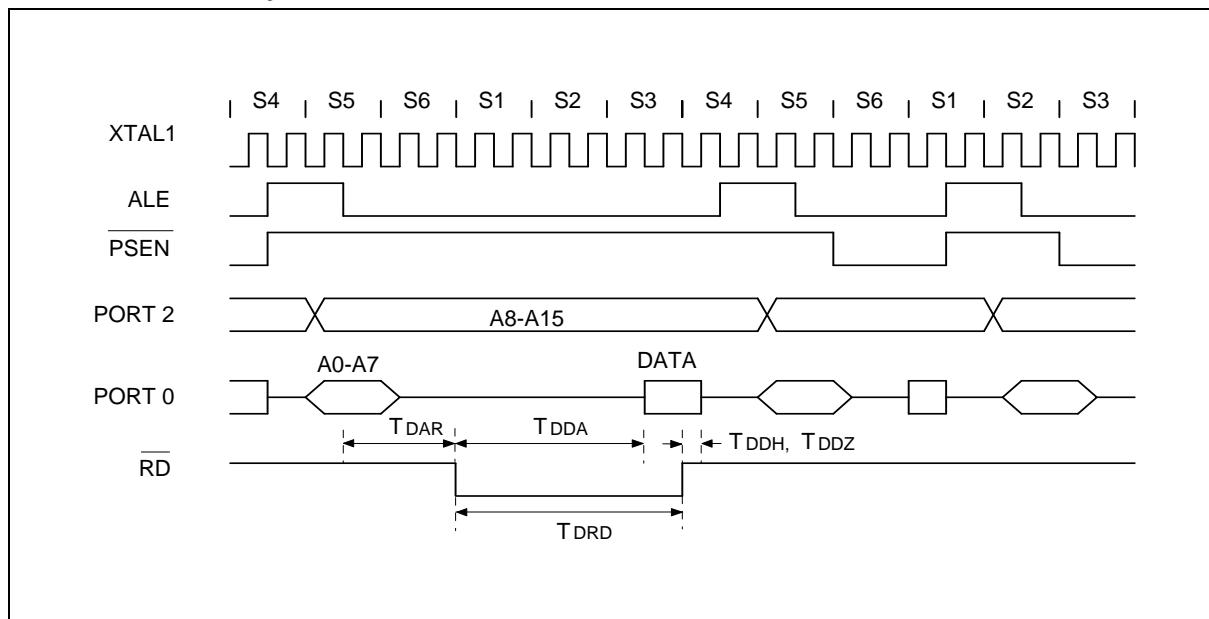
Note: Flash data can be accessed only in flash mode. The RST pin must pull in V_{IH} status, the ALE pin must pull in V_{IL} status, and the PSEN pin must pull in V_{IH} status.

10. TIMING WAVEFORMS

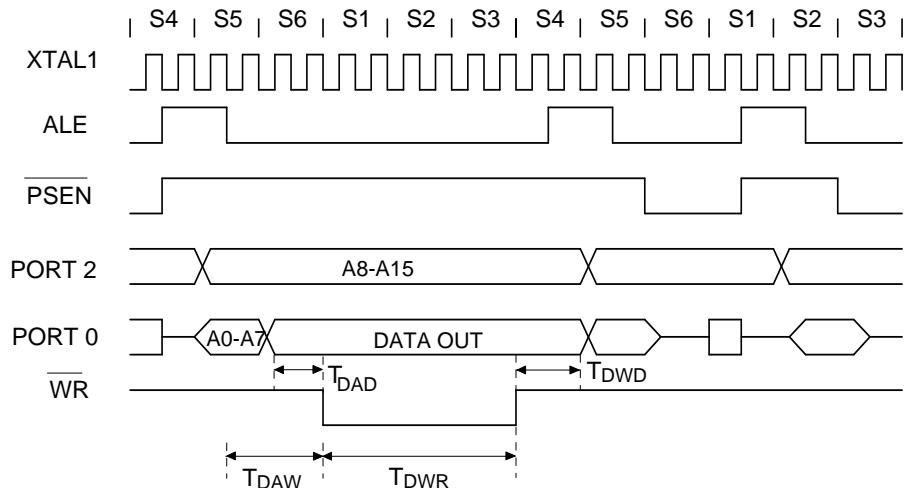
10.1 Program Fetch Cycle



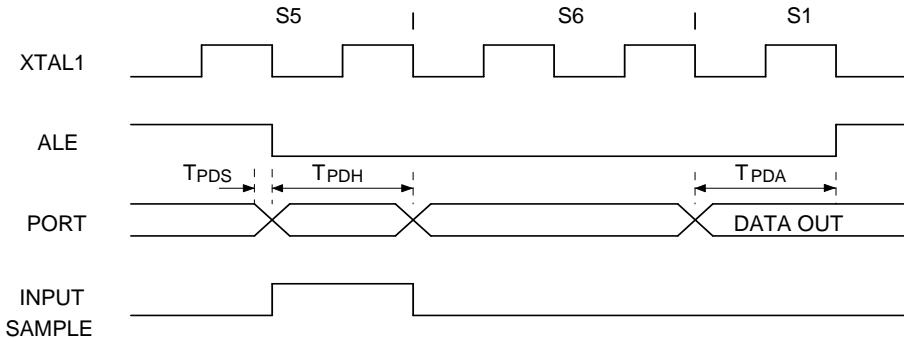
10.2 Data Read Cycle



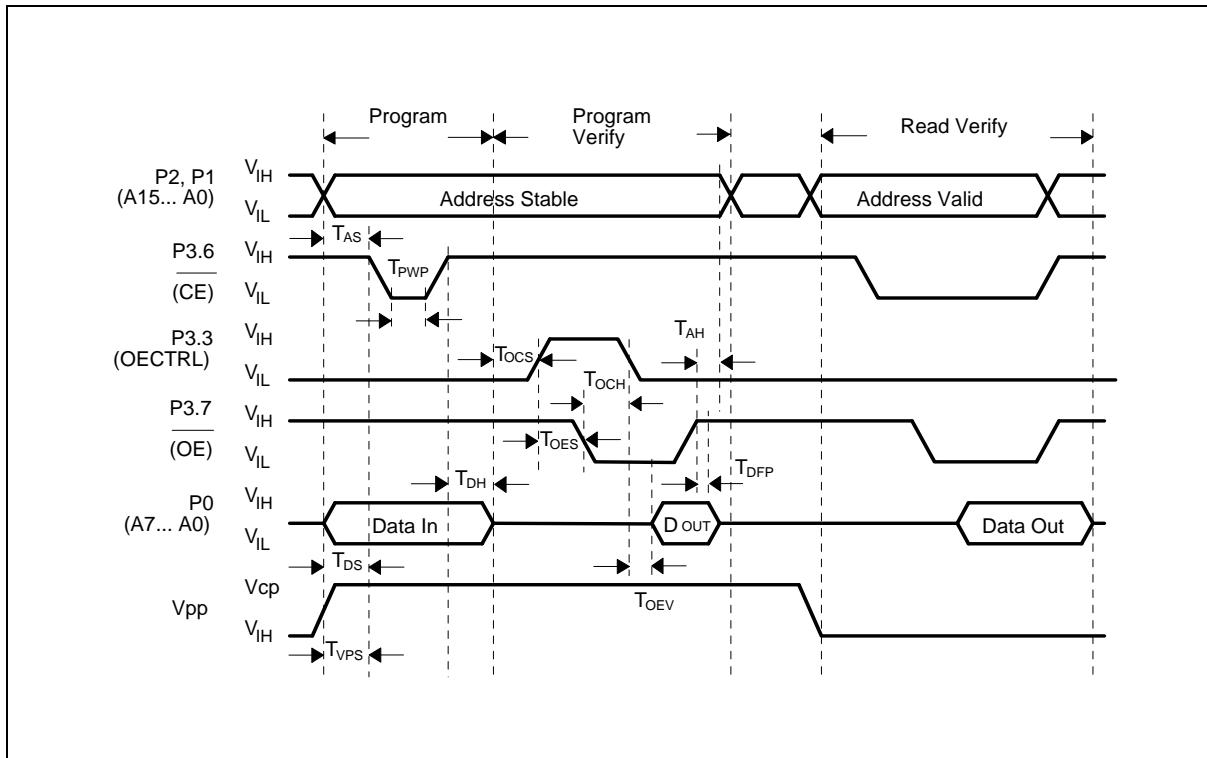
10.3 Data Write Cycle



10.4 Port Access Cycle



10.5 Program Operation



11. TYPICAL APPLICATION CIRCUITS

11.1 Expanded External Program Memory and Crystal

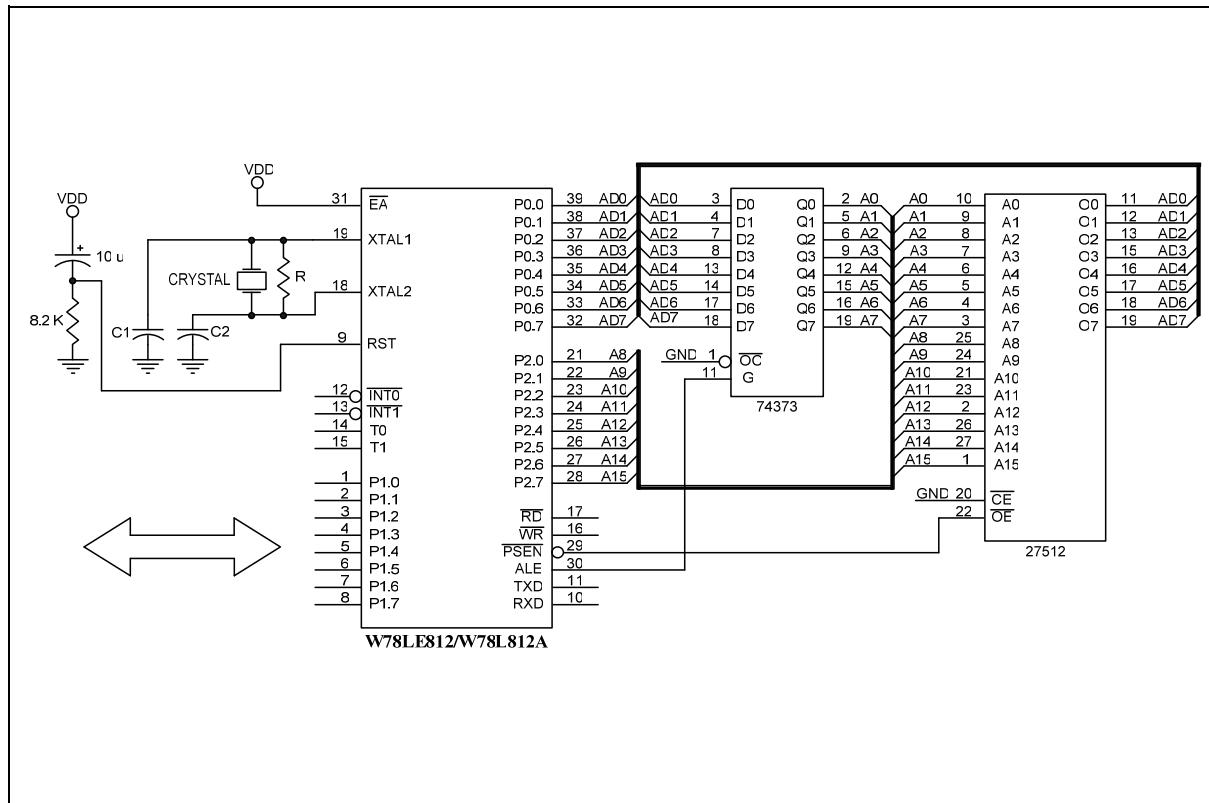


Figure A

| CRYSTAL | C1 | C2 | R |
|---------|-----|-----|---|
| 16 MHz | 30P | 30P | - |
| 20 MHz | 15P | 15P | - |

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Typical Application Circuits, continued

11.2 Expanded External Data Memory and Oscillator

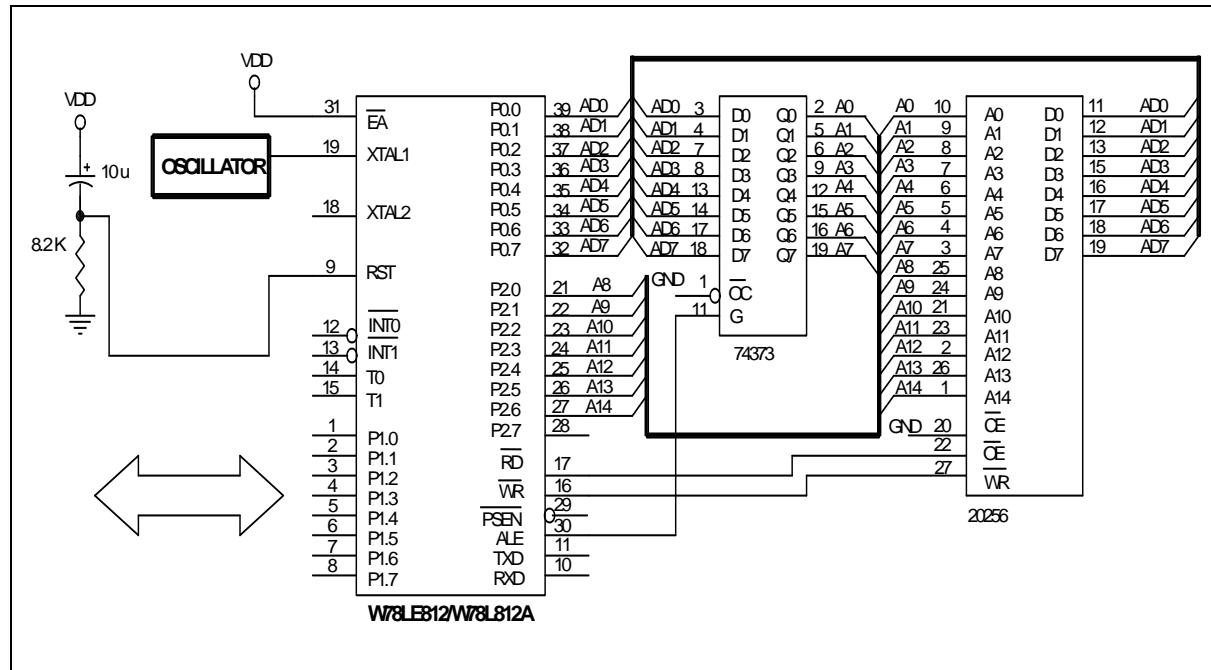
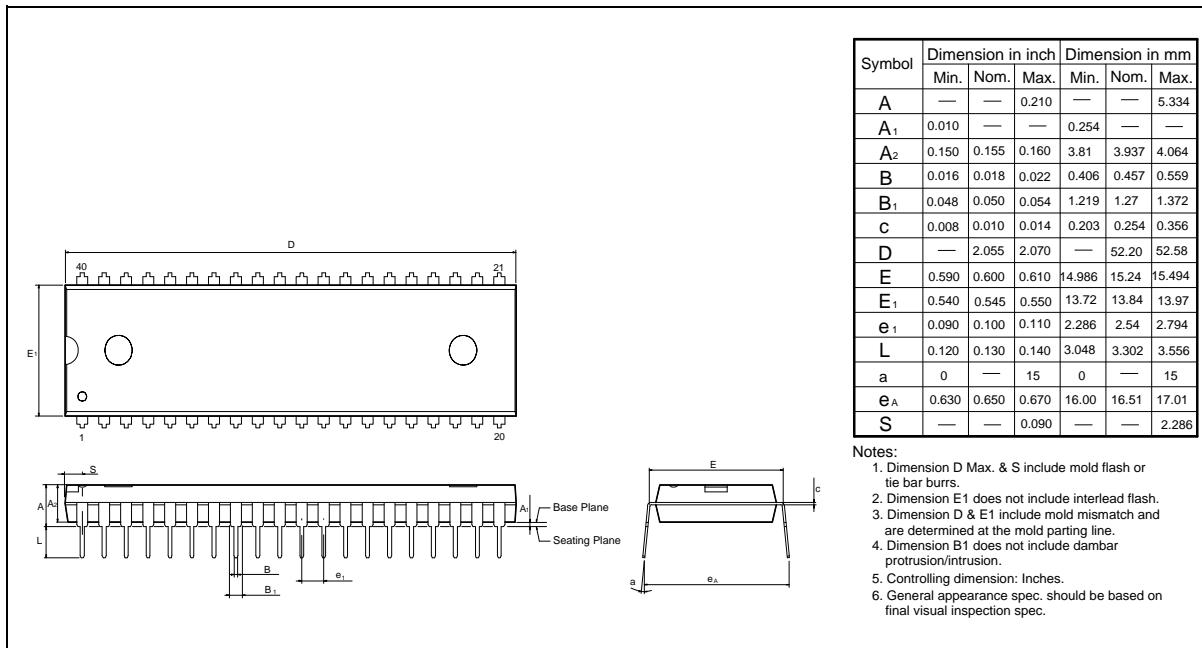


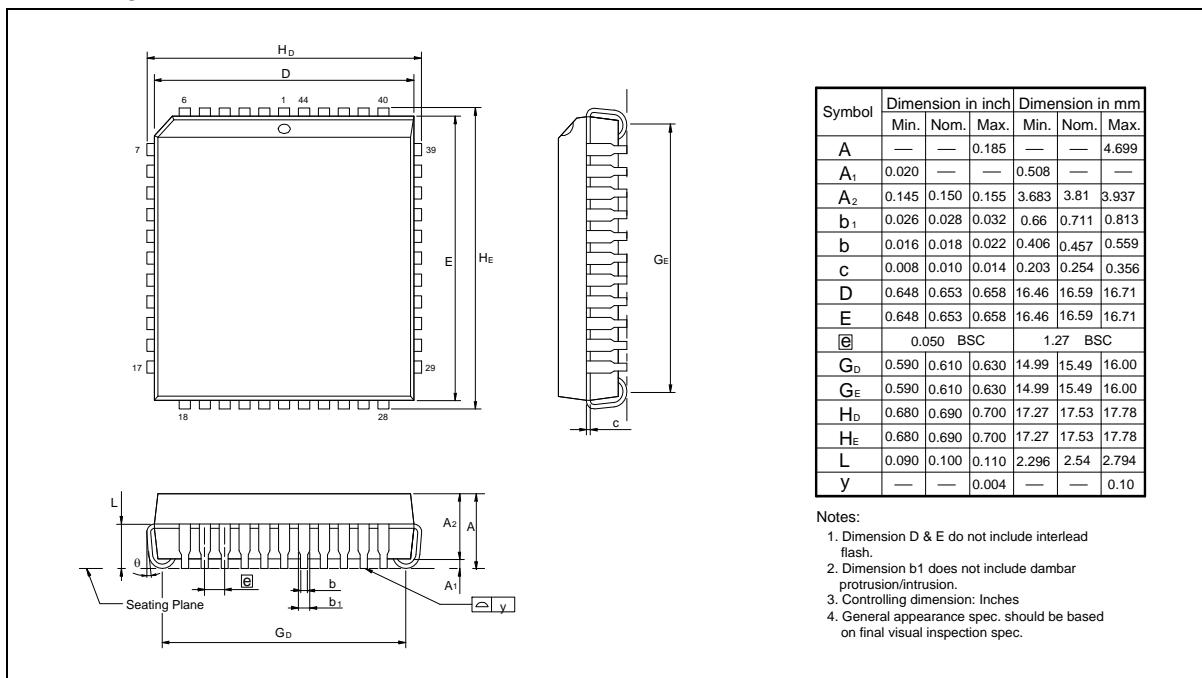
Figure B

12. PACKAGE DIMENSIONS

12.1 40-pin DIP



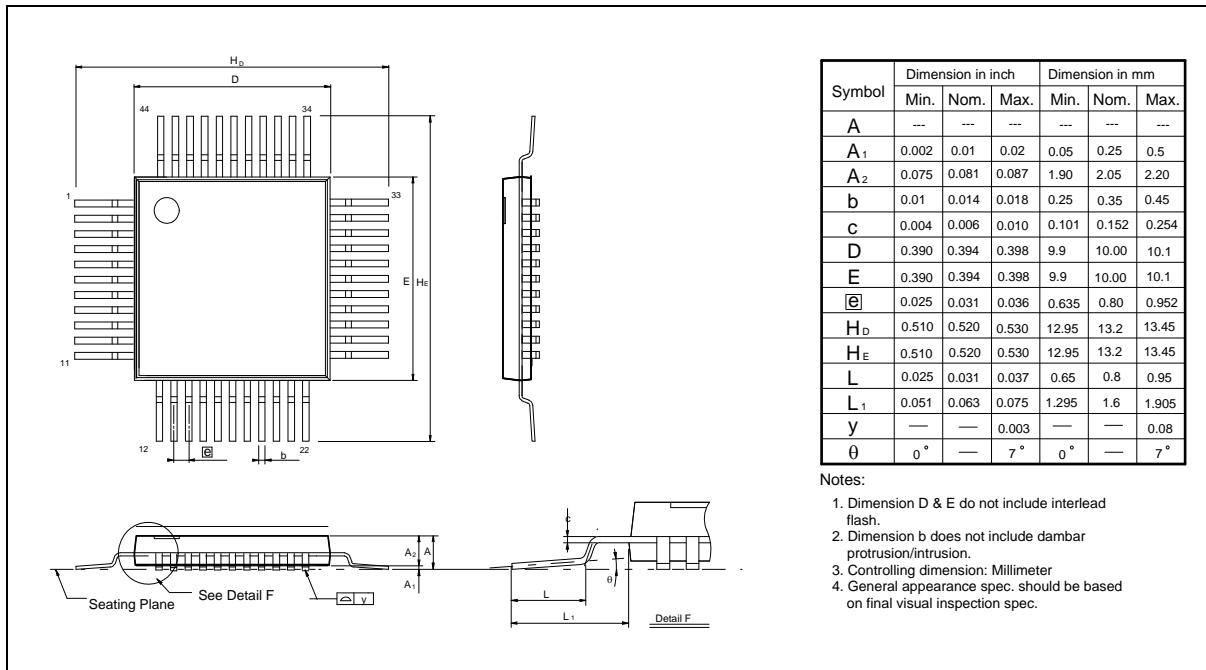
12.2 44-pin PLCC



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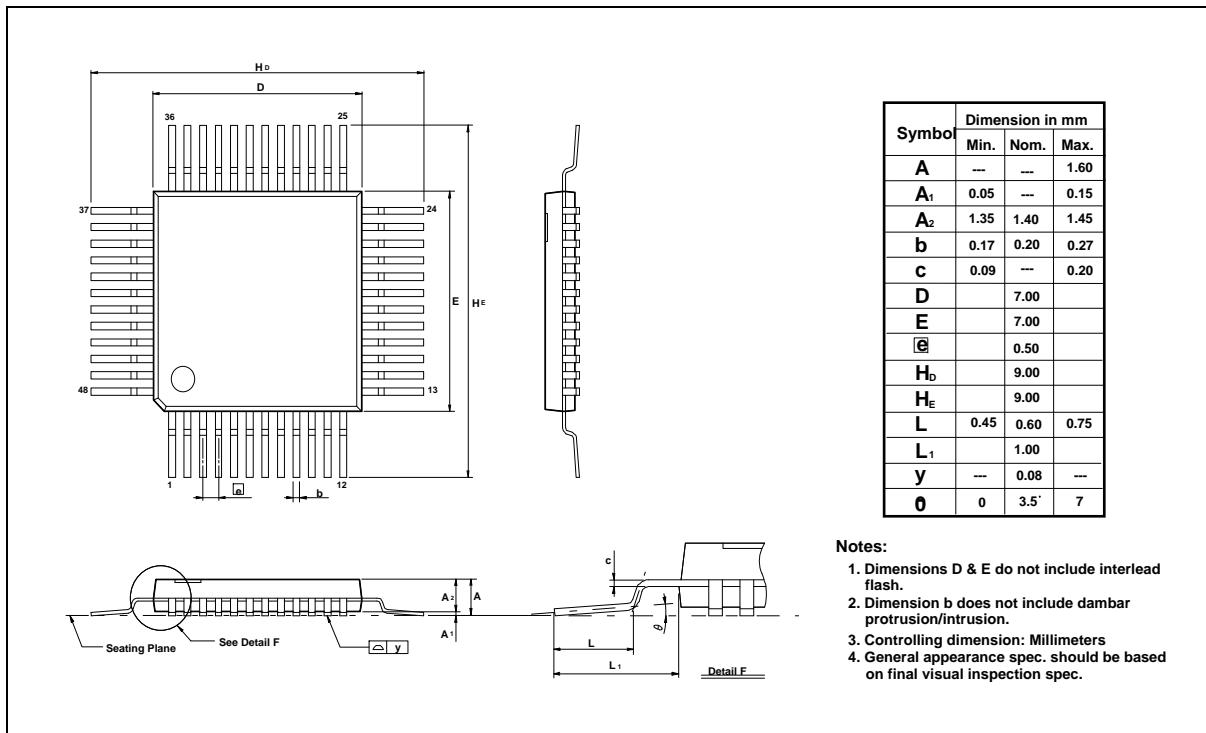
12.3 44-pin PQFP



12.4 48-pin LQFP

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13. REVISION HISTORY

| VERSION | DATE | PAGE | REASONS FOR CHANGE |
|---------|------------------|--------------------|--|
| A5 | October 15, 2001 | | - |
| A6 | April 19, 2005 | 26 | Add Important Notice |
| A7 | July 1, 2005 | 3 | Add lead free (RoHS) parts |
| A8 | June 19, 2006 | 3,5 31 13,14 | Add a part in 48-pin LQFP part Add package spec of 48-pin LQFP Correct the watchdog prescale table |
| A9 | November 6, 2006 | | Remove block diagram |
| | | 3 | Remove all Leaded package parts |
| A10 | July 29, 2008 | 5 | Correct typo and pin sequence in 48-pin LQFP diagram |

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