

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
20	0.003 at $V_{GS} = 4.5$ V	29	57
	0.0042 at $V_{GS} = 2.5$ V	25	

FEATURES

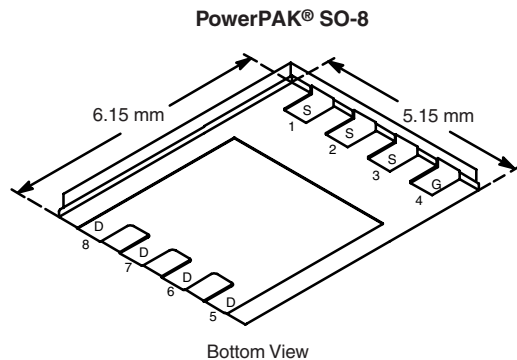
- Halogen-free available
- TrenchFET® Power MOSFETS: 2.5 V Rated
- Low 3.5 m Ω $R_{DS(on)}$
- PWM (Q_{gd} and R_g) Optimized
- 100 % R_g Tested



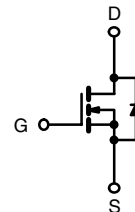
RoHS
COMPLIANT

APPLICATIONS

- Low-Side MOSFET in Synchronous Buck DC/DC Converters in Servers and Routers



Ordering Information: Si7864ADP-T1-E3 (Lead (Pb)-free)
Si7864ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	29	18	A
	T _A = 70 °C		25	14	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	60		
Continuous Source Current (Diode Conduction) ^a		I _S	4.5	1.6	
Avalanche Current	L = 0.1 mH	I _{AS}	40		
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	5.4	1.9	W
	T _A = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	18	23	°C/W
		50	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

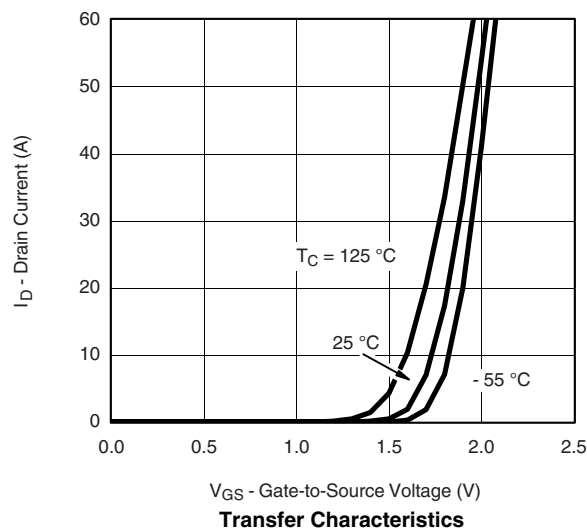
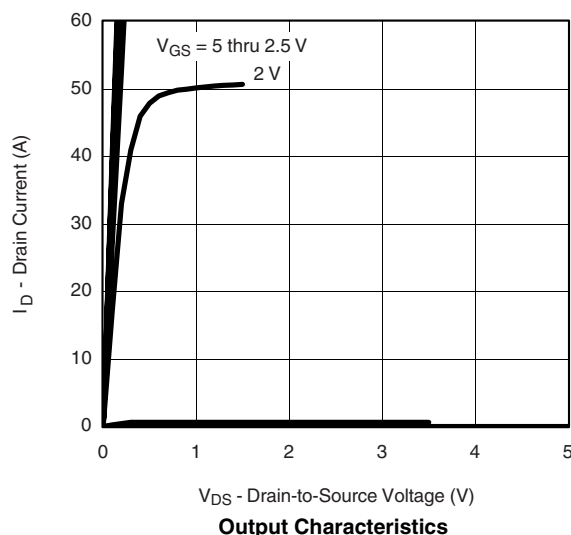
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 29\ \text{A}$		0.0023	0.003	Ω
		$V_{GS} = 2.5\ \text{V}$, $I_D = 25\ \text{A}$		0.0032	0.0042	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6\ \text{V}$, $I_D = 29\ \text{A}$		70		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.5\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.70	1.2	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		5330		pF
Output Capacitance	C_{oss}			1240		
Reverse Transfer Capacitance	C_{rss}			680		
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 29\ \text{A}$		57	85	nC
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}			17		
Gate Resistance	R_g		0.5	1.3	2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_G = 6\ \Omega$		40	60	ns
Rise Time	t_r			44	65	
Turn-Off Delay Time	$t_{d(off)}$			150	240	
Fall Time	t_f			72	110	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		57	80	

Notes:

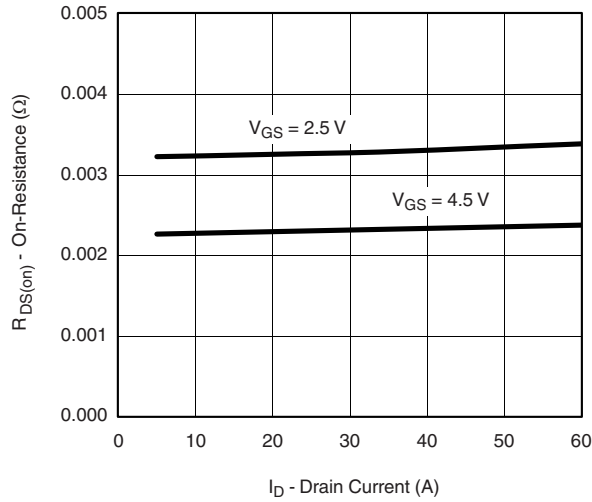
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

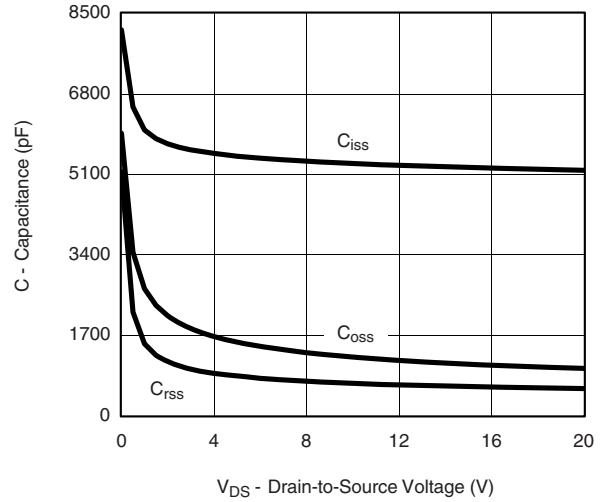
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

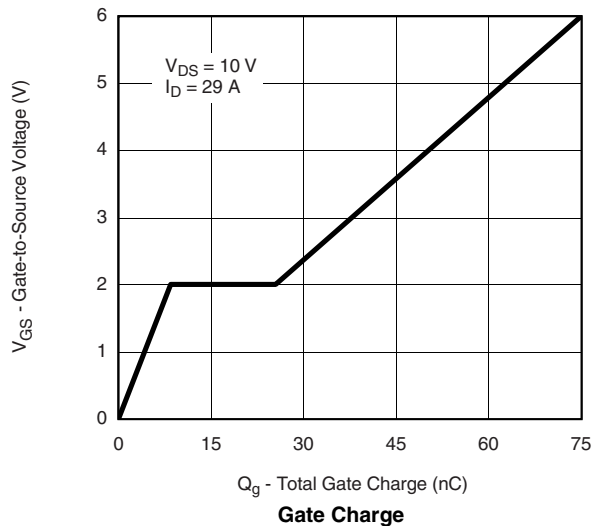
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



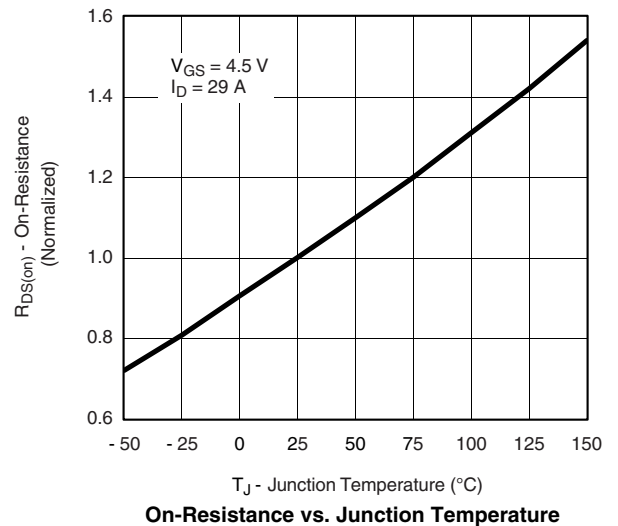
On-Resistance vs. Drain Current



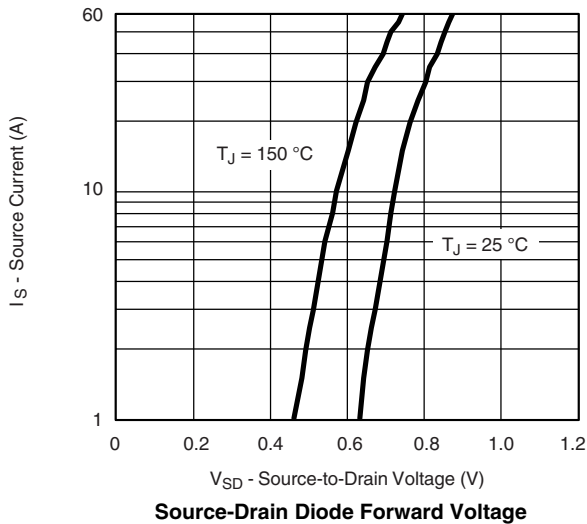
Capacitance



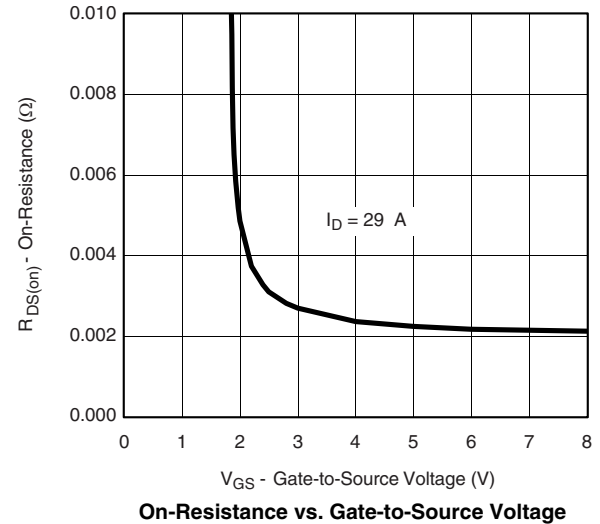
Gate Charge



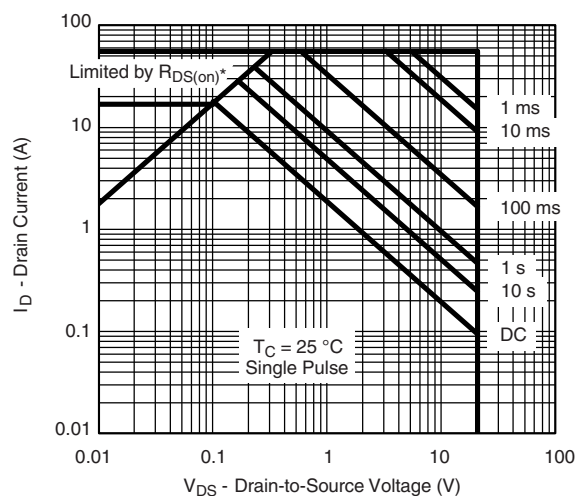
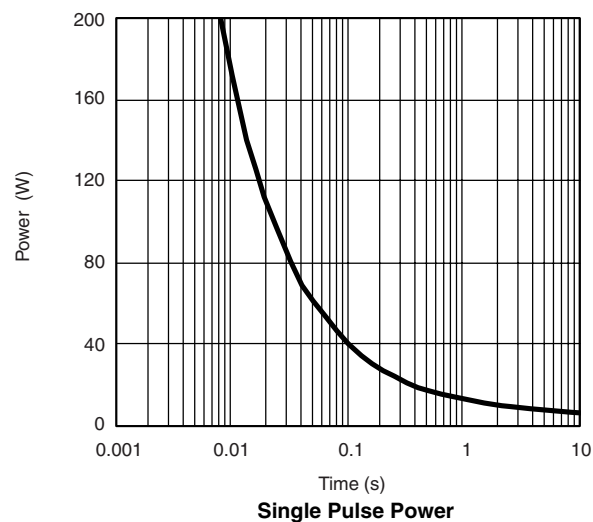
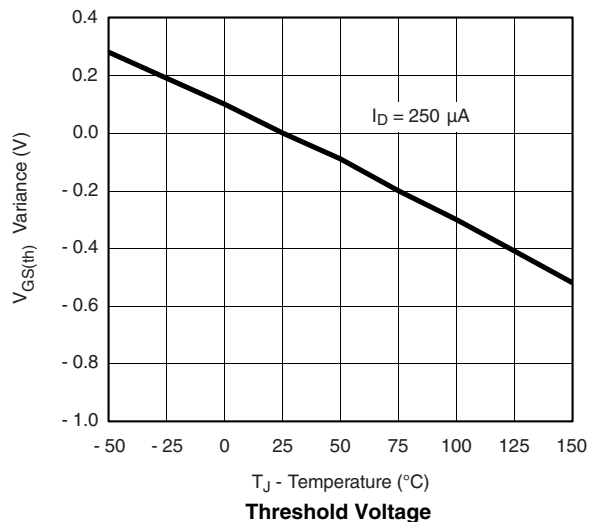
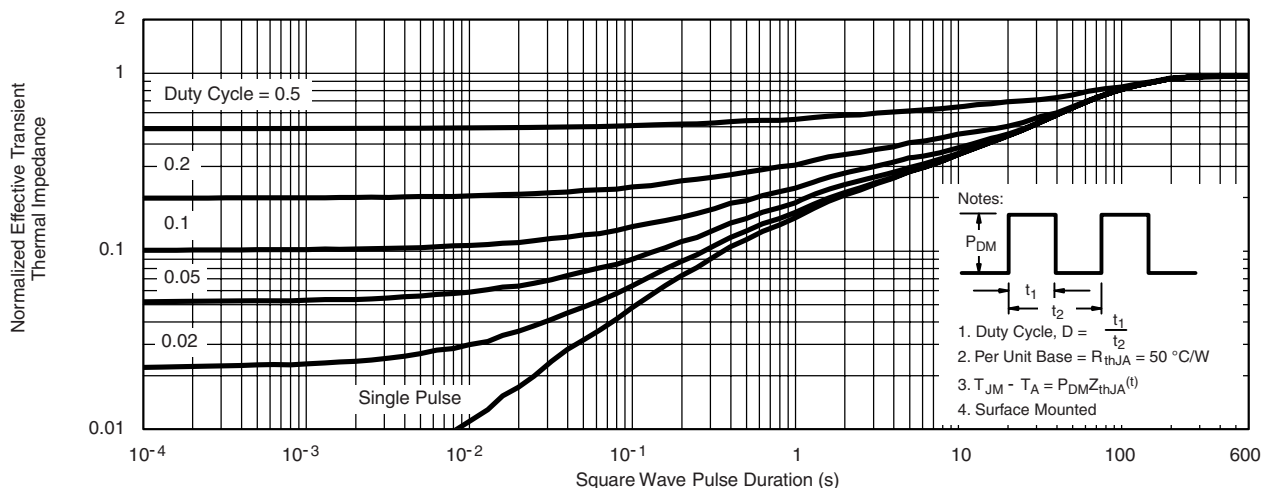
On-Resistance vs. Junction Temperature



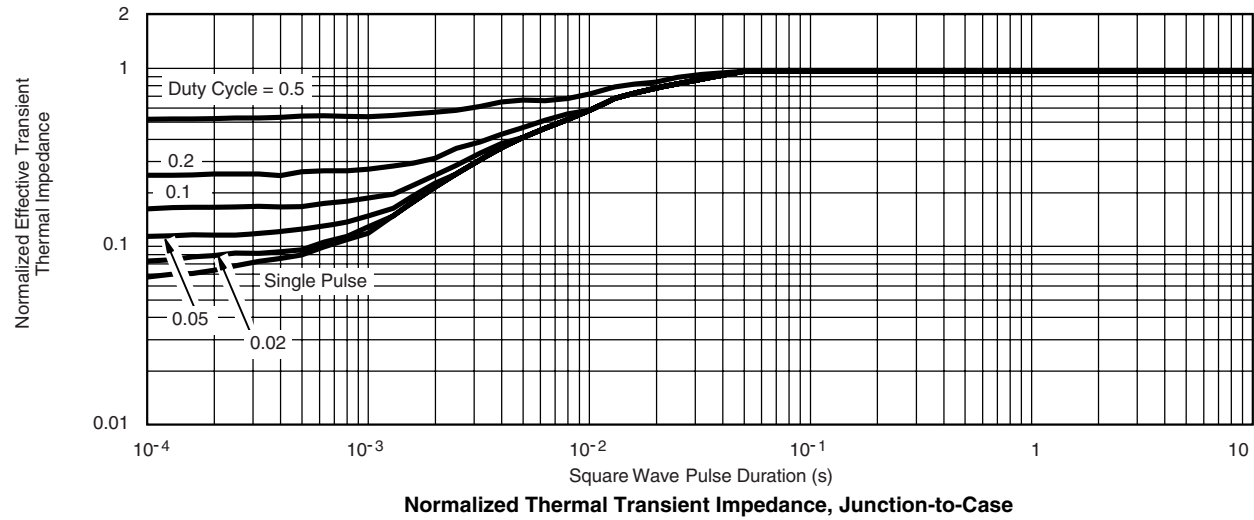
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Case****Normalized Thermal Transient Impedance, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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