



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	TO-220
60V	1.5Ω	3.0A	2.0V	TN0606N3	TN0606N5
100V	1.5Ω	3.0A	2.0V	TN0610N3	—

† MIL visual screening available

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Features

- ☐ Low threshold — 2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance — 100pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

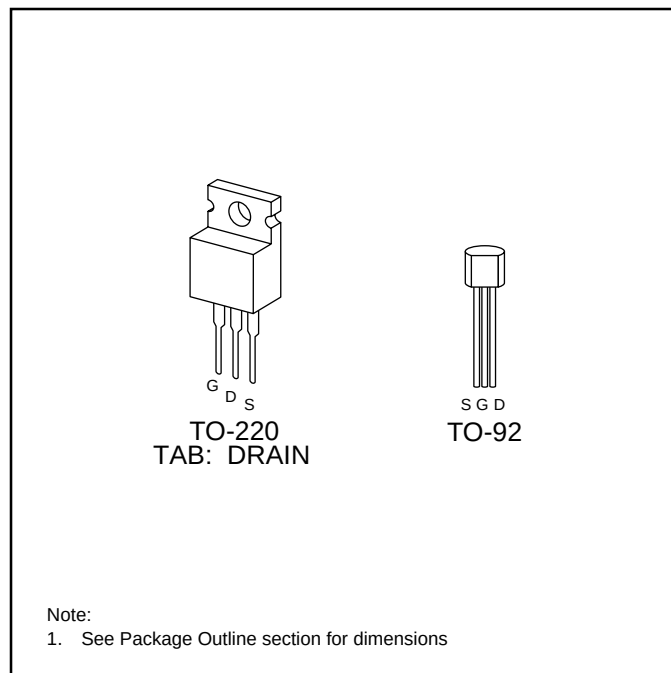
- ☐ Logic level interfaces – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-92	0.8A	3.2A	1W	125	170	0.8A	3.2A
TO-220	3.0A	4.1A	45W	2.7	70	3.0A	4.1A

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0610	100			V	$V_{GS} = 0V, I_D = 1mA$
		TN0606	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		2.0	V	$V_{GS} = V_{DS}, I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
					1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$ (note 2)
$I_{D(ON)}$	ON-State Drain Current		1.2	2.0		A	$V_{GS} = 5V, V_{DS} = 25V$
			3.0	6.7			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance				15	Ω	$V_{GS} = 3V, I_D = 0.25A$
					1.5		$V_{GS} = 5V, I_D = 0.75A$
					1.0		$V_{GS} = 10V, I_D = 0.75A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 0.75A$
G_{FS}	Forward Transconductance		0.4	0.5		S	$V_{DS} = 25V, I_D = 1.0A$
C_{ISS}	Input Capacitance			100	150	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				6	ns	$V_{DD} = 25V$ $I_D = 1.5A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				14		
$t_{d(OFF)}$	Turn-OFF Delay Time				16		
t_f	Fall Time				16		
V_{SD}	Diode Forward Voltage Drop			0.8	1.8	V	$V_{GS} = 0V, I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V, I_{SD} = 1.5A$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

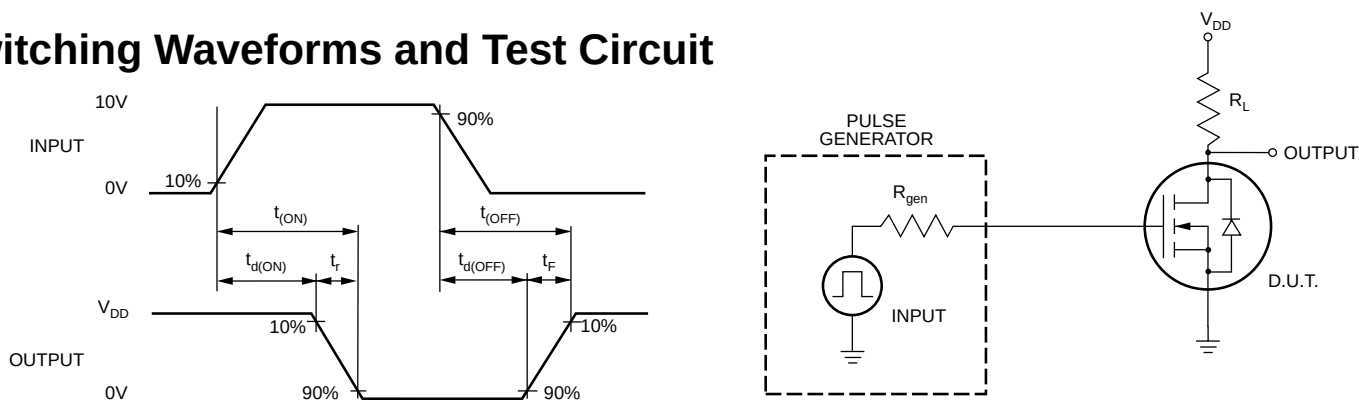


Figure 1 is a graph showing the drain current (I_D) in amperes versus the drain-source voltage (V_{DS}) in volts for the 2N7000 MOSFET. The graph displays several curves for different gate-source voltages (V_{GS}), ranging from 3V to 10V. The curves show that I_D increases with V_{DS} and then saturates. The saturation current increases as V_{GS} increases.

V_{GS} (V)	Saturation I_D (A)
10V	~6.5
9V	~5.5
8V	~4.5
7V	~3.8
6V	~3.0
5V	~2.1
3V	~1.2

Figure 10 is a graph showing the drain current (I_D) in amperes versus the drain-source voltage (V_{DS}) in volts for the 2N7000 MOSFET. The graph displays several curves for different gate-source voltages (V_{GS}), ranging from 3V to 10V. The curves show that I_D increases with V_{DS} and eventually saturates. The saturation current increases as V_{GS} increases.

V_{GS} (V)	I_D (A) at $V_{DS} = 10$ V
3	~1.2
4	~1.6
5	~2.2
6	~2.8
7	~3.5
8	~4.2
9	~4.8
10	~5.5

Figure 10 is a graph showing the forward transconductance (G_{FS}) in siemens versus drain current (I_D) in amperes for the 2N3866 JFET at $V_{DS} = 25V$. The graph includes three curves for different ambient temperatures (T_A): $T_A = -55^\circ C$ (solid line), $T_A = 25^\circ C$ (dashed line), and $T_A = 150^\circ C$ (dotted line). The G_{FS} increases sharply with I_D and then levels off. Higher temperatures result in lower G_{FS} values for a given I_D .

The graph shows the power dissipation capability of TO-220 and TO-92 packages as a function of case temperature. The y-axis represents power dissipation P_D in watts, ranging from 0 to 50. The x-axis represents case temperature T_C in degrees Celsius, ranging from 0 to 150. The TO-220 package (top line) has a constant power dissipation of 45 watts from 0°C to 25°C, then decreases linearly to 0 watts at 150°C. The TO-92 package (bottom line) has a constant power dissipation of 1 watt from 0°C to 25°C, then decreases linearly to 0 watts at 150°C.

T_C (°C)	P_D (watts) - TO-220	P_D (watts) - TO-92
0	45	1
25	45	1
50	35	0.5
75	25	0.25
100	15	0.125
125	5	0.0625
150	0	0

Figure 1 is a log-log plot showing the drain current I_D (amperes) versus the drain-source voltage V_{DS} (volts) for TO-220 and TO-92 packages. The y-axis ranges from 0.01 to 10 amperes, and the x-axis ranges from 1 to 1000 volts. The TO-220 (DC) curve shows a higher current limit (approx. 3A) compared to the TO-92 (DC) curve (approx. 0.8A). Both curves show a linear decrease in current as voltage increases beyond the saturation point. The temperature is specified as $T_C = 25^\circ\text{C}$.

Figure 10 is a graph showing Normalized Thermal Resistance (Y-axis, 0 to 1.0) versus t_b (seconds) (X-axis, logarithmic scale from 0.001 to 10). The graph compares the thermal resistance characteristics of TO-220 and TO-92 packages under different power dissipation and ambient temperature conditions.

Legend:

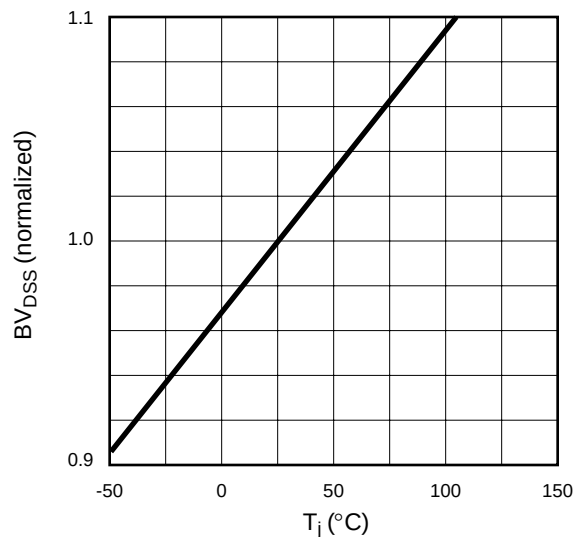
- TO-220: $P_D = 45W$, $T_C = 25^\circ C$
- TO-92: $P_D = 1W$, $T_C = 25^\circ C$

The TO-220 curve (upper curve) shows a higher normalized thermal resistance compared to the TO-92 curve (lower curve) for the same t_b . Both curves start at a normalized thermal resistance of 0 at $t_b = 0$ and increase as t_b increases, reaching 1.0 at $t_b = 10$ seconds.

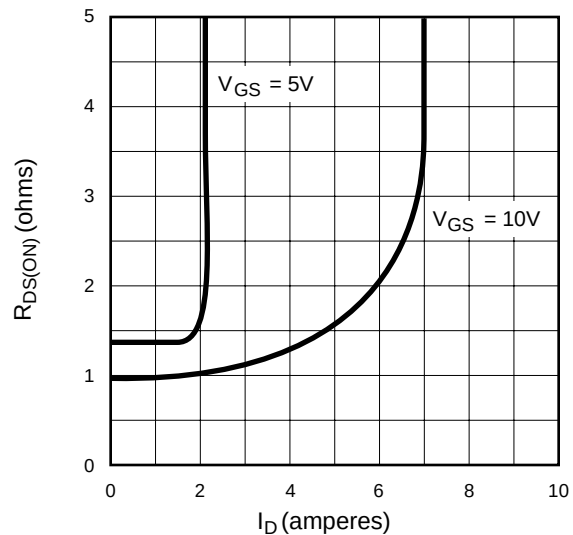
t_b (seconds)	TO-220 Normalized Thermal Resistance	TO-92 Normalized Thermal Resistance
0.001	0.05	0.01
0.01	0.25	0.03
0.1	0.55	0.10
1	0.85	0.25
10	1.00	1.00

Typical Performance Curves

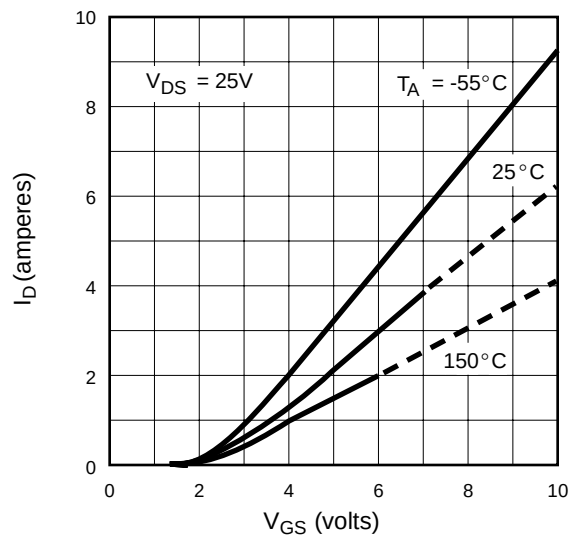
BV_{DSS} Variation with Temperature



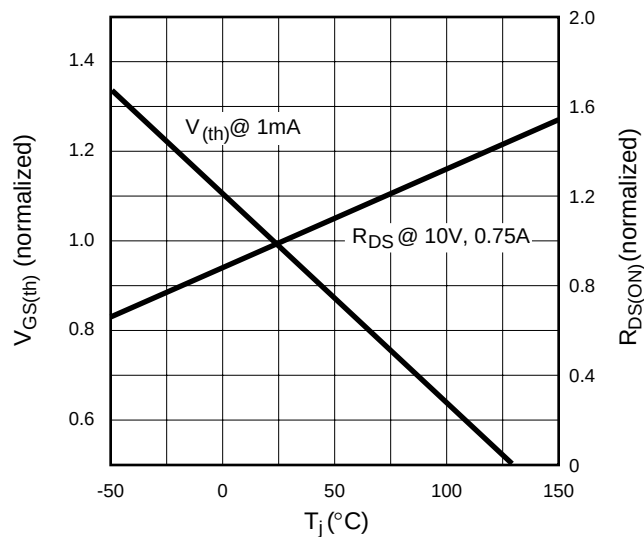
On-Resistance vs. Drain Current



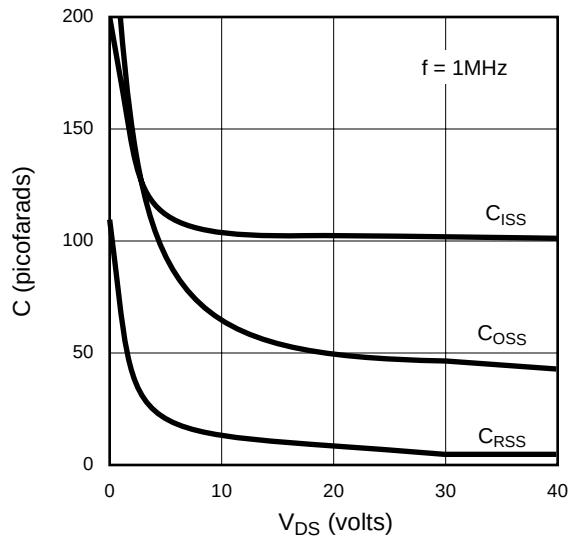
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

