19-4330; Rev 1; 7/95

MAXIM

660ns µP-Compatible, 8-Bit ADC with Track/Hold

MX7821

General Description

The MX7821 high-speed, microprocessor-compatible (µP), 8-bit analog-to-digital converter (ADC) is a plug-in upgrade for the industry-standard 7820. The MX7821 uses a half-flash technique, resulting in a 660ns conversion time vs. 1.36µs for the 7820. A VSS pin, not supplied by the 7820, supports dual power supplies and bipolar analog inputs.

The MX7821 has track-and-hold function capable of digitizing a 100kHz signal, and is tested for both its static and dynamic capability. The converter-µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The MX7821 has an overflow output for cascading devices to attain higher resolution. The ADC's input/reference arrangement enables ratiometric operation. For a detailed description of MX7821 operation, refer to the MX7820 data sheet.

Applications

Digital-Signal Processing

High-Speed Data Acquisition

Telecommunications

High-Speed Servo Loops

Audio Systems

Features

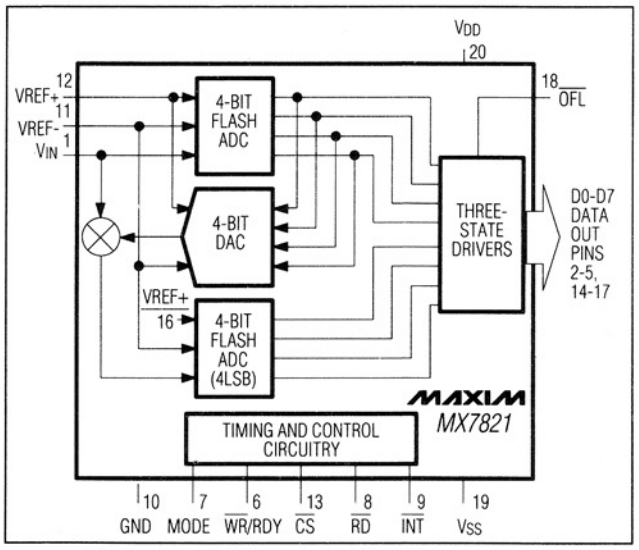
- ♦ 660ns Conversion Time
- ♦ 20-Pin Narrow DIP Package
- ♦ No External Clock
- ♦ Pin-Compatible Upgrade for Industry-Standard 7820
- ♦ 100kHz Input Signal Bandwidth
- ♦ Bipolar/Unipolar Inputs
- ♦ Single +5V or Dual ±5V Supplies
- ♦ Ratiometric Reference Inputs
- ♦ Static and Dynamic Tested
- ♦ Internal Track/Hold

Ordering Information

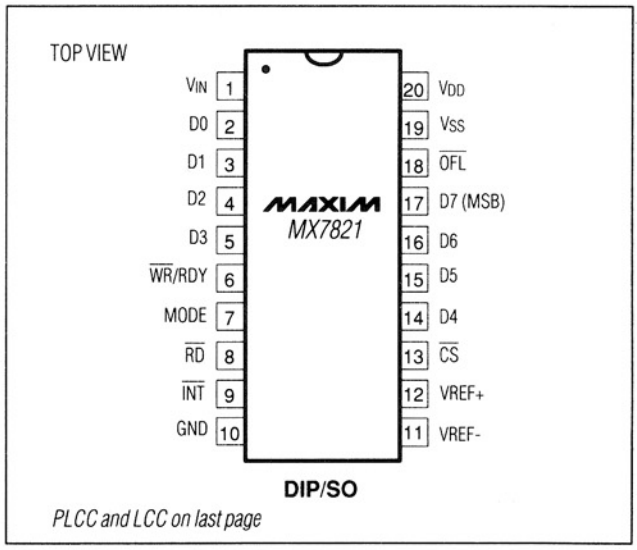
PART	TEMP. RANGE	PIN-PACKAGE
MX7821KN	0°C to +70°C	20 Plastic DIP
MX7821KR	0°C to +70°C	20 Wide SO
MX7821KP	0°C to +70°C	20 PLCC
MX7821K/D	0°C to +70°C	Dice*
MX7821BQ	-40°C to +85°C	20 CERDIP
MX7821KEWP	-40°C to +85°C	20 Wide SO
MX7821TE	-55°C to +125°C	20 LCC**
MX7821TQ	-55°C to +125°C	20 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configurations



DIP/SO

PLCC and LCC on last page

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

660ns µP-Compatible, 8-Bit ADC with Track/Hold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -7V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-16, 18) ..... -0.3V to V_{DD} +0.3V
VREF+ to AGND ..... V_{SS} -0.3V to V_{DD} +0.3V
VREF- to AGND ..... V_{SS} -0.3V to V_{DD} +0.3V
V_{IN} to GND ..... V_{SS} -0.3V to V_{DD} +0.3V
Continuous Power Dissipation (any package)
to +75°C 1000mW
derate above +75°C by ..... 10mW/°C

Operating Temperature Ranges:
MX7821K_ ..... 0°C to +70°C
MX7821B_ ..... -40°C to +85°C
MX7821T_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%; GND = 0V; Unipolar Input Range: V_{SS} = 0V, VREF+ = 5V, VREF- = 0V; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; specifications apply for RD mode, Pin 7 = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UNIPOLAR INPUT RANGE							
Resolution	N			8			Bits
Total Unadjusted Error (Note 2)	TUE					±1	LSB
No Missing Codes Resolution				8			Bits
BIPOLAR INPUT RANGE							
Resolution	N			8			Bits
Zero-Code Error						±1	LSB
Full-Scale Error						±1	LSB
Signal-to-Noise Ratio	SNR	V_{IN} = 99.85kHz full-scale sine wave with $f_{SAMPLING}$ = 500kHz		45			dB
Total Harmonic Distortion	THD	V_{IN} = 99.85kHz full-scale sine wave with $f_{SAMPLING}$ = 500kHz				-50	dB
Peak Harmonic or Spurious Noise		V_{IN} = 99.85kHz full-scale sine wave with $f_{SAMPLING}$ = 500kHz				-50	dB
Intermodulation Distortion	IMD	f_a(84.72kHz) and f_b(94.97kHz) full-scale sine waves with $f_{SAMPLING}$ = 500kHz	2nd-order terms			-50	dB
			3rd-order terms			-50	
Slew Rate, Tracking					2.36	1.6	V/µs
REFERENCE INPUT							
Input Resistance		Resistance between VREF+ and VREF-		1		4	kΩ
VREF+ Input Range				VREF-		V_{DD}	V
VREF- Input Range				V_{SS}		VREF+	V
ANALOG INPUT							
Input Voltage Range				VREF-		VREF+	V
Input Leakage Current		-5V ≤ V_{IN} ≤ 5V				±3	µA
Input Capacitance	C_{IN}				32		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; GND = 0V; Unipolar Input Range: V_{SS} = 0V, VREF+ = 5V, VREF- = 0V; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; specifications apply for RD mode, Pin 7 = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		2.4			V
		MODE		3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				0.8	V
		MODE				1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$				1	µA
		$\overline{WR}$				3	
		MODE			50	200	
Input Low Current	I_{INL}					-1	µA
Input Capacitance (Note 3)	C_{IN}				5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D7–D0, $\overline{INT}$, $\overline{OFL}$; I_{SINK} = 1.6mA				0.4	V
		RDY; I_{SINK} = 2.6mA				0.4	
Output High Voltage	V_{OH}	D7–D0, $\overline{INT}$, $\overline{OFL}$; I_{SOURCE} = -360µA		4.0			V
Floating State Leakage Current	I_{LKG}	D7–D0, RDY				±3	µA
Floating State Output Capacitance (Note 3)	C_{OUT}	D7–D0, RDY			5	8	pF
POWER REQUIREMENTS							
Supply Current	I_{DD}	CS = RD = 0V	MX7821K			15	mA
			MAX7821B/T			20	
	I_{SS}					100	µA
Power Dissipation	P_D				50		mW
Power-Supply Sensitivity	PSR	V_{DD} = 4.75V to 5.25V, VREF+ = 4.75V MAX for unipolar mode			±1/16	±1/4	LSB

Note 1: Performance over power-supply tolerance guaranteed by power-supply rejection test.
Note 2: Total Unadjusted Error includes relative accuracy, zero-code error, and full-scale error.
Note 3: Guaranteed by design.

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = 0V or -5V, Unipolar or Bipolar Input Range, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	t_{CSS}			0			ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	t_{CSH}			0			ns
$\overline{CS}$ to RDY Delay (Note 4)	t_{RDY}	T_A = +25°C				70	ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K			85	
			MX7821T			100	
Conversion Time (RD Mode)	t_{CRD}	T_A = +25°C				700	ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K			875	
			MX7821T			975	

660ns µP-Compatible, 8-Bit ADC with Track/Hold

TIMING CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0V or -5V, Unipolar or Bipolar Input Range, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data-Access Time (RD Mode) (Note 5)	t_{ACC0}	T_A = +25°C, C_L = 20pF				t_{CRD}+25	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 20pF	MX7821B/K			t_{CRD}+30	
			MX7821T			t_{CRD}+35	
		T_A = +25°C, C_L = 100pF				t_{CRD}+50	
		T_A = T_{MIN} to T_{MAX}, C_L = 100pF	MX7821B/K			t_{CRD}+65	
			MX7821T			t_{CRD}+75	
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	T_A = +25°C, C_L = 50pF			50	80	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 50pF	MX7821B/K			85	
			MX7821T			90	
Data-Hold Time (Note 6)	t_{DH}	T_A = +25°C				60	ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K			70	
			MX7821T			80	
Delay Time Between Conversions	t_p	T_A = +25°C		350			ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K	425			
			MX7821T	500			
Write Pulse Width	t_{WR}	T_A = +25°C		0.250		10	µs
		T_A = T_{MIN} to T_{MAX}	MX7821B/K	0.325		10	
			MX7821T	0.400		10	
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	T_A = +25°C		250			ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K	350			
			MX7821T	450			
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC1}	t_{READ1}	T_A = +25°C (Figure 3)		160			ns
		T_A = T_{MIN} to T_{MAX} (Figure 3)	MX7821B/K	205			
			MX7821T	240			
Data-Access Time (WR-RD Mode) (Note 5)	t_{ACC1}	T_A = +25°C, C_L = 20pF (Figure 3) (Note 3)				160	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 20pF (Figure 3) (Note 3)	MX7821B/K			205	
			MX7821T			240	
		T_A = +25°C, C_L = 100pF (Figure 3)				185	
		T_A = T_{MIN} to T_{MAX}, C_L = 100pF (Figure 3)	MX7821B/K			235	
			MX7821T			275	
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}	T_A = +25°C				150	ns
		T_A = T_{MIN} to T_{MAX}	MX7821B/K			185	
			MX7821T			220	
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	T_A = =25°C, C_L = 50pF			380	500	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 50pF	MX7821B/K			610	
			MX7821T			700	

TIMING CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0V or -5V, Unipolar or Bipolar Input Range, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC2}	t_{READ2}	T_A = +25°C (Figure 4)				65	ns
		$T_A = T_{MIN}$ to T_{MAX} (Figure 4)	MX7821B/K			75	
			MX7821T			85	
Data-Access Time (WR-RD Mode) (Note 5)	t_{ACC2}	T_A = +25°C, C_L = 20pF (Figure 4) (Note 3)				65	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF (Note 3)	MX7821B/K			75	
			MX7821T			85	
		T_A = +25°C, C_L = 100pF (Figure 4)				90	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF (Figure 4)	MX7821B/K			110	
			MX7821T			130	
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)	t_{IHWR}	T_A = +25°C, C_L = 50pF				80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MX7821B/K			100	
			MX7821T			120	
Data-Access Time After $\overline{INT}$ (Stand-Alone Operation) (Note 5)	t_{ID}	T_A = +25°C, C_L = 20pF (Note 3)				30	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF (Note 3)	MX7821B/K			35	
			MX7821T			40	
		T_A = +25°C, C_L = 100pF				45	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF	MX7821B/K			60	
			MX7821T			70	

Note 3: Guaranteed by design.
Note 4: C_L = 50pF and R_L = 5kΩ pull-up resistor.
Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.
Note 6: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

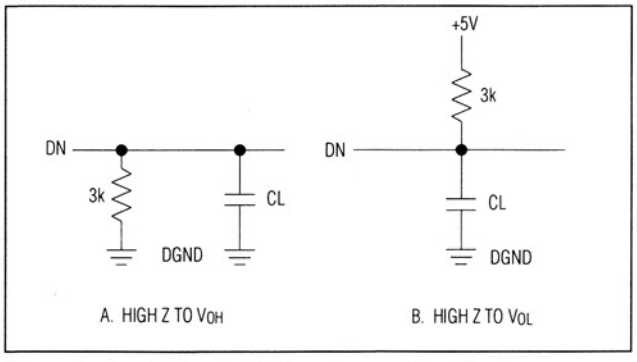


Figure 1. Load Circuits for Data-Access Time Test

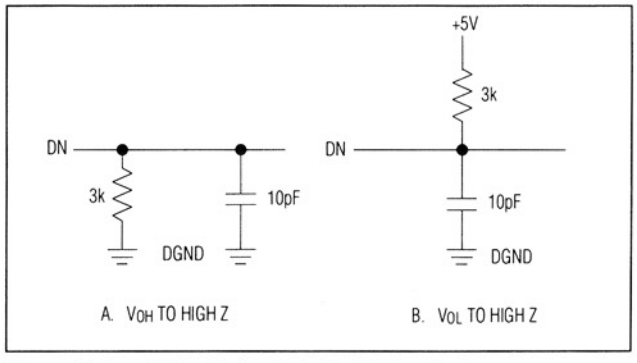


Figure 2. Load Circuits for Data-Hold Time Test

660ns µP-Compatible, 8-Bit ADC with Track/Hold

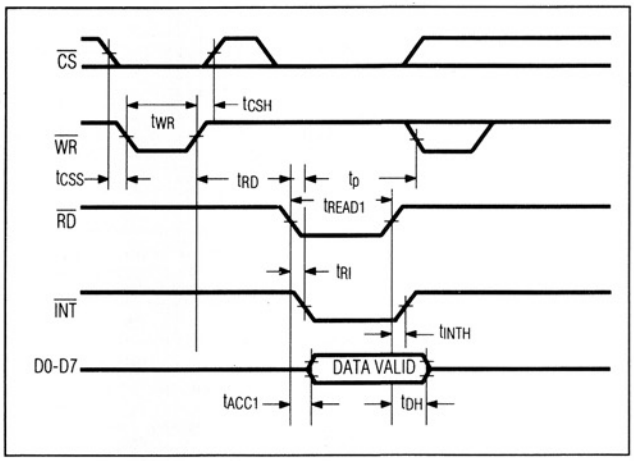


Figure 3. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

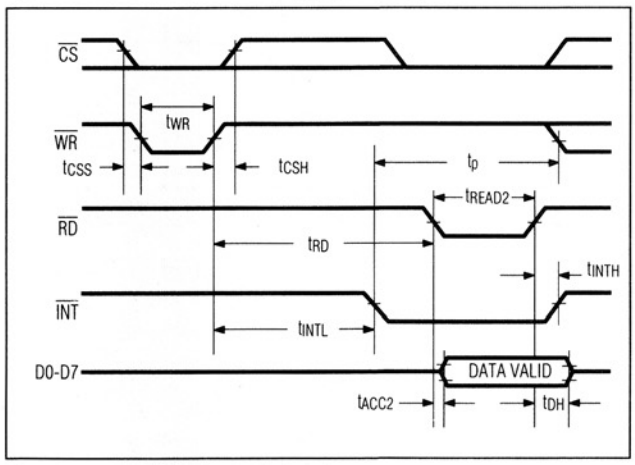


Figure 4: WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

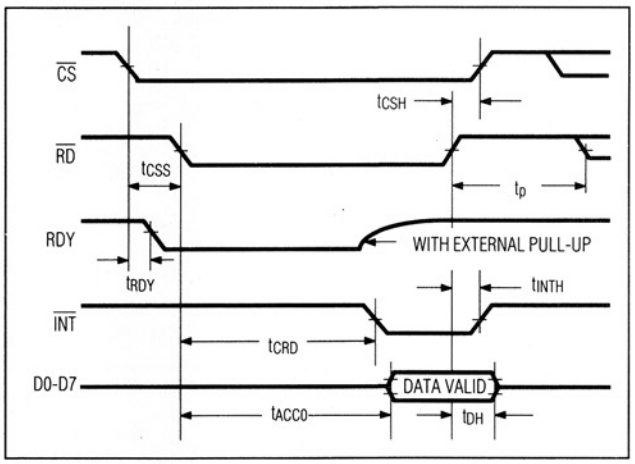


Figure 5. RD Mode

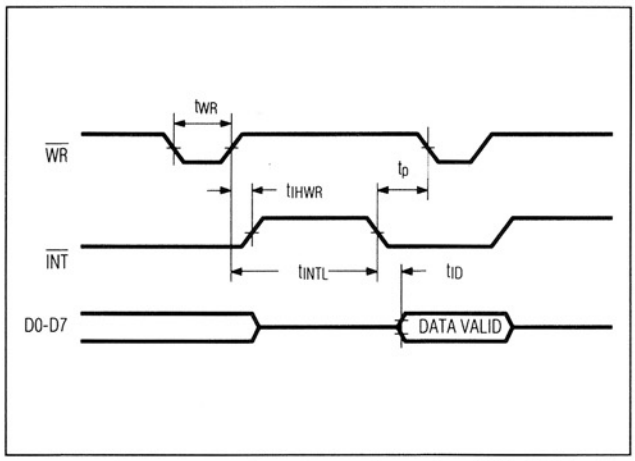
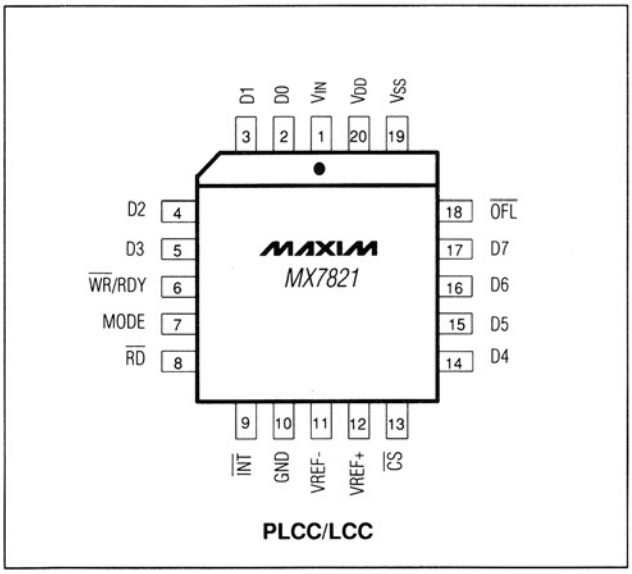


Figure 6. WR-RD Mode Stand-Alone Operation ($\overline{CS} = \overline{RD} = 0$)

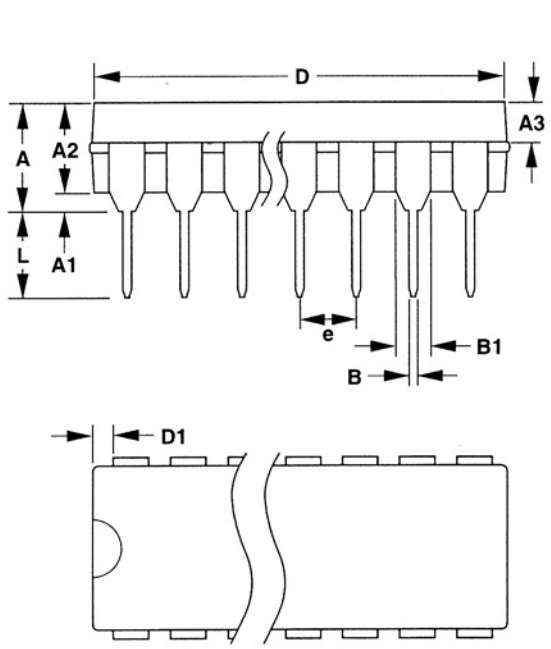
Pin Configurations (continued)



For application information, refer to the MX7820 data sheet.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

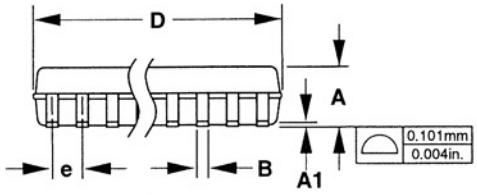


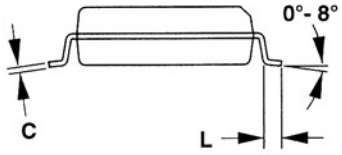
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

**Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)**

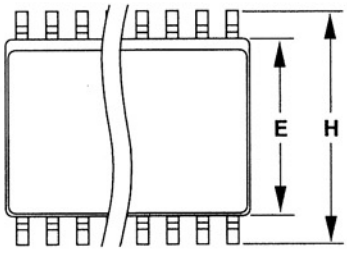
PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



**Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)**

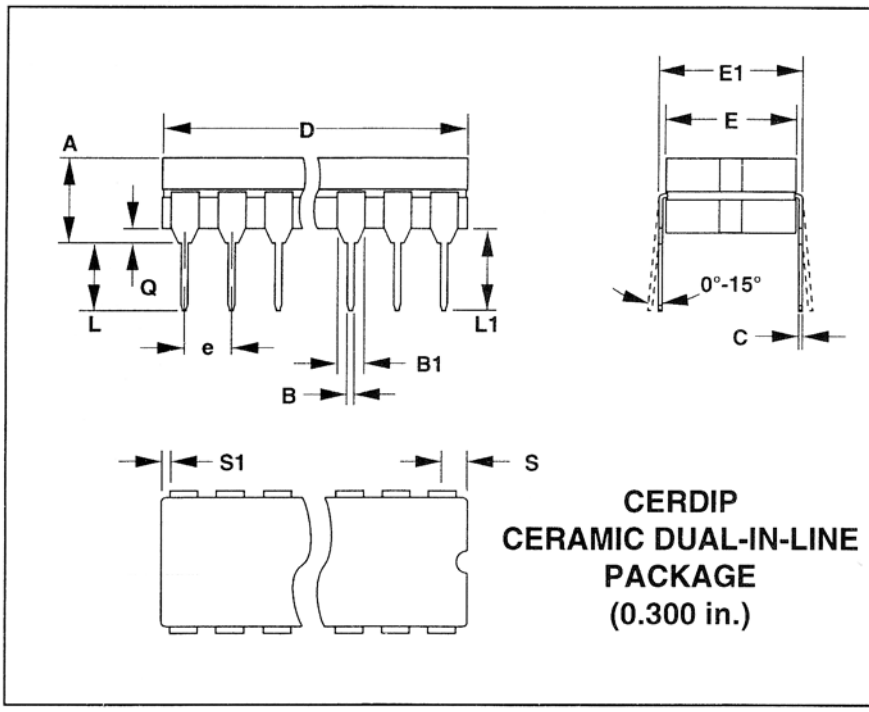
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

660ns µP-Compatible, 8-Bit ADC with Track/Hold

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A

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