RE46C311/2

Low-Input Leakage, Rail-to-Rail Input/Output Op Amps

Features

- Low Quiescent Current: 600 nA/Amplifier (typical)
- Rail-to-Rail Input/Output
- Gain Bandwidth Product: 10 kHz (typical)
- Wide Supply Voltage Range: 1.8V to 5.5V
- Unity Gain Stable
- Available in Single and Dual Configurations
- Temperature Ranges: -10°C to +60°C

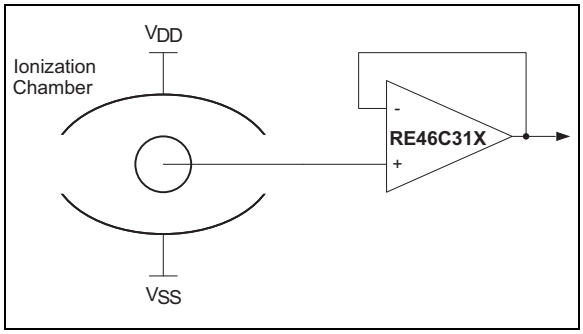
Applications

- Ionization Smoke Detectors
- Low Leakage High-Impedance Input Circuits
- Battery-Powered Circuits

Design Aids

- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



Description

The RE46C311/2 family of operational amplifiers (op amps) from Microchip Technology Inc. operate with a single-supply voltage as low as 1.8V, while drawing less than 1 µA (maximum) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

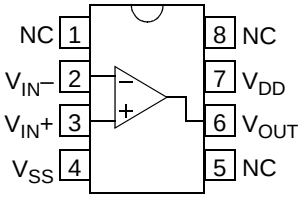
The RE46C311/2 amplifiers have a gain-bandwidth product of 10 kHz (typical) and are unity gain stable. These specifications make these op amps appropriate for low-frequency applications, such as ionization smoke detectors and sensor conditioning.

The RE46C311/2 family operational amplifiers are offered in single (RE46C311), and dual (RE46C312) configurations.

Package Types

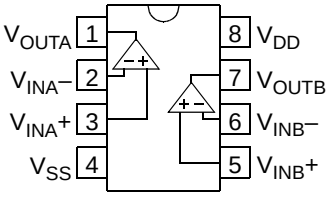
RE46C311

PDIP, SOIC



RE46C312

PDIP, SOIC



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.0V
Current at Input Pins .....±2 mA
All Inputs and Outputs..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....–65°C to +150°C
Junction Temperature.....+150°C
ESD protection on all pins (HBM; MM) ..... ≥ 4 kV; 400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1, Rail-to-Rail Input**.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and R_L = 1 MΩ to V_L (refer to Figure 1-1 and Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3	—	+3	mV	
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	T_A= -10°C to +60°C
Power Supply Rejection	PSRR	70	76	—	dB	$V_{CM} = V_{SS}$
Input Leakage Current and Impedance						
Input Leakage Current	I_{L1}	-0.75	—	0.75	pA	Non Inverting Input only, $V_{IN} = V_{DD}$ or V_{SS}
		—	3.5	6		T_A = +60°C
Input Leakage Current	I_{L2}	-100	—	100	nA	Inverting input only
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common-Mode Input Range	V_{CMR}	V_{SS}	—	V_{DD}	V	
Common-Mode Rejection Ratio	CMRR	62	86	—	dB	V_{DD} = 5V, V_{CM} = 0V to 5.0V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	85	115	—	dB	R_L = 50 kΩ to V_L, V_{OUT} = 0.1V to V_{DD}-0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} - 10	mV	R_L = 50 kΩ to V_L, 0.5V input overdrive
Output Short Circuit Current	I_{SC}	—	5	—	mA	V_{DD} = 1.8V
		—	27	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.3	0.6	1.0	µA	I_O = 0

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L, and C_L = 60 pF (refer to Figure 1-1 and Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	10	—	kHz	
Slew Rate	SR	—	3.0	—	V/ms	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Noise						
Input Voltage Noise	E_{ni}	—	5.0	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_{ni}	—	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-10	—	+60	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-1 and Figure 1-2. The bypass capacitors are laid out according to the rules discussed in **Section 4.5, Supply Bypass**.

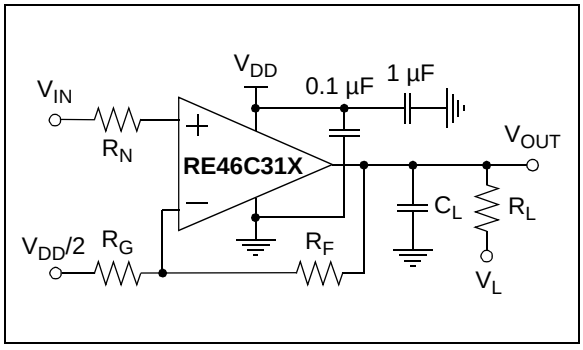


FIGURE 1-1: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

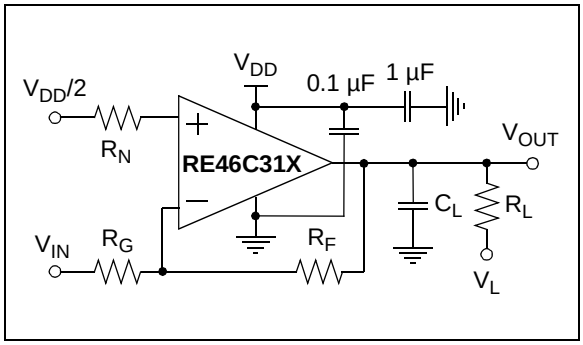


FIGURE 1-2: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

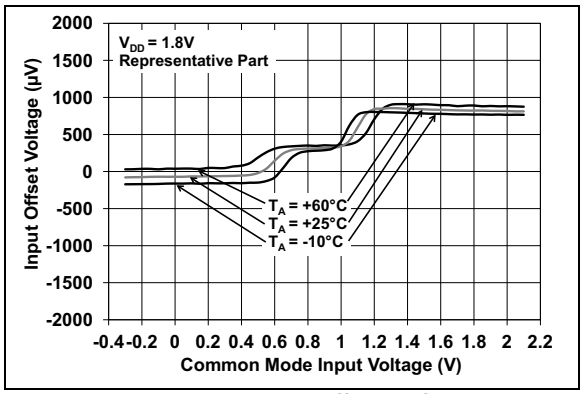


FIGURE 2-1: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 1.8V.*

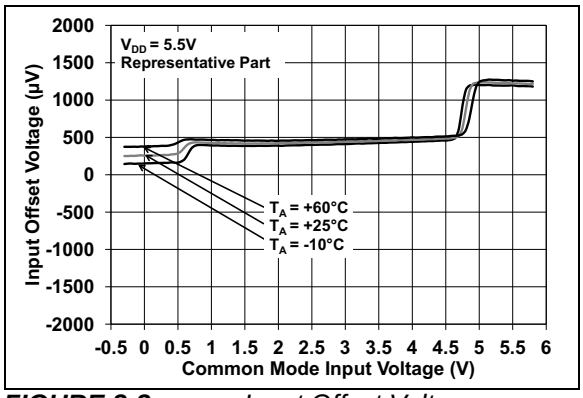


FIGURE 2-2: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

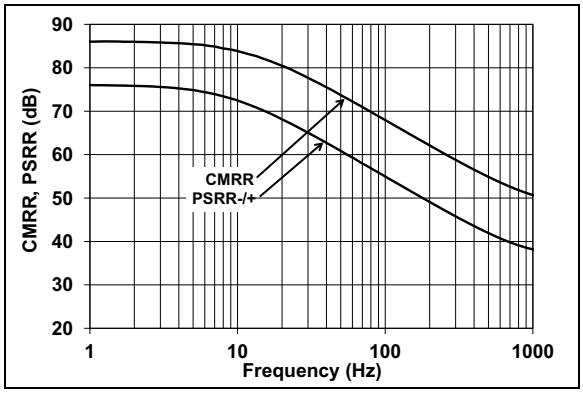


FIGURE 2-3: *CMRR, PSRR vs. Frequency.*

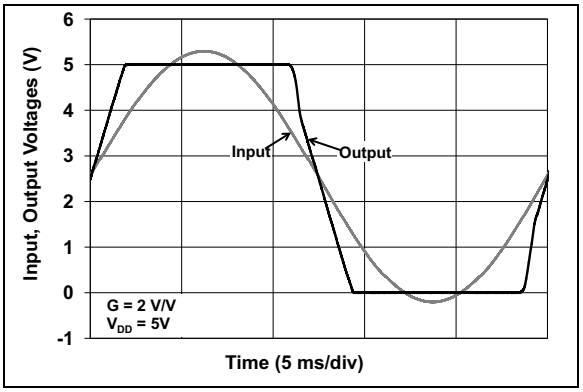


FIGURE 2-4: *The RE46C311/2 Family Shows No Phase Reversal.*

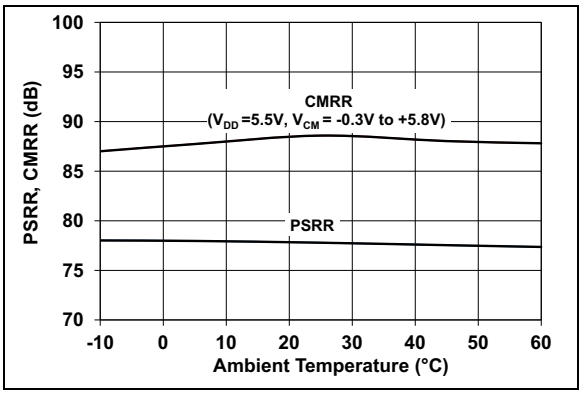


FIGURE 2-5: *CMRR, PSRR vs. Ambient Temperature.*

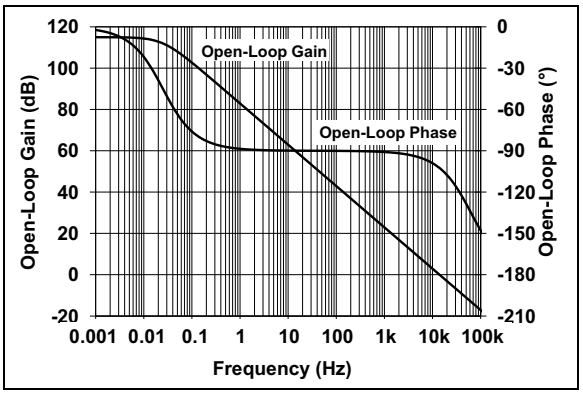


FIGURE 2-6: *Open-Loop Gain, Phase vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

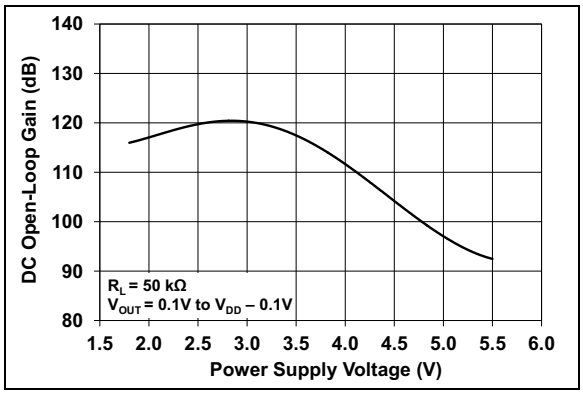


FIGURE 2-7: *DC Open-Loop Gain vs. Power Supply Voltage.*

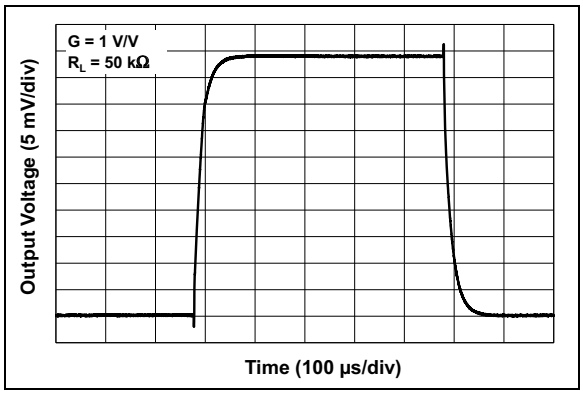


FIGURE 2-10: *Small Signal Non-inverting Pulse Response.*

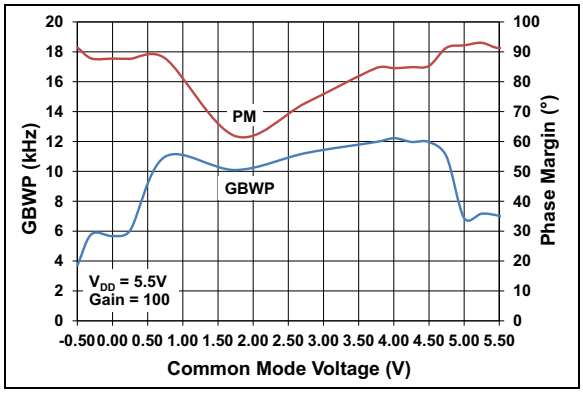


FIGURE 2-8: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

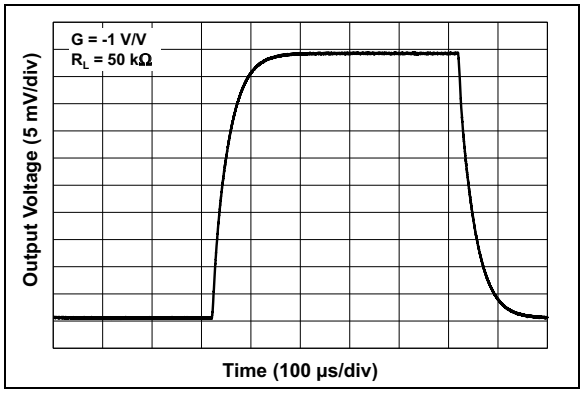


FIGURE 2-11: *Small Signal Inverting Pulse Response.*

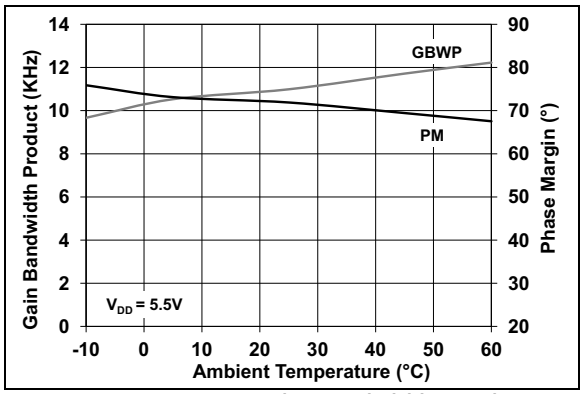


FIGURE 2-9: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 5.5V.*

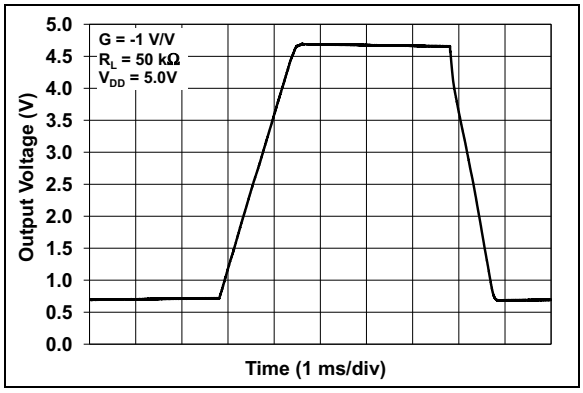


FIGURE 2-12: *Large Signal Non-inverting Pulse Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, and C_L = 60 pF.

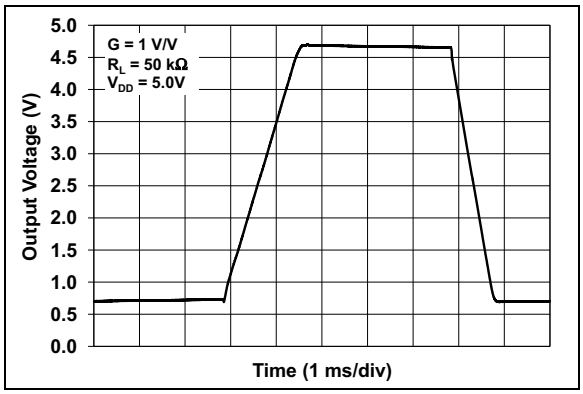


FIGURE 2-13: *Large Signal Inverting Pulse Response.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

RE46C311	RE46C312	Symbol	Description
PDIP, SOIC	PDIP, SOIC,		
6	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
2	2	V_{IN}–, V_{INA}–	Inverting Input (op amp A)
3	3	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
7	8	V_{DD}	Positive Power Supply
—	5	V_{INB}+	Non-inverting Input (op amp B)
—	6	V_{INB}–	Inverting Input (op amp B)
—	7	V_{OUTB}	Analog Output (op amp B)
4	4	V_{SS}	Negative Power Supply
1, 5, 8	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias and leakage currents.

3.3 Power Supply Pins

The positive power supply pin (V_{DD}) is 1.8V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

4.0 APPLICATIONS INFORMATION

The RE46C311/2 family of op amps is manufactured using a state of the art CMOS process. These op amps are unity gain stable and suitable for a wide range of general purpose, low-power applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The RE46C311/2 op amps are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-4 shows an input voltage exceeding both supplies with no phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} or one diode drop above V_{DD}.

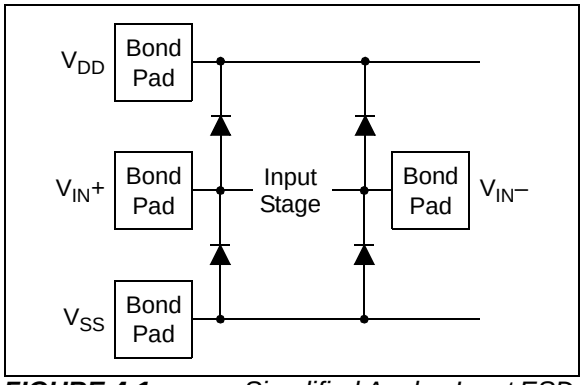


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see Absolute Maximum Ratings †).

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below V_{SS} or above V_{DD}. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the RE46C311/2 op amps uses two differential input stages in parallel. One operates at a low common mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to V_{DD} and down to V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS}$ and V_{DD} to ensure proper operation.

There are two transitions in input behavior as V_{CM} is changed. The first occurs when V_{CM} is near V_{SS} + 0.4V, and the second occurs when V_{CM} is near V_{DD} – 0.5V (see Figure 2-1 and Figure 2-2). For the best distortion performance with non-inverting gains, avoid these regions of operation.

4.2 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the RE46C311/2 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load condition. Thus, the output voltage swings to within 10 mV of either supply rail with a 50 kΩ load to $V_{DD}/2$. Figure 2-4 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} condition in the specification table.

4.3 Output Loads and Battery Life

The RE46C311/2 op amp family has outstanding quiescent current, which supports battery-powered applications.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply current to increase by 25 µA, depleting the battery 43 times as fast as I_Q (0.6 µA, typical) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ ($1/2\pi fC$) to a 100 Hz sine wave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sine wave (1.77 V_{rms}), under these conditions, is:

EQUATION 4-1:

$$\begin{aligned} P_{Supply} &= (V_{DD} - V_{SS})\,(I_Q + V_{L(p\text{-}p)}\,f\,C_L) \\ &= (5V)(0.6\,\mu A + 5.0V_{p\text{-}p} \cdot 100Hz \cdot 0.1\mu F) \\ &= 3.0\,\mu W + 50\,\mu W \end{aligned}$$

This will drain the battery 17 times as fast as I_Q alone.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer (G = +1) is the most sensitive to capacitive loads, although all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-2) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

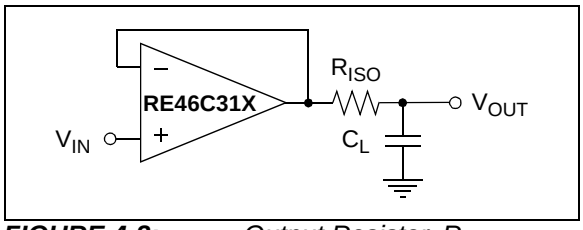


FIGURE 4-2: *Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.*

Figure 4-3 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

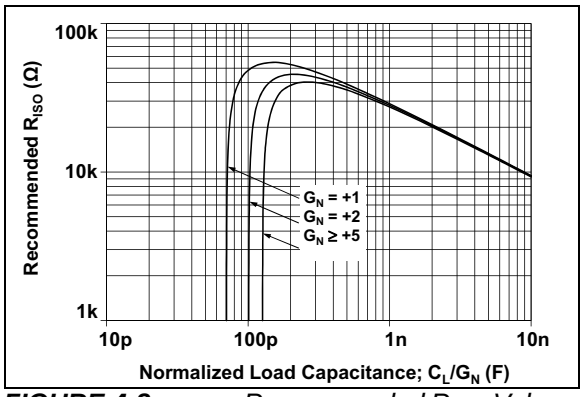


FIGURE 4-3: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable.

4.5 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required for most applications and can be shared with nearby analog parts.

4.6 Unused Op Amps

An unused op amp in a dual package (RE46C312) should be configured as shown in Figure 4-4. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

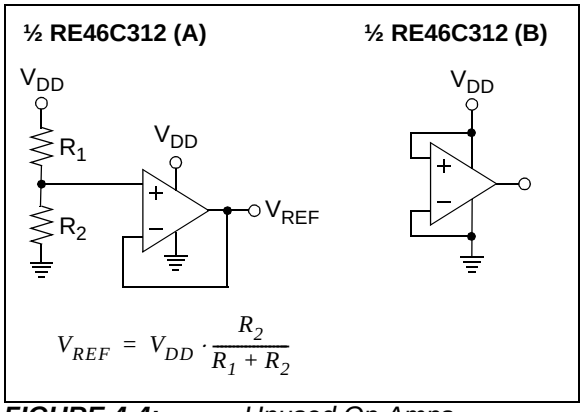


FIGURE 4-4: *Unused Op Amps.*

4.7 PCB Surface Leakage

In applications where low input bias current is critical, printed circuit board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the RE46C311/2 family's leakage current at +25°C.

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-5 shows an example of this type of layout.

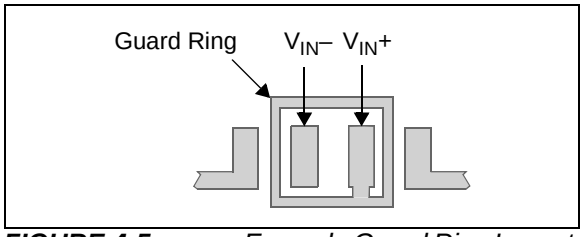


FIGURE 4-5: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common mode input voltage.
2. Inverting Gain and Transimpedance Gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.8 Application Circuits

4.8.1 INSTRUMENTATION AMPLIFIER

The RE46C311/2 op amp is well suited for conditioning sensor signals in battery-powered applications. Figure 4-6 shows a two op amp instrumentation amplifier, using the RE46C312, that works well for applications requiring rejection of Common mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low impedance source. In single supply applications, V_{REF} is typically V_{DD}/2.

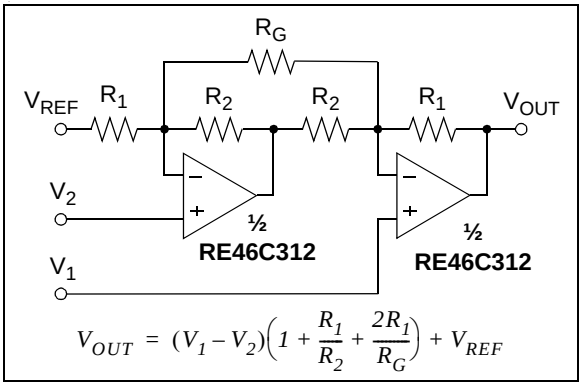


FIGURE 4-6: *Two Op Amp Instrumentation Amplifier.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the RE46C311/2 family of op amps.

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs.

Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase, and sampling of Microchip parts.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Three of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*
- **P/N MCP651EV-VOS:** *MCP651 Input Offset Evaluation Board*

5.3 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications",* DS00722

AN723: *"Operational Amplifier AC Specifications and Applications",* DS00723

AN884: *"Driving Capacitive Loads With Op Amps",* DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

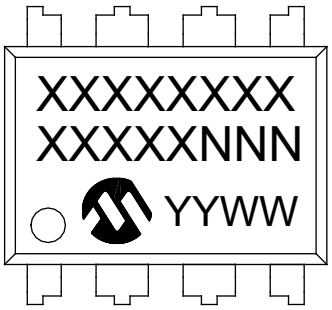
These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

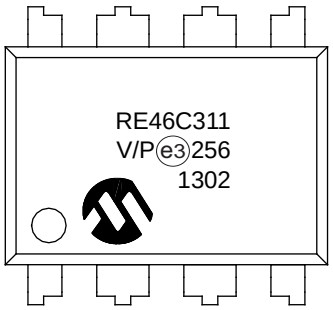
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

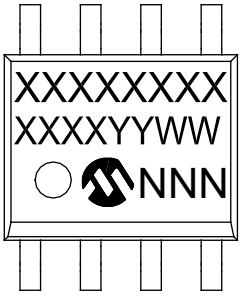
8-Lead PDIP (300 mil)



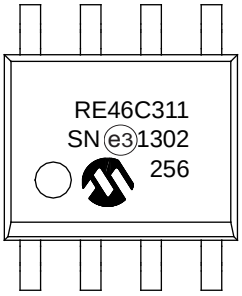
Example



8-Lead SOIC (3.90 mm)



Example

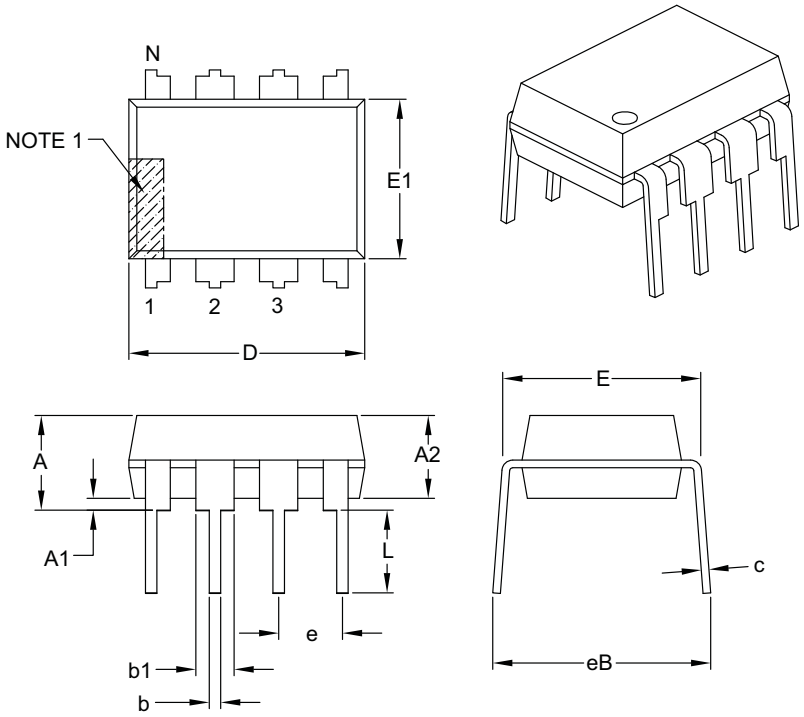


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	(e3)	Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

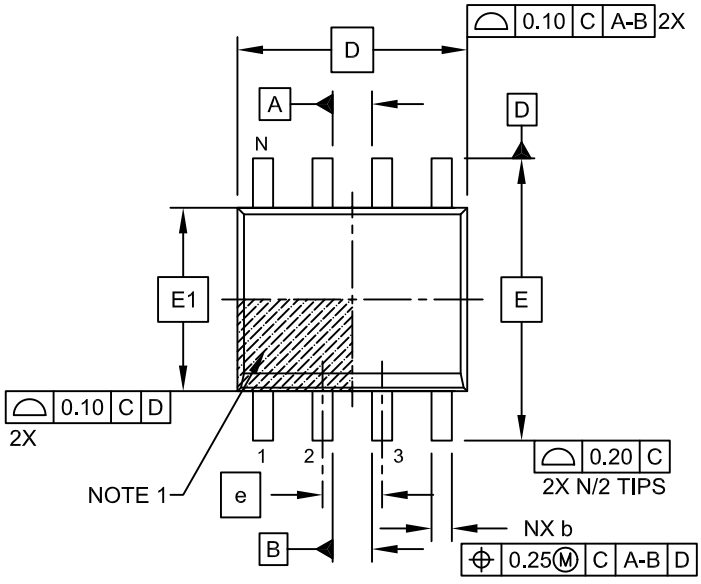
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

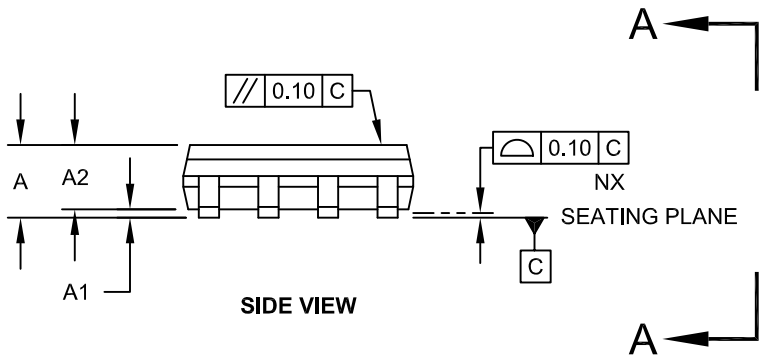
Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

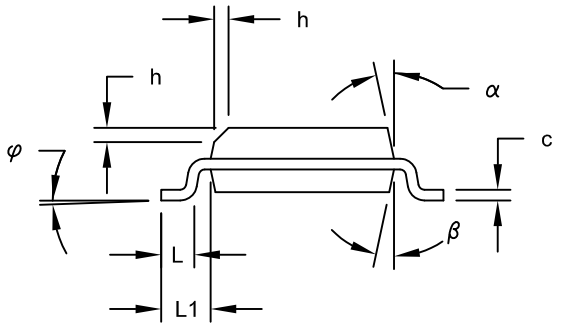
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

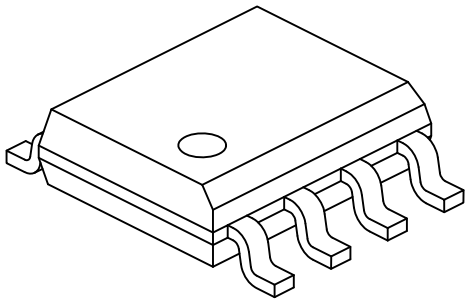


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

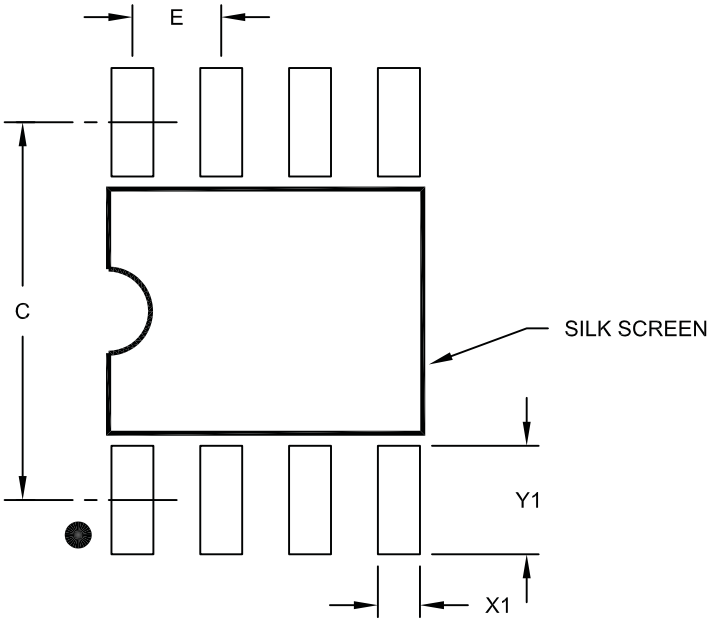
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision A (May 2013)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	X
Device	Package	Number of Pins	Lead Free/ Tape and Reel

Device:	RE46C311:	Single Low-Input Leakage Op Amp
	RE46C312:	Dual Low-Input Leakage Op Amp
Package:	E =	Plastic Dual In-Line (300 mil Body), 8-lead (PDIP)
	S =	Small Plastic Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)

Examples:

a)	RE46C311E8F:	8LD PDIP package, RoHS Compliant
b)	RE46C311S8F:	8LD SOIC package, RoHS Compliant
c)	RE46C311S8TF:	8LD SOIC package, Tape and Reel
a)	RE46C312E8F:	8LD PDIP package, RoHS Compliant
b)	RE46C312S8F:	8LD SOIC package, RoHS Compliant
c)	RE46C312S8TF:	8LD SOIC package, Tape and Reel

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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