

# 74HC377; 74HCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 6 — 5 August 2024

Product data sheet

## 1. General description

The 74HC377; 74HCT377 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and data enable (E) inputs. When E is LOW, the outputs Qn assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. Input E must be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Input levels:
  - For 74HC377: CMOS level
  - For 74HCT377: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74HC377D</a> <a href="#">74HCT377D</a>	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<a href="#">SOT163-1</a>
<a href="#">74HC377PW</a> <a href="#">74HCT377PW</a>	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	<a href="#">SOT360-1</a>

## 4. Functional diagram

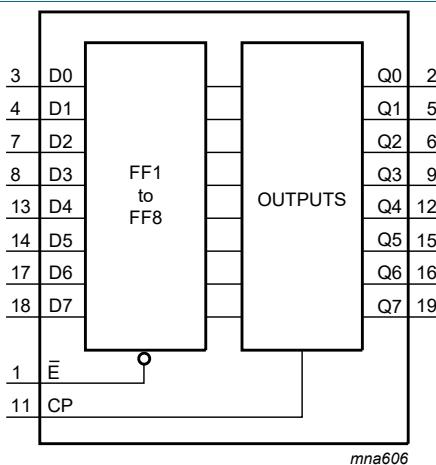


Fig. 1. Functional diagram

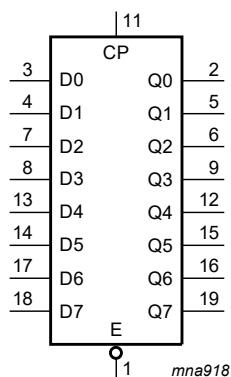


Fig. 2. Logic symbol

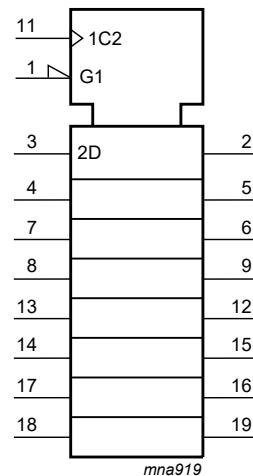


Fig. 3. IEC logic symbol

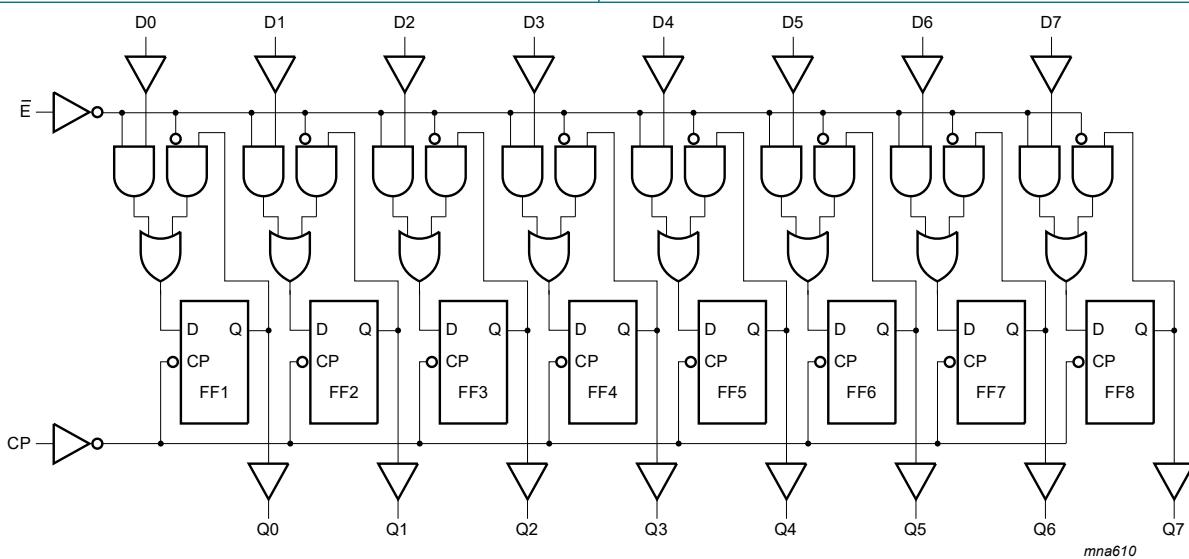
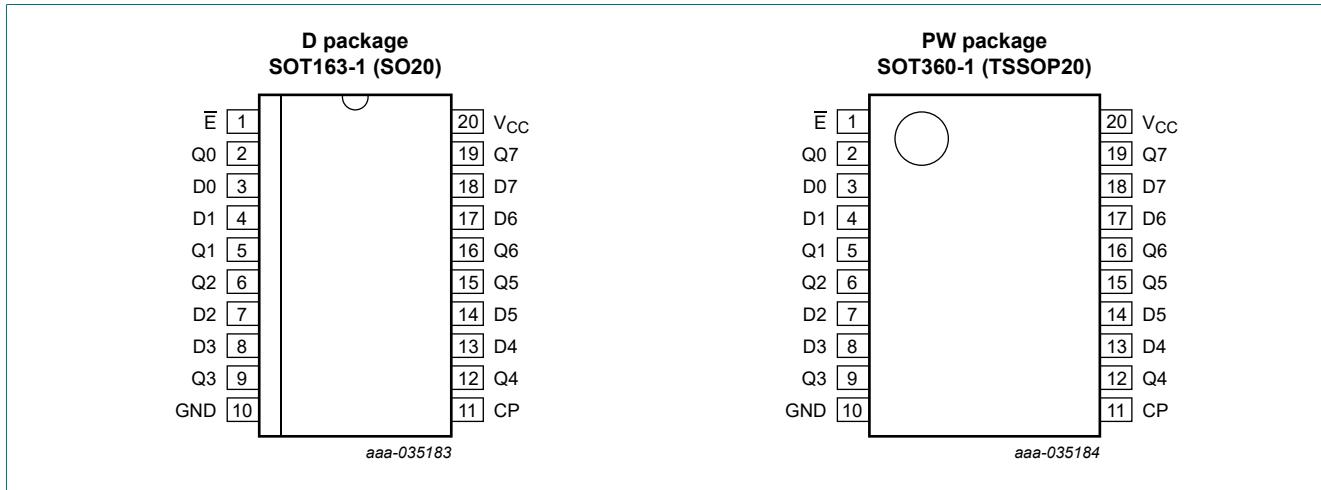


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Ē	1	data enable input (active LOW)
Q <sub>0</sub> , Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub> , Q <sub>4</sub> , Q <sub>5</sub> , Q <sub>6</sub> , Q <sub>7</sub>	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D <sub>0</sub> , D <sub>1</sub> , D <sub>2</sub> , D <sub>3</sub> , D <sub>4</sub> , D <sub>5</sub> , D <sub>6</sub> , D <sub>7</sub>	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs			Outputs
	CP	Ē	D <sub>n</sub>	
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package: P<sub>tot</sub> derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P<sub>tot</sub> derates linearly with 10.0 mW/K above 100 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC377			74HCT377			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC377</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT377</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 5.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$\bar{E}$ input	-	150	540	-	675	-	735	$\mu\text{A}$
		CP input	-	50	180	-	225	-	245	$\mu\text{A}$
		Dn input	-	20	72	-	90	-	98	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see Fig. 7.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC377</b>										
$t_{pd}$	propagation delay	CP to Qn; see Fig. 5 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	44	160	-	200	-	240	ns
		$V_{CC} = 4.5 \text{ V}$	-	16	32	-	40	-	48	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	13	-	-	-	-	-	-
		$V_{CC} = 6.0 \text{ V}$	-	13	27	-	34	-	41	ns
$t_t$	transition time	Qn output; see Fig. 5 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
$t_w$	pulse width	CP input HIGH or LOW; see Fig. 5								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
$t_{su}$	set-up time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	60	14	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	5	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	4	-	13	-	15	-	ns
		E to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	60	6	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	2	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	2	-	13	-	15	-	ns
$t_h$	hold time	Dn to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	3	-8	-	3	-	3	-	ns
		$V_{CC} = 4.5 \text{ V}$	3	-3	-	3	-	3	-	ns
		$V_{CC} = 6.0 \text{ V}$	3	-2	-	3	-	3	-	ns
		E to CP; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	4	-3	-	4	-	4	-	ns
		$V_{CC} = 4.5 \text{ V}$	4	-1	-	4	-	4	-	ns
		$V_{CC} = 6.0 \text{ V}$	4	-1	-	4	-	4	-	ns
$f_{max}$	maximum frequency	CP input; see Fig. 5								
		$V_{CC} = 2.0 \text{ V}$	6	23	-	5	-	4	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	70	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	77	-	-	-	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	35	83	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	[3]	-	20	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT377</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Fig. 5</a> [1]								
		$V_{CC} = 4.5 \text{ V}$	-	17	32	-	40	-	48	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	-	-	-	-	ns
$t_t$	transition time	Qn output; see <a href="#">Fig. 5</a> [2]								
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
$t_w$	pulse width	CP input; see <a href="#">Fig. 5</a>								
		$V_{CC} = 4.5 \text{ V}$	20	8	-	25	-	30	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Fig. 6</a>								
		$V_{CC} = 4.5 \text{ V}$	12	4	-	15	-	18	-	ns
		$\bar{E}$ to CP; see <a href="#">Fig. 6</a>								
		$V_{CC} = 4.5 \text{ V}$	22	12	-	28	-	33	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Fig. 6</a>								
		$V_{CC} = 4.5 \text{ V}$	2	-4	-	2	-	2	-	ns
		$\bar{E}$ to CP; see <a href="#">Fig. 6</a>								
		$V_{CC} = 4.5 \text{ V}$	3	-2	-	3	-	3	-	ns
$f_{max}$	maximum frequency	CP input; see <a href="#">Fig. 5</a>								
		$V_{CC} = 4.5 \text{ V}$	27	48	-	22	-	18	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	53	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$ [3]	-	20	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

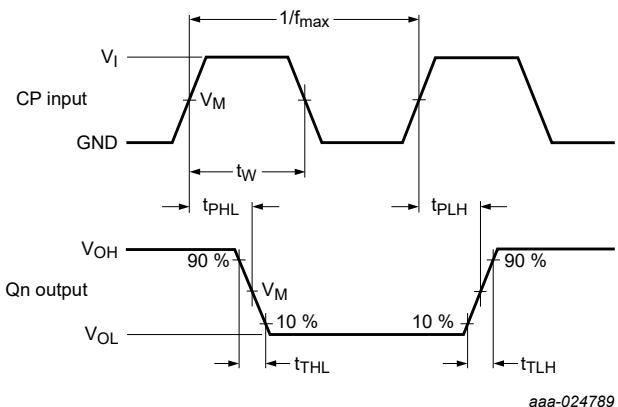
$f_o$  = output frequency in MHz;

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs};$$

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V.

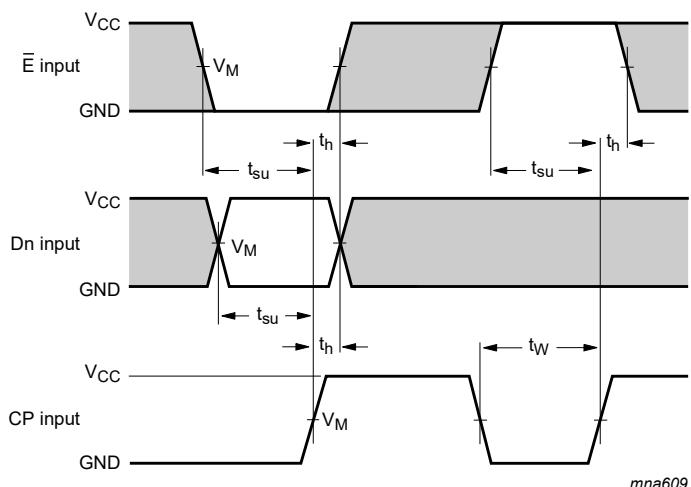
## 10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency**



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

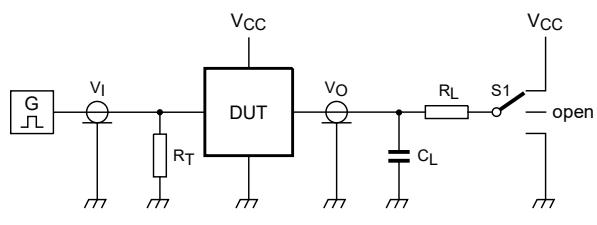
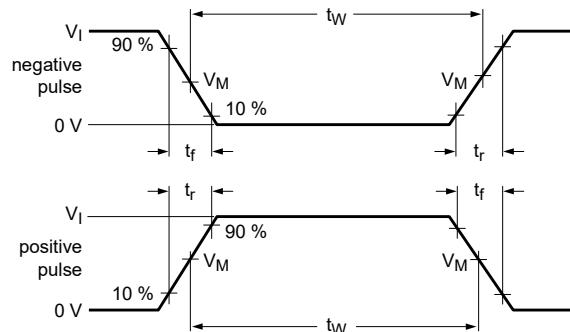
$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 6. Data set-up and hold times data input (Dn)

**Table 8. Measurement points**

Type	Input		Output
	$V_I$	$V_M$	
74HC377	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT377	3 V	1.3 V	1.3 V

## Octal D-type flip-flop with data enable; positive-edge trigger



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator; $C_L$  = Load capacitance including jig and probe capacitance; $R_L$  = Load resistance;

S1 = Test selection switch.

Fig. 7. Test circuit for measuring switching times

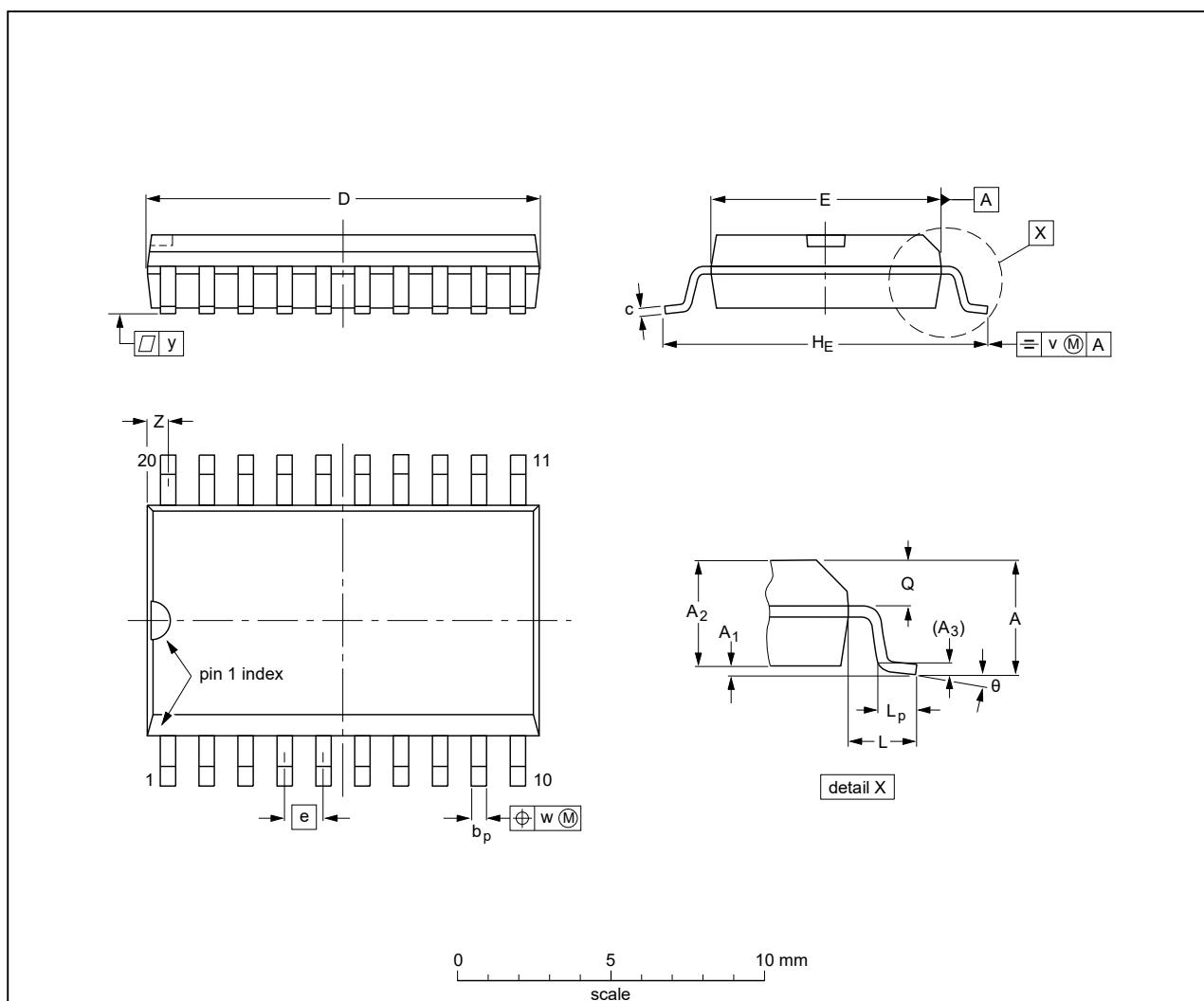
Table 9. Test data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
74HC377	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open
74HCT377	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open

## 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ	
mm	2.65	0.3	2.45	0.25	0.49	0.32	13.0	7.6	1.27	10.65	1.4	1.1	1.1	0.25	0.25	0.1	0.9	8°	
inches	0.1	0.012	0.096	0.01	0.019	0.013	0.51	0.30	0.05	0.419	0.055	0.043	0.043	0.01	0.01	0.004	0.035	0.016	0°

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

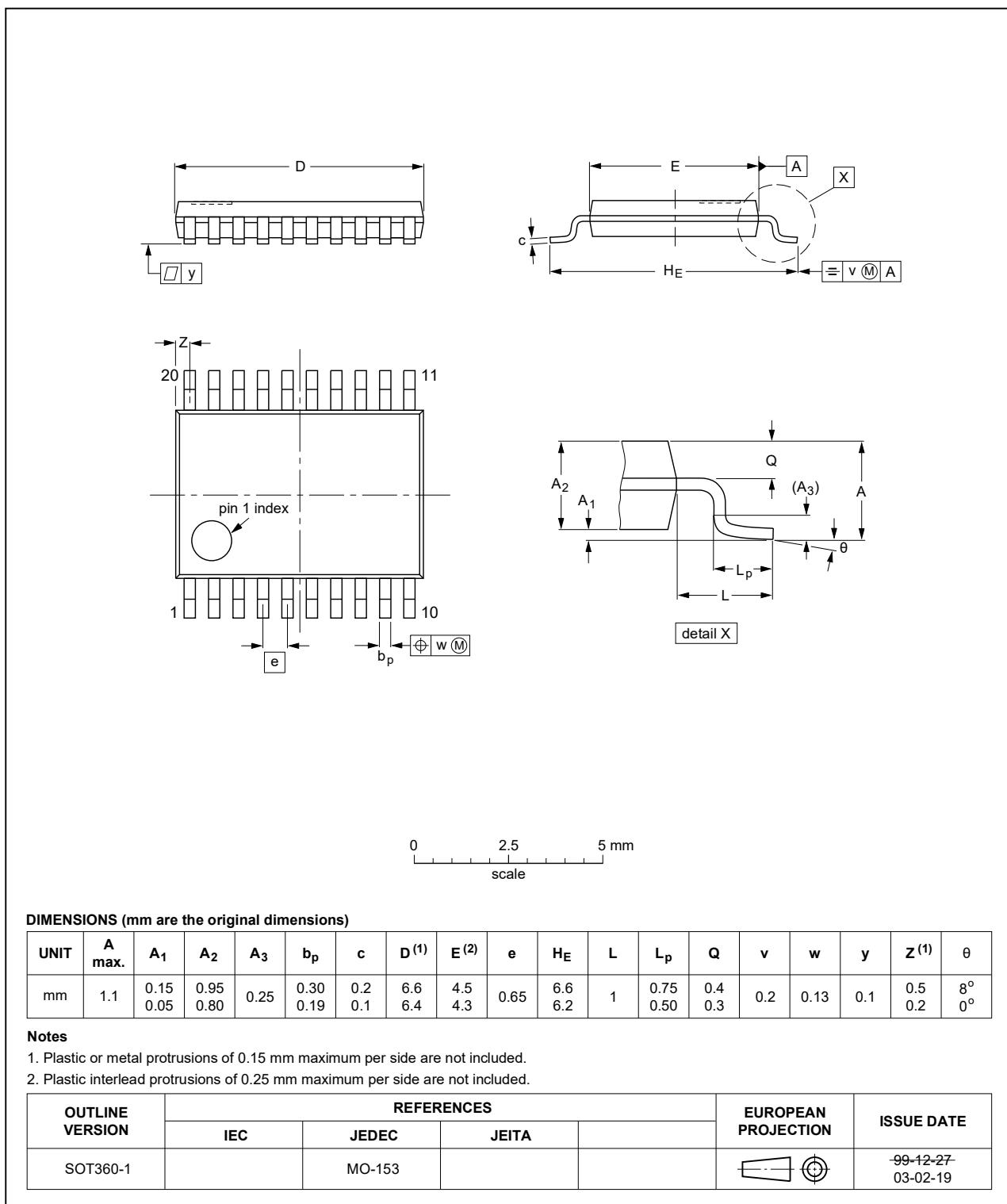


Fig. 9. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT377 v.6	20240805	Product data sheet	-	74HC_HCT377 v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74HC_HCT377 v.5	20210225	Product data sheet	-	74HC_HCT377 v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li>Type numbers 74HC377DB and 74HCT377DB (SOT339-1 / SSOP20) removed.</li> </ul>			
74HC_HCT377 v.4	20160224	Product data sheet	-	74HC_HCT377 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC377N and 74HCT377N (SOT146-1) removed.</li> </ul>			
74HC_HCT377 v.3	20130925	Product data sheet	-	74HC_HCT377_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT377_CNV v.2	19901227	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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