

## TFT-LCD I<sup>2</sup>C Programmable VCOM Calibrator

The V<sub>COM</sub> voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external V<sub>COM</sub> buffer amplifier. The desired V<sub>COM</sub> setting is loaded from an external source via a standard 2-wire I<sup>2</sup>C serial interface. At power up, the part automatically comes up at the last programmed EEPROM setting.

An external resistor attaches to the SET pin and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45041 is available in an 8 Ld 3mm x 3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

An evaluation kit complete with software to control the DCP from a computer is available. Reference Application Note [AN1275](#) and "Ordering Information".

## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45041IRZ	041Z	0 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL45041EVAL1Z	Evaluation Board			

### NOTE:

1. Add "-T\*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL45041](#). For more information on MSL, please see Technical Brief [TB363](#).

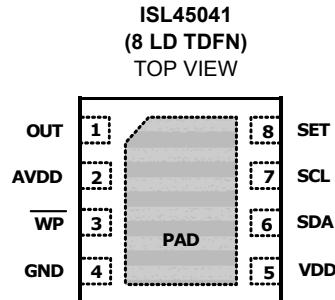
## Features

- 128-Step Adjustable Sink Current Output
- 2.25V to 3.6V Logic Supply Voltage Operating Range (2.6V Minimum Programming Voltage)
- 4.5V to 18V Analog Supply Voltage Operating Range (10.8V Minimum Programming Voltage)
- I<sup>2</sup>C Interface With Addresses 100111x and 100110x
- On-Chip 7-Bit EEPROM
- Output Adjustment SET Pin
- Output Guaranteed Monotonic Over-Temperature
- Thin 8 Ld 3mm x 3mm DFN (0.8mm max)
- Pb-free (RoHS compliant)

## Applications

- LCD Panels

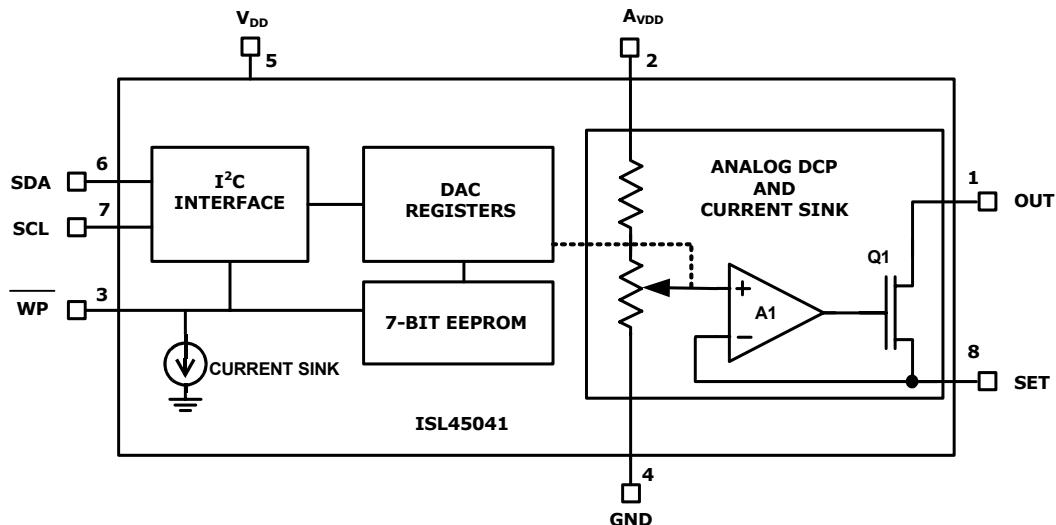
## Pinout



## Pin Descriptions

PIN	TYPE	PULL U/D	FUNCTION
OUT	Output		Adjustable Sink Current Output Pin. The current that sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maximum adjustable sink current setting.
AV <sub>DD</sub>	Supply		High-Voltage Analog Supply. Bypass to GND with 0.1μF capacitor.
WP	Input	Pull-Down	Write Protect. Active Low. To enable programming, connect to 0.7*V <sub>DD</sub> supply or greater. The WP pin is designed for static control. It has an internal pull-down current sink. To avoid the possibly over-writing the EEPROM contents, no frequency above 1Hz should be applied to this input. Care should be taken to avoid any glitches on the input. When removing or applying mechanical jumpers, always ensure the V <sub>DD</sub> power is off. A high to low transition on the WP pin results in the register contents being loaded with EEPROM data.
GND	Supply		Ground connection.
V <sub>DD</sub>	Supply		Digital power supply input. Bypass to GND with 0.1μF capacitor.
SDA	In/Out		I <sup>2</sup> C Serial Data Input and Output.
SCL	Input		I <sup>2</sup> C Clock Input
SET	Analog		Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AV <sub>DD</sub> /20) divided by RSET.

## Block Diagram



**Absolute Maximum Ratings**

V <sub>DD</sub> to GND	.....	+4V
Input Voltages to GND		
SET	.....	-0.3V to +4V
AV <sub>DD</sub>	.....	-0.3V to +20V
Output Voltages to GND		
OUT	.....	-0.3V to +AV <sub>DD</sub>
ESD Rating		
Human Body Model		
Device (Tested per JESD22-A114E)	.....	2kV
Input Pins (SCL, SDA) (Tested per JESD22-A114E)	.....	4kV

**Thermal Information**

Thermal Resistance (Typical)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
8 Ld TDFN Package (Notes 4, 5)	.....	53
Moisture Sensitivity (see Technical Brief TB363)		11
All Packages	.....	Level 2
Maximum Junction Temperature (Plastic Package)	.....	+150°C
Maximum Storage Temperature Range	.....	-65°C to +150°C
Pb-free reflow profile	.....	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**Operating Conditions**

Temperature Range	.....	0°C to +85°C
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*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

## NOTES:

4. θ<sub>JA</sub> is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ<sub>JC</sub>, the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications** Test Conditions: V<sub>DD</sub> = 3.3V, AV<sub>DD</sub> = 18V, R<sub>SET</sub> = 5kΩ, R<sub>1</sub> = 10kΩ, R<sub>2</sub> = 10kΩ; (See Figure 1) Unless Otherwise Specified. Typicals are at T<sub>A</sub> = +25°C. **Boldface limits apply over the operating temperature range, 0°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
<b>POWER SUPPLY CHARACTERISTICS</b>						
V <sub>DD</sub> Supply Range Supporting EEPROM Programming	V <sub>DD</sub>		<b>2.6</b>		<b>3.6</b>	V
AV <sub>DD</sub> Supply Range Supporting EEPROM Programming	AV <sub>DD</sub>		<b>10.8</b>		<b>18</b>	V
V <sub>DD</sub> Supply Range for Wide-Supply Operation (not supporting EEPROM programming)	V <sub>DD</sub>		<b>2.25</b>		<b>3.6</b>	V
AV <sub>DD</sub> Supply Range for Wide-Supply Operation (not supporting EEPROM programming)	AV <sub>DD</sub>	2.6V < V <sub>DD</sub> < 3.6V	<b>4.5</b>		<b>18</b>	V
		2.25V < V <sub>DD</sub> < 2.6V	<b>4.5</b>		<b>13</b>	V
V <sub>DD</sub> Supply Current	I <sub>DD</sub>	(Note 7)			<b>65</b>	μA
AV <sub>DD</sub> Supply Current	I <sub>AVDD</sub>	(Note 8)			<b>38</b>	μA
<b>DC CHARACTERISTICS</b>						
SET Voltage Resolution	SET <sub>VR</sub>		<b>7</b>	7	<b>7</b>	Bits
SET Differential Nonlinearity	SET <sub>DN</sub>	Monotonic Over-Temperature			<b>±1</b>	LSB
SET Zero-Scale Error	SET <sub>ZSE</sub>				<b>±3</b>	LSB
SET Full-Scale Error	SET <sub>FSE</sub>				<b>±8</b>	LSB
SET Current (R <sub>SET</sub> = 24.9kΩ and AV <sub>DD</sub> = 10V)	I <sub>SET</sub>	Through R <sub>SET</sub> (Note 11)		20		μA
SET External Resistance	SET <sub>ER</sub>	To GND, AV <sub>DD</sub> = 18V	<b>5</b>		<b>200</b>	kΩ
		To GND, AV <sub>DD</sub> = 4.5V	<b>2.25</b>		<b>45</b>	kΩ
		To GND, AV <sub>DD</sub> = 15V, V <sub>DD</sub> = 3V V <sub>OUT</sub> > 2.5V (Note 12)	<b>1.0</b>		<b>200</b>	kΩ
AV <sub>DD</sub> to SET Voltage Attenuation	AV <sub>DD</sub> to SET	(Note 9)		1:20		V/V
OUT Settling Time	OUT <sub>ST</sub>	To ±0.5 LSB Error Band (Note 9)		8		μs
OUT Voltage Range	V <sub>OUT</sub>		<b>V<sub>SET</sub>+0.5V</b>		<b>13</b>	V
SET Voltage Drift	SET <sub>VD</sub>	25°C < T <sub>A</sub> < 55°C (Note 9)		<10		mV

**Electrical Specifications** Test Conditions:  $V_{DD} = 3.3V$ ,  $AV_{DD} = 18V$ ,  $R_{SET} = 5k\Omega$ ,  $R1 = 10k\Omega$ ,  $R2 = 10k\Omega$ ; (See Figure 1) Unless Otherwise Specified. Typicals are at  $T_A = +25^\circ C$ . **Boldface limits apply over the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SDA, SCL Input Logic High	$I^2CV_{IH}$		<b>0.7*V<sub>DD</sub></b>			V
SDA, SCL Input Logic Low	$I^2CV_{IL}$				<b>0.55</b>	V
SDA, SCL Hysteresis		(Note 9)		260		mV
SDA Output Logic High	$VOH_S$		<b>V<sub>DD</sub> - 0.4</b>			V
SDA Output Logic Low	$VOL_S$	@ 3mA			<b>0.4</b>	V
WP Input Logic High	$V_{IH}$		<b>0.7*V<sub>DD</sub></b>			V
WP Input Logic Low	$V_{IL}$				<b>0.3*V<sub>DD</sub></b>	V
WP Hysteresis		(Note 9)		0.14V <sub>DD</sub>		V
WP Input Current	$IL_{WPN}$		<b>0.20</b>		<b>35</b>	µA

#### **I<sup>2</sup>C Timing**

SCL Clock Frequency	$f_{SCL}$		<b>0</b>		<b>400</b>	kHz
I <sup>2</sup> C Clock High Time	$t_{SCH}$		<b>0.6</b>			µs
I <sup>2</sup> C Clock Low Time	$t_{SCL}$		<b>1.3</b>			µs
I <sup>2</sup> C Spike Rejection Filter Pulse Width	$t_{DSP}$		<b>0</b>		<b>50</b>	ns
I <sup>2</sup> C Data Set Up Time	$t_{SDS}$		<b>100</b>			ns
I <sup>2</sup> C Data Hold Time	$t_{SDH}$		<b>900</b>			ns
I <sup>2</sup> C SDA, SCL Input Rise Time	$t_{ICR}$	Dependent on Load (Note 10)		20 + 0.1*Cb	<b>1000</b>	ns
I <sup>2</sup> C SDA, SCL Input Fall Time	$t_{ICF}$	(Note 10)		20 + 0.1*Cb	<b>300</b>	ns
I <sup>2</sup> C Bus Free Time Between Stop and Start	$t_{BUF}$		<b>200</b>			µs
I <sup>2</sup> C Repeated Start Condition Set-up	$t_{STS}$		<b>0.6</b>			µs
I <sup>2</sup> C Repeated Start Condition Hold	$t_{STH}$		<b>0.6</b>			µs
I <sup>2</sup> C Stop Condition Set-up	$t_{SPS}$		<b>0.6</b>			µs
I <sup>2</sup> C Bus Capacitive Load	$C_b$				<b>400</b>	pF
SDA Pin Capacitance	$C_{SDA}$				<b>10</b>	pF
SCL Pin Capacitance	$C_s$				<b>10</b>	pF
EEPROM Write Cycle Time	$t_w$				<b>100</b>	ms

#### NOTES:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- $I_{DD}$  current may increase to 2mA for 45ms or less during each EEPROM programming operation.
- $AV_{DD}$  current may increase to 1mA for 30ms or less during each EEPROM programming operation.
- Simulated and Determined via Design and NOT Directly Tested.
- Simulated and Designed According to I<sup>2</sup>C Specifications.
- A typical Current of 20µA is Calculated using  $AV_{DD} = 10V$  and  $R_{SET} = 24.9k\Omega$ . Reference “ $R_{SET}$  Resistor” in Figure 2.
- Minimum value of  $R_{SET}$  resistor guaranteed when:  $AV_{DD} = 15V$ ,  $V_{DD} = 3.0V$  and when voltage on the  $V_{OUT}$  pin is greater than 2.5V. Reference Equation 2 on page 5 with Setting = 128.

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## Application Information

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the  $V_{COM}$  voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

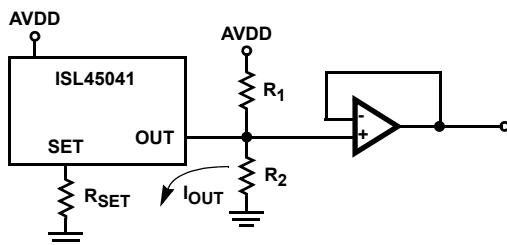


FIGURE 1. OUTPUT CONNECTION CIRCUIT EXAMPLE

The adjustment of the output is provided by the 2-wire  $I^2C$  serial interface.

### Expected Output Voltage

The ISL45041 provides an output sink current, which lowers the voltage on the external voltage divider ( $V_{COM}$  output voltage). Equation 1 and Equation 2 can be used to calculate the output current ( $I_{OUT}$ ) and output voltage ( $V_{OUT}$ ) values. The setting is the register value +1 with a value between 1 and 128.

$$I_{OUT} = \frac{\text{Setting} \times \frac{AV_{DD}}{20(R_{SET})}}{128} \quad (\text{EQ. 1})$$

$$V_{OUT} = \left( \frac{R_2}{R_1 + R_2} \right) AV_{DD} \left( 1 - \frac{\text{Setting} \times \frac{R_1}{20(R_{SET})}}{128} \right) \quad (\text{EQ. 2})$$

Table 1 gives the calculated value of  $V_{OUT}$  using the resistor values of:  $R_{SET} = 24.9\text{k}\Omega$ ,  $R_1 = 200\text{k}\Omega$ ,  $R_2 = 243\text{k}\Omega$ , and  $AV_{DD} = 10\text{V}$ .

TABLE 1.

SETTING VALUE	$V_{OUT}$
1	5.486
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109
90	3.936
100	3.764
110	3.592
128	3.282

### $R_{SET}$ Resistor

The external  $R_{SET}$  resistor sets the full-scale sink current,  $I_{SET}$  maximum, that determines the lowest voltage of the external voltage divider  $R_1$  and  $R_2$  (Figure 1). The voltage difference between the OUT pin and SET pin (Figure 2), which are also the drain and source of the output transistor, must be greater than 1.75V. This will keep the output transistor in its saturation region to maintain linear operation over the full range of register values. Expected current settings and 7-bit accuracy occurs when the output MOS transistor is operating in the saturation region. Figure 2 shows the internal connection for the output MOS transistor. The value of the  $AV_{DD}$  supply sets the voltage at the source of the output transistor. This voltage is equal to  $(\text{Setting}/128) \times (AV_{DD}/20)$ . The  $I_{SET}$  current is therefore equal to  $(\text{Setting}/128) \times (AV_{DD}/20 \times R_{SET})$ . The drain voltage is calculated using Equation 2. The values of  $R_1$  and  $R_2$  (Equation 2) should be determined using  $I_{OUT}$  maximum (setting equal to 128) so the minimum value of  $V_{OUT}$  is greater than  $1.75V + AV_{DD}/20$ .

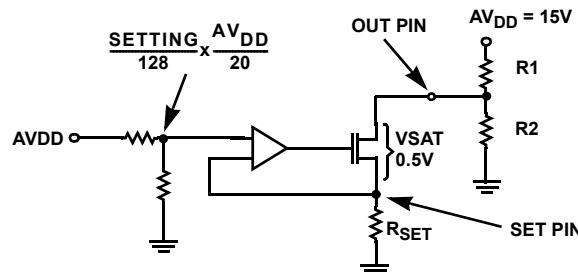


FIGURE 2. OUTPUT CONNECTION CIRCUIT EXAMPLE

### Ramp-Up of the VDD Power Supply

The ramp-up from 10%  $V_{DD}$  to 90%  $V_{DD}$  level must be achieved in 10ms or less to ensure that the EEPROM and power-on-reset circuits are synchronized and the correct value is read from the EEPROM Memory.

### Power Supply Sequence

The recommended power supply sequencing is shown in Figure 3. When applying power,  $V_{DD}$  should be applied before or at the same time as  $AV_{DD}$ . The minimum time for  $t_{VS}$  is 0 $\mu$ s. When removing power, the sequence of  $V_{DD}$  and  $AV_{DD}$  is not important.

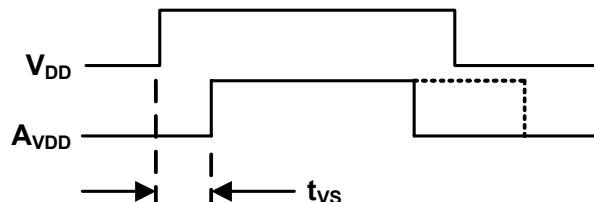
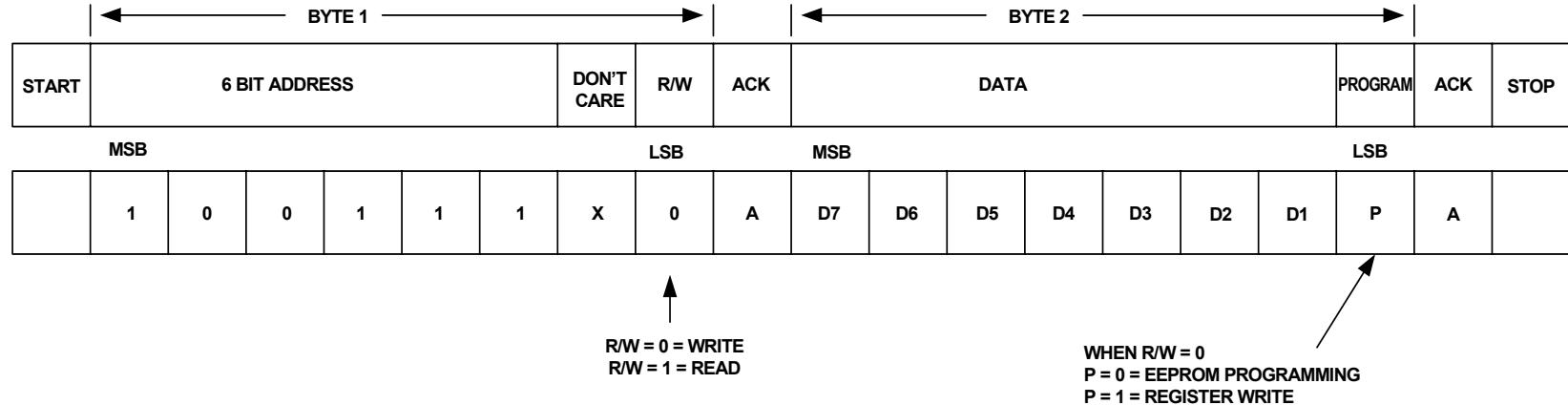


FIGURE 3. POWER SUPPLY SEQUENCE

Do not remove  $V_{DD}$  or  $AV_{DD}$  within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

## ***I<sup>2</sup>C Bus Format.***

### ISL45041 I<sup>2</sup>C WRITE FORMAT



### ISL45041 I<sup>2</sup>C READ FORMAT

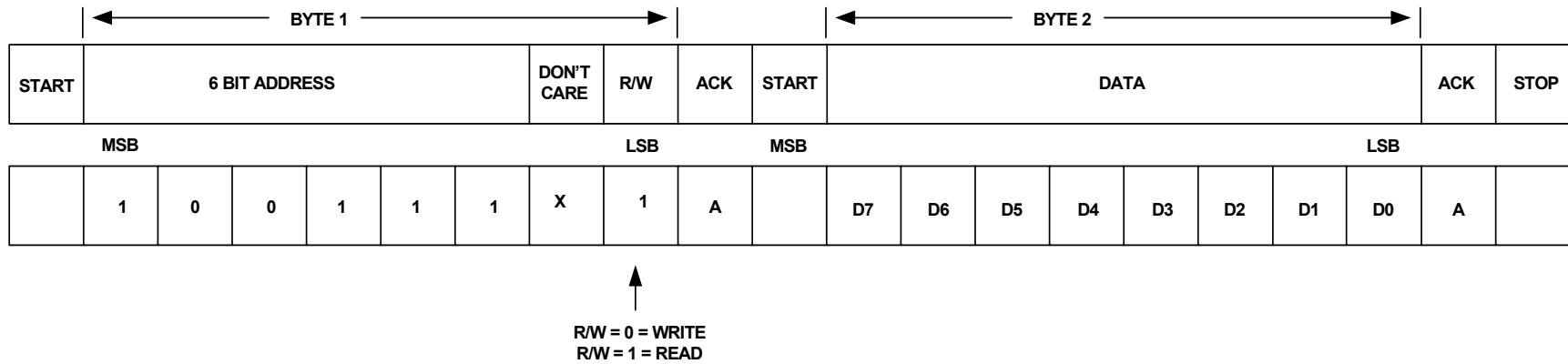


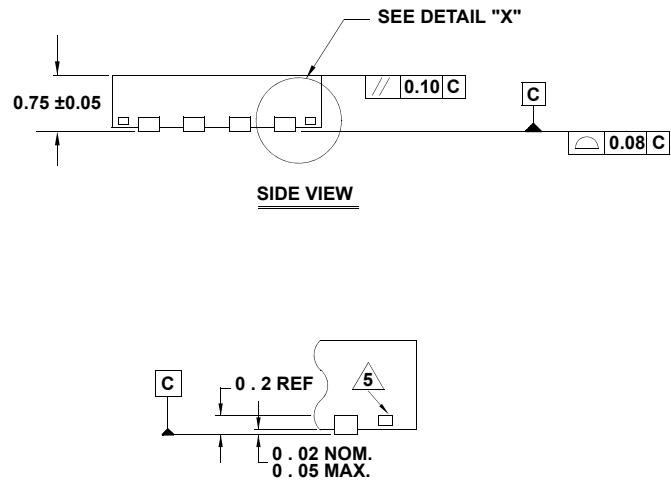
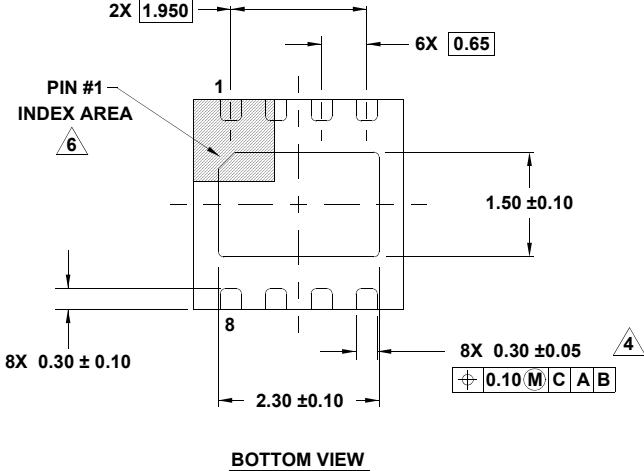
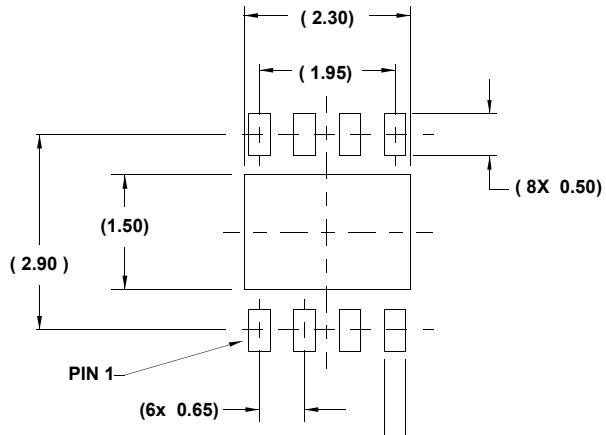
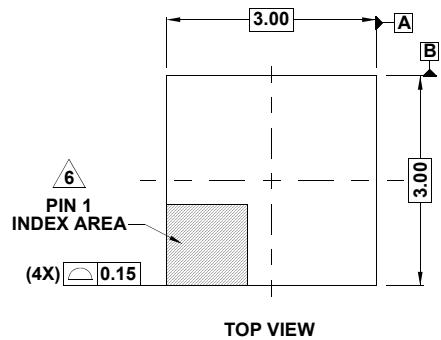
FIGURE 4. ISL45041 I<sup>2</sup>C READ AND WRITE FORMAT

## ***I<sup>2</sup>C Addressing***

The ISL45041 will respond identically to either of two I<sup>2</sup>C address: 1001110x and 1001111x. 100111x is the preferred address. To prevent bus conflicts, ensure that there are no other devices on the I<sup>2</sup>C bus with either of the above addresses.

## Package Outline Drawing

L8.3x3A

8 LEAD THIN FLAT NO-LEAD PLASTIC PACKAGE  
Rev 4, 2/10

### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.