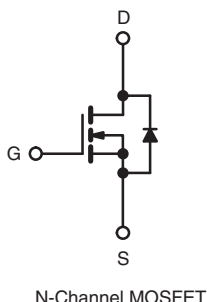
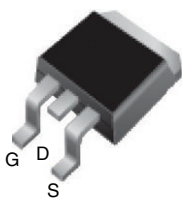


S Series Power MOSFET

PRODUCT SUMMARY

V_{DS} at T_J max. (V)	650	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.190
Q_g max. (nC)	98	
Q_{gs} (nC)	17	
Q_{gd} (nC)	25	
Configuration	Single	

D²PAK (TO-263)


FEATURES

- Generation one
- High E_{AR} capability
- Lower figure-of-merit $R_{on} \times Q_g$
- 100 % avalanche tested
- Ultra low R_{on}
- dV/dt ruggedness
- Ultra low gate charge (Q_g)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- PFC power supply stages
- Hard switching topologies
- Solar inverters
- UPS
- Motor control
- Lighting
- Server telecom



RoHS
COMPLIANT
HALOGEN
FREE
Available

ORDERING INFORMATION

Package	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHB22N60S-GE3
Lead (Pb)-free	SiHB22N60S-E3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	65	
Linear Derating Factor	D ² PAK (TO-263)	2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	690	mJ
Repetitive Avalanche Energy ^a	E_{AR}	25	
Maximum Power Dissipation	D ² PAK (TO-263)	250	W
Drain-Source Voltage Slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse Diode dV/dt ^d			
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

**THERMAL RESISTANCE RATINGS**

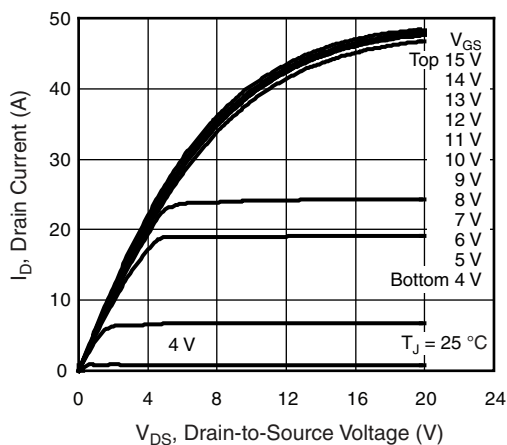
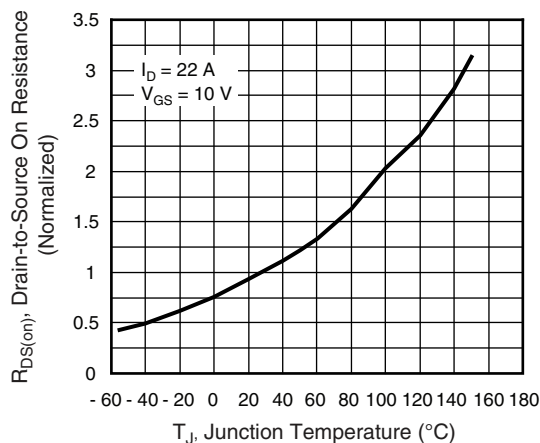
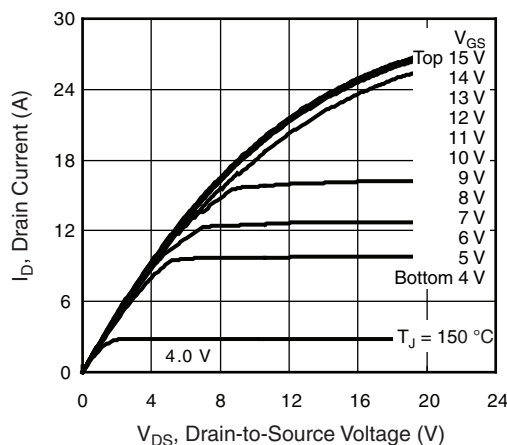
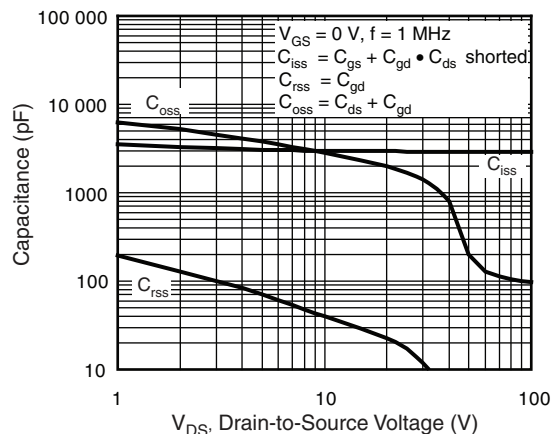
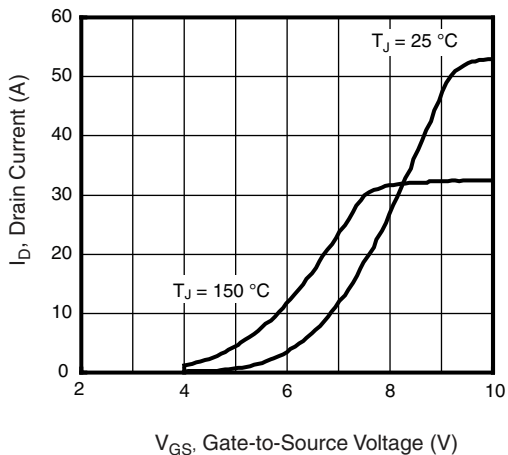
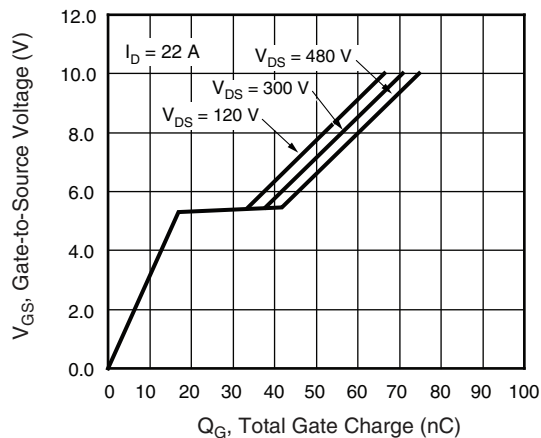
PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	D ² PAK (TO-263)	R _{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	D ² PAK (TO-263)	R _{thJC}	-	0.5	

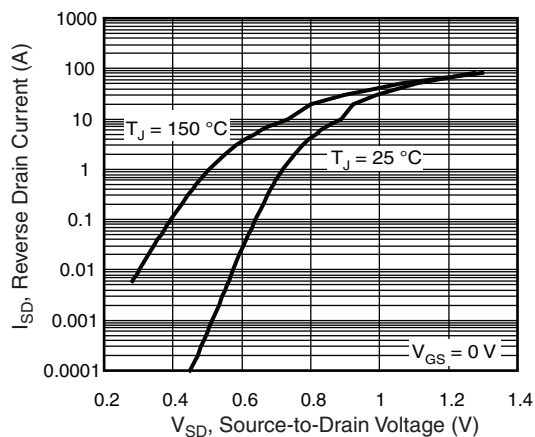
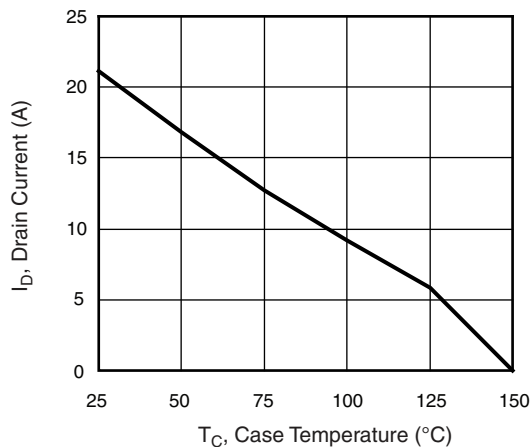
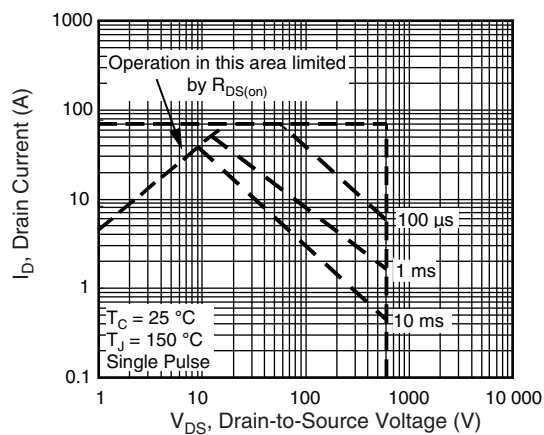
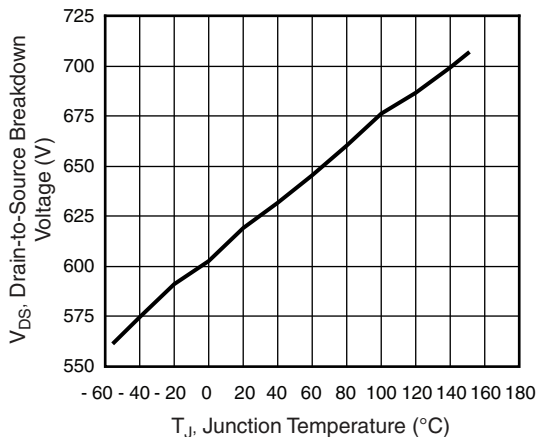
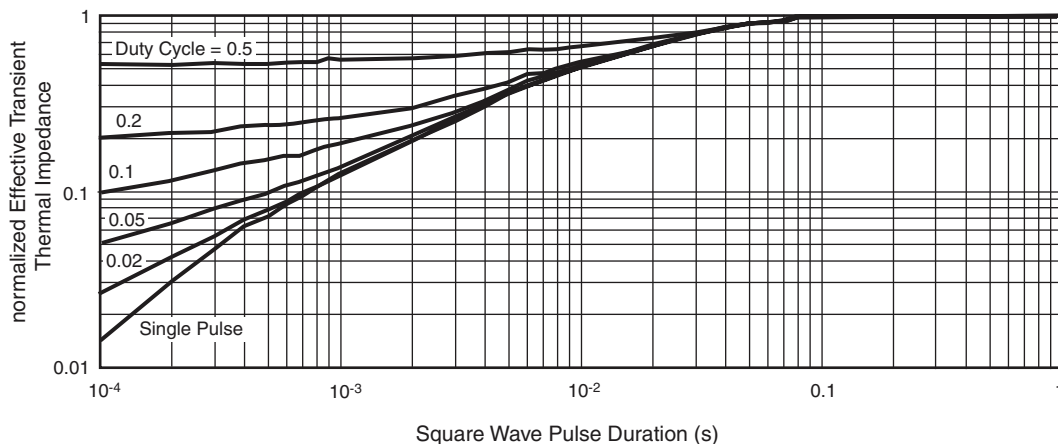
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

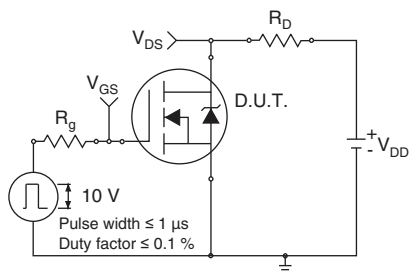
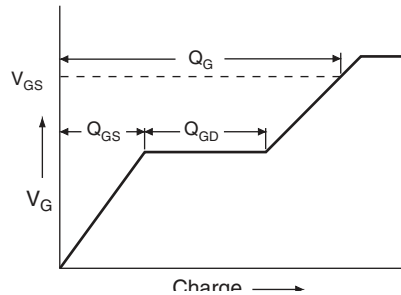
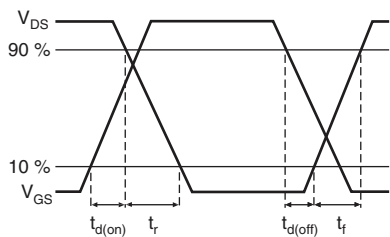
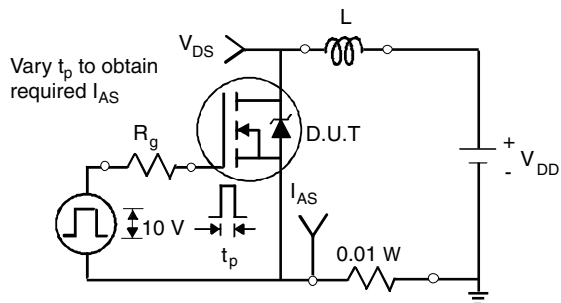
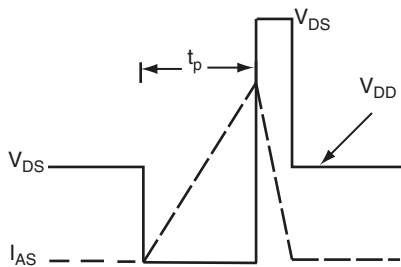
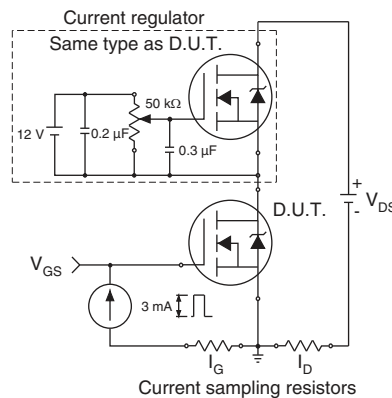
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA		600	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 600 V, V _{GS} = 0 V, T _J = 150 °C		-	-	100	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.160	0.190	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 50 V, I _D = 13 A		-	9.4	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz		-	2810	-	pF
Output Capacitance	C _{oss}			-	1480	-	
Reverse Transfer Capacitance	C _{rss}			-	33	-	
Effective Output Capacitance (Time Related)	C _{oss} eff. (TR) ^a	V _{GS} = 0 V	V _{DS} = 0 V to 480 V	-	155	-	nC
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 22 A, V _{DS} = 480 V	-	75	110	
Gate-Source Charge	Q _{gs}			-	17	-	
Gate-Drain Charge	Q _{gd}			-	25	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 380 V, I _D = 22 A, R _g = 9.1 Ω, V _{GS} = 10 V		-	24	50	ns
Rise Time	t _r			-	68	100	
Turn-Off Delay Time	t _{d(off)}			-	77	115	
Fall Time	t _f			-	59	90	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.65	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	22	A
Pulsed Diode Forward Current	I _{SM}			-	-	88	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 22 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 25 V		-	462	690	ns
Reverse Recovery Charge	Q _{rr}			-	8.3	16	μC
Reverse Recovery Current	I _{RRM}			-	30	60	A

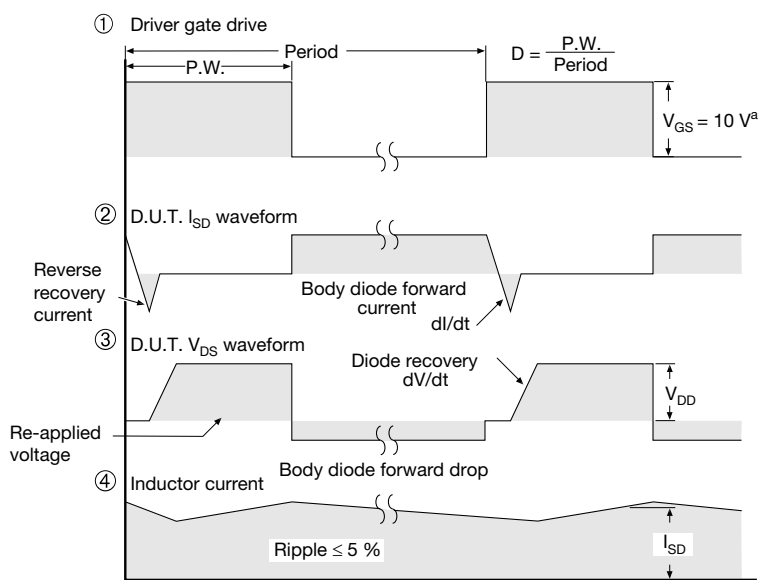
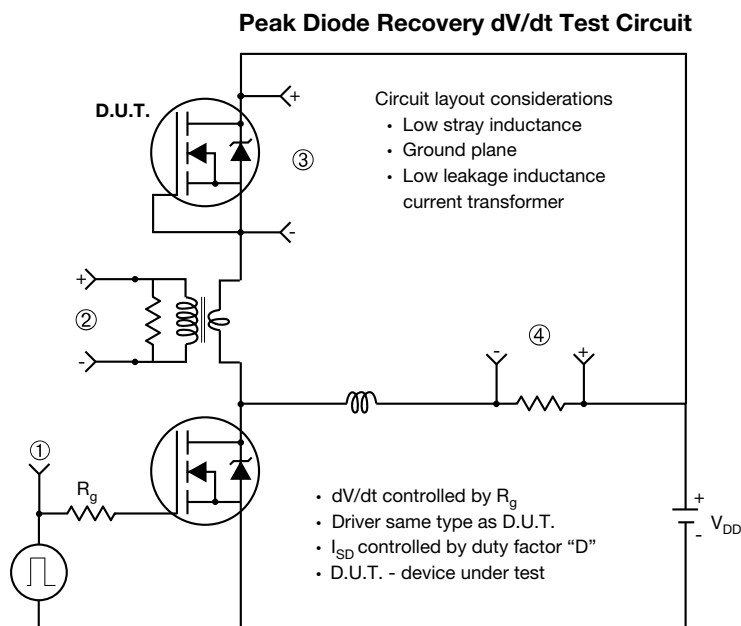
Note

a. C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_J = 25^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics, $T_J = 150^\circ\text{C}$

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Drain-to-Source Breakdown Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms

Fig. 17 - Gate Charge Test Circuit


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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